1. The instruction that is used to transfer the data from source operand to destination operand is

   a) data copy/transfer instruction

   b) branch instruction

   c) arithmetic/logical instruction

   d) string instruction

   Answer: A

   Explanation: these instructions are used to copy and transfer the instructions.
2. Which of the following is not a data copy/transfer instruction?

   a) MOV

   b) PUSH

   c) DAS

   d) POP

   Answer: c

   Explanation: DAS (Decimal Adjust after Subtraction) is an arithmetic instruction.
3. The instructions that involve various string manipulation operations are

   a) branch instructions

   b) flag manipulation instructions

   c) shift and rotate instructions

   d) string instructions

   Answer: d

   Explanation: The string instructions perform operations on strings such as load, move, scan, compare etc.
4. Which of the following instruction is not valid?

   a) MOV AX, BX

   b) MOV DS, 5000H

   c) MOV AX, 5000H

   d) PUSH AX

   Answer: b

   Explanation: both the source and destination operands cannot be memory locations except for string instructions.

5. In PUSH instruction, after each execution of the instruction, the stack pointer is
   a) incremented by 1
   b) decremented by 1
   c) incremented by 2
   d) decremented by 2
   Answer: d
   Explanation: The actual current stack-top is always occupied by the previously pushed data. So, the push operation decrements SP by 2 and then stores the two bytes contents of the operand onto the stack.
6. The instruction that pushes the contents of the specified register/memory location on to the stack is
   a) PUSHF
   b) POPF
   c) PUSH
   d) POP
   Answer: c
   Explanation: Since PUSH operation transfers data to stack from register or memory location.
7. In POP instruction, after each execution of the instruction, the stack pointer is
   a) incremented by 1
   b) decremented by 1
   c) incremented by 2
   d) decremented by 2
   Answer: c
   Explanation: The actual current stack top is poped into the specific operand as the contents of stack top memory is stored in AL&SP and further contents of memory location pointed to by SP are copied to AH & SP.
8. The instructions that are used for reading an input port and writing an output port respectively are
   a) MOV, XCHG

b) MOV, IN

c) IN, MOV

d) IN, OUT

Answer: d

Explanation: The address of the input/output port may be specified directly or indirectly.

Example for input port: IN AX, DX ; This instruction reads data from a 16-bit port whose address is in DX and stores it in AX

Example for output port: OUT 03H, AL ;This sends data available in AL to a port whose address is 03H.

9. The instruction that is used for finding out the codes in case of code conversion problems is

   a) XCHG

   b) XLAT

   c) XOR

   d) JCXZ

   Answer: b

   Explanation: the translate(XLAT) instruction is used to find codes.

10. The instruction that loads effective address formed by destination operand into the specified source register is

    a) LEA

    b) LDS

    c) LES

    d) LAHF

    Answer: a

    Explanation: the instruction, LEA loads effective address and is more useful for assembly language rather than for machine language.

11. The instruction that loads the AH register with the lower byte of the flag register is

    a) SAHF

    b) AH

    c) LAHF

    d) PUSHF

Answer: c

Explanation: The instruction LAHF(Load AH from lower byte of Flag) may be used to observe the status of all the condition code flags(except overflow flag) at a time.

12. In the RCL instruction, the contents of the destination operand undergoes function as

    a) carry flag is pushed into LSB & MSB is pushed into carry flag

    b) carry flag is pushed into MSB & LSB is pushed into carry flag

    c) auxiliary flag is pushed into LSB & MSB is pushed into carry flag

    d) parity flag is pushed into MSB & LSB is pushed into carry flag

    Answer: a

    Explanation: In RCL(Rotate right through carry), for each operation, the carry flag is pushed into LSB and the MSB of the operand is pushed into carry flag.

13. The instructions that are used to call a subroutine from a main program and return to the main program after execution of called function are

    a) CALL,JMP

    b) JMP,IRET

    c) CALL,RET

    d) JMP,RET

    Answer: c

    Explanation: At each CALL instruction, the IP and CS of the next instruction is pushed onto stack, before the control is transferred to the procedure. At the end of procedure the RET instruction must be executed to retrieve the stored contents of IP & CS registers from stack.

14. Which of the following is not a machine controlled instruction?

    a)HLT

    b) CLC

    c) LOCK

    d) ESC

    Answer: b

    Explanation: Since CLC is a flag manipulation instruction where CLC stands for Clear Carry Flag.

15. The instruction, MOV AX, 0005H belongs to the address mode

    a) register

    b) direct

    c) immediate

    d) register relative

    Answer: c

    Explanation: In Immediate addressing mode, immediate data is a part of instruction and appears in the form of successive byte or bytes.

16. The instruction, MOV AX, 1234H is an example of

    a) register addressing mode

    b) direct addressing mode

    c) immediate addressing mode

    d) based indexed addressing mode

    Answer: c

    Explanation: since immediate data is present in the instruction.

17. If the data is present in a register and it is referred using the particular register, then it is

    a) direct addressing mode

    b) register addressing mode

    c) indexed addressing mode

    d) immediate addressing mode

    Answer: b

    Explanation: Since register is used to refer the address.

18. The instruction, MOV AX,[BX] is an example of

    a) direct addressing mode

    b) register addressing mode

    c) register relative addressing mode

    d) register indirect addressing mode

    Answer: d

    Explanation: Since the register used to refer the address is accessed indirectly.

19. If the offset of the operand is stored in one of the index registers, then it is

    a) based indexed addressing mode

b) relative based indexed addressing mode

c) indexed addressing mode

d) none of the mentioned

Answer: c

Explanation: in indexed addressing mode, the offset of operand is stored and in the rest of them, address is stored.

20. The instruction, JMP 5000H:2000H; is an example of

a) intrasegment direct mode

b) intrasegment indirect mode

c) intersegment direct mode

d) intersegment indirect mode

Answer: c

Explanation: since in intersegment direct mode, the address to which the control is to be transferred is in a different segment.

21. The contents of a base register are added to the contents of index register in

a) indexed addressing mode

b) based indexed addressing mode

c) relative based indexed addressing mode

d) based indexed and relative based indexed addressing mode

Answer: d

Explanation: The effective address is formed by adding the contents of both base and index registers to a default segment.

22. The stack pointer register contains

a) address of the stack segment

b) pointer address of the stack segment

c) offset of address of stack segment

d) data present in the stack segment

Answer: c

Explanation: The stack pointer register contains the offset of the address of the stack segment.

23. The stack segment register contains

    a) address of the stack segment

    b) base address of the stack segment

    c) pointer address of the stack segment

    d) data in the stack segment

    Answer: b

    Explanation: The stack segment register contains base address of the stack segment in the memory. The stack pointer register (sP) and stack segment register (SS) together address the stack-top.

24. PUSH operation

    a) decrements SP

    b) increments SP

    c) decrements SS

    d) increments SS

    Answer: a

    Explanation: Each PUSH operation decrements the SP (Stack Pointer) register.

25. POP operation

    a) decrements SP

    b) increments SP

    c) decrements SS

    d) increments SS

    Answer: b

    Explanation: Each POP operation increments the SP (Stack Pointer) register.

26. The register or memory location that is pushed into the stack at the end must be

    a) popped off last

    b) pushed off first

    c) popped off first

    d) pushed off last

    Answer: c

    Explanation: The data can be retrieved by POP operation and as in stack, the data that is pushed at the end must be popped off first.

27. In the instruction, ASSUME CS : CODE, DS : DATA, SS : STACK
    the ASSUME directive directs to the assembler the
    a) address of the stack segment
    b) pointer address of the stack segment
    c) name of the stack segment
    d) name of the stack, code and data segments
    Answer: d
    Explanation: the directive ASSUMES facilitates to name the segments with desired name that is not a mnemonic or keyword.
28. When a stack segment is initialized then
    a) SS and SP are initialized
    b) only SS is initialized
    c) only SP is initialized
    d) SS and SP need not be initialized
    Answer: a
    Explanation: though the Stack segment is initialized, the SS and SP pointers must be initialized.
29. The number of PUSH instructions and POP instructions in a subroutine must be
    a) PUSH instructions must be greater than POP instructions
    b) POP instructions must be greater than PUSH instructions
    c) both must be equal
    d) instructions may be any kind
    Answer: c
    Explanation: The number of PUSH instructions must be equal to the number of POP instructions.
30. 8086 does not support
    a) arithmetic operations
    b) logical operations
    c) BCD operations
    d) direct BCD packed multiplication

Answer: d

Explanation: the 8086 microprocessor does not support direct BCD packed operations.

31. For 8086 microprocessor, the stack segment may have a memory block of a maximum of

a) 32K bytes

b) 64K bytes

c) 16K bytes

d) NONE

Answer: b

Explanation: In 8086 microprocessor, the memory segments each have a memory of 64K bytes.

32. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple B. single C. double D. triple

ANSWER: B

33. Microprocessor is a/an _____ circuit that functions as the CPU of the compute

A. electronic B. mechanic C. integrating D. processing

ANSWER: A

34. Microprocessor is the _____ of the computer and it perform all the computational tasks

A. main B. heart C. important D. simple

ANSWER: B

35. The purpose of the microprocessor is to control _____

A. memory B. switches C. processing D. tasks

ANSWER: A

36. The first digital electronic computer was built in the year_____

A. 1950 B. 1960 C. 1940 D. 1930

ANSWER: C

37. In 1960's texas institute invented _____

A. integrated circuits B. microprocessor C. vacuum tubes D. transistors

ANSWER: A

38. The intel 8086 microprocessor is a _____ processor

A. 8 bit B. 16 bit C. 32 bit D. 4 bit

ANSWER: B

39. The microprocessor can read/write 16 bit data from or to _____

A. memory B. I /O device C. processor D. register

ANSWER: A

40. In 8086 microprocessor , the address bus is _____ bit wide

A. 12 bit B. 10 bit C. 16 bit D. 20 bit

ANSWER: D

41. The work of EU is _____

A. encoding B. decoding C. processing D. calculations

ANSWER: B

42. The 16 bit flag of 8086 microprocessor is responsible to indicate _____

A. the condition of result of ALU operation B. the condition of memory

C. the result of addition D. the result of subtraction

ANSWER: A

43. The CF is known as _____

A. carry flag B. condition flag C. common flag D. single flag

.ANSWER: A

44. The SF is called as _____

A. service flag B. sign flag C. single flag D. condition flag

ANSWER: B

45. The OF is called as _____

A. overflow flag B. overdue flag C. one flag D. over flag

ANSWER: A

46. The IF is called as _____

A. initial flag B. indicate flag C. interrupt flag D. inter flag

ANSWER: C

47. The register AX is formed by grouping _____

A. AH & AL B. BH & BL C. CH & CL D. DH & DL

ANSWER: A

48. The SP is indicated by _____

A. single pointer B. stack pointer C. source pointer D. destination pointer

ANSWER: B

49. The BP is indicated by _____

A. base pointer B. binary pointer C. bit pointer D. digital pointer

ANSWER: A

50. The SS is called as _____

A. single stack B. stack segment C. sequence stack .D. random stack

ANSWER: B

51. The index register are used to hold _____

A. memory register B. offset address C. segment memory D. offset memory

ANSWER: A

52. The BIU contains FIFO register of size _____ bytes

A. 8 B. 6 C. 4 D. 12

ANSWER: B

53. The BIU prefetches the instruction from memory and store them in _____

A. queue B. register C. memory D. stack

ANSWER: A

54. The 1 MB byte of memory can be divided into _____ segment

A. 1 Kbyte B. 64 Kbyte C. 33 Kbyte D. 34 Kbyte

ANSWER: B

55. The DS is called as _____

A. data segment B. digital segment C. divide segment D. decode segment

ANSWER: A

56. The CS register stores instruction _____ in code segment

A. stream B. path C. codes D. stream line

ANSWER: C

57. The IP is _____ bits in length

A. 8 bits B. 4 bits C. 16 bits D. 32 bits

ANSWER: C

58. The push source copies a word from source to _____

A. stack B. memory C. register D. destination

ANSWER: A

59. LDs copies to consecutive words from memory to register and _____

A. ES B. DS C. SS D. CS

ANSWER: B

60. INC destination increments the content of destination by _____

A. 1 B. 2 C. 30 D. 41

ANSWER: A

61. IMUL source is a signed _____

A. multiplication B. addition C. subtraction D. division

ANSWER: A

62. _____destination inverts each bit of destination

A. NOT B. NOR C. AND D. OR

ANSWER: A

63. The JS is called as _____

A. jump the signed bit B. jump single bit

C. jump simple bit D. jump signal it

ANSWER: A

64. Instruction providing both segment base and offset address are called _____

A. below type .B. far type C. low type D. high type

ANSWER: B

65. The conditional branch instruction specify _____ for branching

A. conditions B. instruction C. address D. memory

ANSWER: A

66. The microprocessor determines whether the specified condition exists or not by testing the_____

A. carry flag B. conditional flag C. common flag D. sign flag

ANSWER: B

67. The LES copies to words from memory to register and _____

A. DS B. CS C. ES D. DS

ANSWER: C

68. The _____ translates a byte from one code to another code

A. XLAT B. XCHNG C. POP D. PUSH

ANSWER: A

69. The _____ contains an offset instead of actual address

A. SP B. IP C. ES D. SS

ANSWER: B

70. The 8086 fetches instruction one after another from _____ of memory

A. code segment B. IP C. ES D. SS

ANSWER: A

71. The BIU contains FIFO register of size 6 bytes called _____.

A. queue B. stack C. segment D. register

ANSWER: A

72. The _____ is required to synchronize the internal operands in the processor CLK Signal

A. UR Signal B. Vcc C. AIE D. Ground

ANSWER: A

73. The pin of minimum mode AD0-AD15 has _____ address

A. 16 bit B. 20 bit C. 32 bit D. 4 bit

ANSWER: B

74. The pin of minimum mode AD0- AD15 has _____ data bus

A. 4 bit B. 20 bit C. 16 bit D. 32 bit

ANSWER: C

75. The address bits are sent out on lines through _____

A. A16-19 B. A0-17 C. D0-D17 D. C0-C17

ANSWER: A

76. _____ is used to write into memory

A. RD B. WR C. RD / WR D. CLK

ANSWER: B

77. The functions of Pins from 24 to 31 depend on the mode in which _____ is operating

A. 8085 B. 8086 C. 80835 D. 80845

ANSWER: B

78. The RD, WR, M/IO is the heart of control for a _____ mode

A. minimum B. maximum C. compatibility mode D. control mode

ANSWER: A

79. In a minimum mode there is a _____ on the system bus

A. single B. double C. multiple D. triple

ANSWER: A

80. If MN/MX is low the 8086 operates in _____ mode

A. Minimum B. Maximum C. both (A) and (B) D. medium

ANSWER: B

81. In max mode, control bus signal So,S1 and S2 are sent out in _____ form

A. decoded B. encoded C. shared D. unshared

ANSWER: B

82. The ___ bus controller device decodes the signals to produce the control bus signal

A. internal B. data C. external D. address

ANSWER: C

83. A _____ Instruction at the end of interrupt service program takes the execution back to the interrupted program

A. forward B. return C. data D. line

ANSWER: B

84. The main concerns of the _____ are to define a flexible set of commands

A. memory interface B. peripheral interface

C. both (A) and (B) D. control interface

.ANSWER: A

85. Primary function of memory interfacing is that the _____ should be able to read from and write into register

A. multiprocessor B. microprocessor C. dual Processor D. coprocessor

ANSWER: B

86. To perform any operations, the Mp should identify the _____

A. register B. memory C. interface D. system

ANSWER: A

87. The Microprocessor places _____ address on the address bus

A. 4 bit B. 8 bit C. 16 bit D. 32 bit

ANSWER: C

88. The Microprocessor places 16 bit address on the add lines from that address by _____ register should be selected

A. address B. one C. two D. three

ANSWER: B

89. The _____of the memory chip will identify and select the register for the EPROM

A. internal decoder B. external decoder C. address decoder D. data decoder

ANSWER: A

90. Microprocessor provides signal like ____ to indicate the read operatio

A. LOW B. MCMW C. MCMR D. MCMWR

ANSWER: C

91. To interface memory with the microprocessor, connect register the lines of the address bus must be added to address lines of the _____ chip.

A. single B. memory C. multiple D. triple

ANSWER: B

92. The remaining address line of _____ bus is decoded to generate chip select signal

A. data B. address C. control bus D. both (a) and (b)

ANSWER: B

93. _____ signal is generated by combining RD and WR signals with IO/M

A. control B. memory C. register D. system

ANSWER: A

94. Memory is an integral part of a _____ system

A. supercomputer B. microcomputer

C. mini computer D. mainframe computer

ANSWER: B

95. _____ has certain signal requirements write into and read from its registers

A. memory B. register C. both (a) and (b) D. control

ANSWER: A

96. An _____ is used to fetch one address

A. internal decoder B. external decoder C. encoder D. register

ANSWER: A

97. The primary function of the _____ is to accept data from I/P devices

A. multiprocessor B. microprocessor C. peripherals D. interfaces

ANSWER: B

98. _____ signal prevent the microprocessor from reading the same data more than one

A. pipelining B. handshaking C. controlling D. signaling

ANSWER: B

99. Bits in IRR interrupt are _____

A. reset B. set C. stop D. start

ANSWER: B

100. _____ generate interrupt signal to microprocessor and receive acknowledge

A. priority resolver B. control logic

C. interrupt request register D. interrupt register

ANSWER: B

101. The _____ pin is used to select direct command word

A. A0 B. D7-D6 C. A12 D. AD7-AD6

ANSWER: A

102. The _____ is used to connect more microprocessor

A. peripheral device B. cascade C. I/O devices D. control unit

ANSWER: B

103. CS connect the output of _____

A. encoder B. decoder C. slave program D. buffer

ANSWER: B

104. In which year, 8086 was introduced?

A. 1978 B. 1979 C. 1977 D. 1981

ANSWER: A

105. 8086 and 8088 contains _____ transistors

A. 29000B. 24000 C. 34000 D. 54000

ANSWER: A

106. ALE stands for _____

A. address latch enable B. address level enable

C. address leak enable D. address leak extension

ANSWER: A

107. What is DEN?

A. direct enable B. data entered C. data enable D. data encoding

ANSWER: C

108. In 8086, Example for Non maskable interrupts are _____.

A. TRAP B. RST6.5 C. INTR D. RST6.6

ANSWER: A

109. In 8086 the overflow flag is set when _____.

a. the sum is more than 16 bits.

b. signed numbers go out of their range after an arithmetic operation.

c. carry and sign flags are set.

d. subtraction

ANSWER: B

110. In 8086 microprocessor the following has the highest priority among all type interrupts?

A. NMI B. DIV 0 C. TYPE 255 D. OVER FLOW

ANSWER: A

111. In 8086 microprocessor one of the following statements is not true?

A. coprocessor is interfaced in max mode. B. coprocessor is interfaced in min mode.

C. I /O can be interfaced in max / min mode. D. supports pipelining

ANSWER: B

112. Address line for TRAP is?

A. 0023H B. 0024H C. 0033H D. 0099H

ANSWER: B

113. Access time is faster for _____.

A. ROM B. SRAM C. DRAM D. ERAM

ANSWER: B

114. The First Microprocessor was_____.

A. Intel 4004 B. 8080 C. 8085 D. 4008

ANSWER: A

115. Status register is also called as _____.

A. accumulator B. stack C. counter D. flags

ANSWER: D

116. Which of the following is not a basic element within the microprocessor?

A. Microcontroller B. Arithmetic logic unit (ALU)

C. Register array D. Control unit

Ans.: A

117. Which method bypasses the CPU for certain types of data transfer?

A. Software interrupts B. Interrupt-driven I/O

C. Polled I/O D. Direct memory access (DMA)

Ans.: D

118. Which bus is bidirectional?

A. Address bus B. Control bus

C. Data bus D. None of the above

Ans.: C

119. The first microprocessor had a(n)_____.

A. 1 – bit data bus B. 2 – bit data bus

C. 4 – bit data bus D. 8 – bit data bus

Ans.: C

120. Which microprocessor has multiplexed data and address lines?

A. 8086 B. 80286 C. 80386 D. Pentium

Ans.: A

121. Which is not an operand?

A. Variable B. Register C. Memory location D. Assembler

Ans.: D

122. Which is not part of the execution unit (EU)?

A. Arithmetic logic unit (ALU) B. Clock

C. General registers D. Flags

Ans.: B

123. A 20-bit address bus can locate _____.

A. 1,048,576 locations B. 2,097,152 locations

C. 4,194,304 locations D. 8,388,608 locations

Ans.: A

124. Which of the following is not an arithmetic instruction?

A. INC (increment) B. CMP (compare)

C. DEC (decrement) D. ROL (rotate left)

Ans.: D

125. During a read operation the CPU fetches _____.

A. a program instruction B. another address

C. data itself D. all of the above

Ans.: D

126. Which of the following is not an 8086/8088 general-purpose register?

A. Code segment (CS) B. Data segment (DS)

C. Stack segment (SS) D. Address segment (AS)

Ans.: D

127. A 20-bit address bus allows access to a memory of capacity

A. 1 MB B. 2 MB C. 4 MB D. 8 MB

Ans.: A

128. Which microprocessor accepts the program written for 8086 without any changes?

A. 8085 B. 8086 C. 8087 D. 8088

Ans.: D

129. Which group of instructions do not affect the flags?

A. Arithmetic operations B. Logic operations

C. Data transfer operations D. Branch operations

Ans.: C

130. The result of MOV AL, 65 is to store

A. store 0100 0010 in AL B. store 42H in AL

C. store 40H in AL D. store 0100 0001 in AL

Ans.: D

131. 8086 HAVE———————— of segment registers

A. 2 B. 4 C. 6 D. 8

ANSWER: B

132. 8086 can be operated in Two modes they are ——————————and——————

A. Minimum, Maximum B. External, internal

C. Mode1, Mode2 D. Data, address

ANSWER: A

133. Which of the following is the function of microprocessor?

A. Receiving input B. Performing computations.

C. Storing data & instructions D. All of the these

ANSWER: D

134. If there are two operands, the _____ operand appears first.

A. destination B. Destination C. source D. label

ANSWER: A

135. 8086 processor has ————- address pins out of which ————- number of pins are used as data pins

A. 16,8 B. 16,14 C. 20,16 D. 20,8

ANSWER: C

136. In 8086 is a ————bit microprocessor and is fabricated using ———— technology

A. 16,CMOS B. 8,HMOS C. 20,NMOS D. 16,HMOS

ANSWER: D

137. Data storage in stack is designed in _____method.

A. First in first out B. last in last out

C. first in last out D. last in first out

ANSWER: D

138. ————flag is used in 8086 for string manipulation instructions

A. DF B. AF C. OF D. PF

ANSWER: A

139. BHE of 8086 microprocessor signal is used to interface the

A. Even bank memory B. Odd bank memory

C. I/O D. DMA

ANSWER: B

140. In 8086 microprocessor one of the following statements is not true.

A. Coprocessor is interfaced in MAX mode

B. Coprocessor is interfaced in MIN mode

C. I/O can be interfaced in MAX / MIN mode

D. Supports pipelining

ANSWER: D

141. In 8086 the overflow flag is set when

A. The sum is more than 16 bits

B. Signed numbers go out of their range after an arithmetic operation

C. Carry and sign flags are set D. During subtraction

ANSWER: B

142. Using assembly language with c++ for 16 bit application compilation and linking process performed at _____

a. Command line **b.** Word pad c. Note pad d. None of the above

143. In assembly language with C/C++ 16 bit application programs are generated using _____

a. MS_word b. DOS edit only c. Note pad or word pad only

d. Either b or c

144. For inline assembly code we have to use _____

a. Only upper case characters **b. Only lower case characters**

c. either upper or lower case characters d. Mixedmode

145. Which compiler switch recognized by both 16 Bit and 32 Bit C++ compiler

a. /G1 b. /G2,/G4 c. /G1,/G3 **d. /G3,/G4,/G5,/G6**

146. Which compiler switch select the 80188/80186/80286

a) /G1 **b) /G2** **c)** /G3 d) /Gs

Unit 5

1. The 8051 microcontroller is of ___pin package as a _____ processor.

a) 30, 1byte b) 20, 1 byte c) 40, 8 bit d) 40, 8 byte

2. The SP is of ___ wide register. And this may be defined anywhere in the _____.

a) 8 byte, on-chip 128 byte RAM. b) 8 bit, on chip 256 byte RAM.

c) 16 bit, on-chip 128 byte ROM d) 8 bit, on chip 128 byte RAM.

3. After reset, SP register is initialized to address_____.

a) 8H b) 9H c) 7H d) 6H

4. What is the address range of SFR Register bank?

a) 00H-77H b) 40H-80H c) 80H-7FH d) 80H-FFH

5. Which pin of port 3 is has an alternative function as write control signal for external data memory?

a) P3.8 b) P3.3 c) P3.6 d) P3.1

6. What is the Address (SFR) for TCON, SCON, SBUF, PCON and PSW respectively?

a) 88H, 98H, 99H, 87H, 0D0H. b) 98H, 99H, 87H, 88H, 0D0H

c) 0D0H, 87H, 88H, 99H, 98H d) 87H, 88H, 0D0H, 98H, 99H

7. Match the following:

1) TCON i) contains status information

2) SBUF ii) timer / counter control register.

3) TMOD iii) idle bit, power down bit

4) PSW iv) serial data buffer for Tx and Rx.

5) PCON v) timer/ counter modes of operation.

a) 1->ii, 2->iv, 3->v, 4->i, 5->iii. b) 1->i, 2->v, 3->iv, 4->iii, 5->ii.

c) 1->v, 2->iii, 3->ii, 4->iv, 5->i. d) 1->iii, 2->ii, 3->i, 4->v, 5->iv.

8. Which of the following is of bit operations?

i) SP

ii) P2

iii) TMOD

iv) SBUF

v) IP

a) ii, v only b) ii, iv, v only c) i, v only d) iii, ii only

9. Serial port interrupt is generated, if ____ bits are set

a) IE b) RI, IE c) IP, TI d) RI, TI

10. In 8051 which interrupt has highest priority?

a)IE1 b)TF0 c)IE0 d)TF1

11. Intel 8096 is of ___ bit microcontroller family called as _____.

a) 8, MCS51 b) 16, MCS51 c) 8, MCS96 d) 16, MCS96

12. 8096 has following features fill up the following,

i) ____ Register file,

ii) ____ I/O Ports

iii) ____ architecture.

a) 256 byte, five 8bit, register to register

b) 256 byte, four 8bit, register to register

c) 232 byte, five 8bit, register to register

d) 232 byte, six 8 bit, register to register

13. How many synchronous and asynchronous modes are there in serial port of 8096?

a) 2, 2 respectively b) 3,1 respectively c) 1, 3 respectively d) 1, 2 respectively

14. In 8096 we have _____interrupt sources and _____ interrupt vectors.

a) 18, 8 b) 21, 6 c) 21, 8 d) 16, 8

15. 8096 has ___ general purpose I/O ports, Port 2 includes _____ of the following

i) two quasi-bidirectional I/O lines

ii) two output lines

iii) four input lines

iv) open drain outputs

a) 4, i, iv b) 6, ii, iii c) 4, i,ii,iii d) 6, i, ii, iv

16. 8096 write-protected mode, no code can write to memory address between __.

a) 2020 to 3FFFH b) 8000 to FFFFH c) 2000 to 3FFFH d) 2020 to 202FH

17. If the __ pin is ___ , then we have the option of using the ____ ROM or EPROM together with _____ memory and devices.

a) EA, high, internal, external

b) EA, low, internal, external

c) EA, high, external, internal

d) EA, low, external, internal

18. In 8096, CCB bit 3 is ____.

a) write strobe mode select b) address valid strobe select

c) bus width select d) Internal read control mode

19. In 8096, mode ____ of serial port are ___ modes commonly used for ____ communications.

a) 1, 8bit, single processor b) 0, 7bit, multiple microcontroller

c) 2, 9 bit, multiple processors d) 3, 8 bit, multiple microcontroller

20. What is the function of watchdog timer?

a) The watchdog Timer is an external timer that resets the system if the software fails to operate properly.

b) The watchdog Timer is an internal timer that sets the system if the software fails to operate properly.

c) The watchdog Timer is an internal timer that resets the system if the software fails to operate properly.

d) None of them

Key:

5.1 C 5.2 D 5.3 C 5.4 D 5.5 C 5.6 A 5.7 A 5.8 A 5.9 D 5.10 C 5.11 D 5.12 C 5.13 C 5.14 C 5.15 C 5.16 C 5.17 A 5.18 B 5.19 C 5.20 C

8051 Microcontroller Questions and Answers – Interrupt Programming

1. When any interrupt is enabled, then where does the pointer moves immediately after this interrupt has occurred?

a) to the next instruction which is to be executed

b) to the first instruction of ISR

c) to the first location of the memory called the interrupt vector table

d) to the end of the program

Answer: c

Explanation: When any interrupt is enabled, then it goes to the vector table where the address of the ISR is placed.

2. What are the contents of the IE register, when the interrupt of the memory location 0x00 is caused?

a) 0xFFH

b) 0x00H

c) 0x10H

d) 0xF0H

View Answer

Answer: b

Explanation: When interrupt of 0x00 is caused (the reset interrupt) then all the other interrupts will be disabled or the contents of the IE register becomes null.

3. After RETI instruction is executed then the pointer will move to which location in the program?

a) next interrupt of the interrupt vector table

b) next instruction of the program after the IE instruction

c) next instruction after the RETI in the memory

d) none of the mentioned

Answer: b

Explanation: When the RETI instruction is executed, it will execute the instruction present at the top of the stack (which is the PC's value i.e after the interrupt enable instruction).

4. Which pin of the external hardware is said to exhibit INT0 interrupt?

a) pin no 10

b) pin no 11

c) pin no 12

d) pin no 13

Answer: c

Explanation: INT0 interrupt is caused when pin no 12 in the hardware of the 8051 controller is enabled with a low levelled pulse.

5. Which bit of the IE register is used to enable TxD/RxD interrupt?

a) IE.D5

b) IE.D2

c) IE.D3

d) IE.D4

Answer: d

Explanation: IE.D4 is used to enable RS interrupt or the serial communication interrupt.

6. Which of the following combination is the best to enable the external hardware interrupt 0 of the IE register (assuming initially all bits of the IE register are zero)?

a) EX0=1

b) EA=1

c) any of the mentioned

d) both of the mentioned

Answer: d

Explanation: For executing the EX0 interrupt, the EX0 and EA bits of the IE register should be set. EA is set to enable all the interrupts and EX0 is set to enable the external hardware interrupt 0 interrupt and mask the other enabled interrupts.

7. Why normally LJMP instructions are the topmost lines of the ISR?

a) so as to jump to some other location where there is a wider space of memory available to write the codes

b) so as to avoid overwriting of other interrupt instructions

c) both of the mentioned

d) none of the mentioned

Answer: c

Explanation: There is a small space of memory present in the vector table between two different interrupts so in order to avoid overwriting of other interrupts we normally jump to other locations where a wide range of space is available.

8. Which register is used to make the pulse a level or a edge triggered pulse?

a) TCON

b) IE

c) IPR

d) SCON

Answer: a

Explanation: TCON register is used to make any pulse level or edge triggered one.

9. What is the disadvantage of a level triggered pulse?

a) a constant pulse is to be maintained for a greater span of time

b) difficult to analyse its effects

c) it is difficult to produce

d) another interrupt may be caused, if the signal is still low before the completion of the last instruction

Answer: d

Explanation: In a level triggered pulse, if the signal does not becomes high before the last instruction of the ISR, then the same interrupt will be caused again, so monitoring of pulse is required for a level triggered pulse.

10. What is the correct order of priority that is set after a controller gets reset?

a) TxD/RxD> T1 > T0 > EX1 > EX0

b) TxD/RxD< T1 < T0 < EX1 < EX0 c) EX0 > T0 > EX1 > T1 >TxD/RxD

d) EX0 < T0 < EX1 < T1 <TxD/RxD

Answer: c Explanation: EX0 > T0 > EX1 > T1 >TxD/RxD. This is the correct order of priority that is set after a controller gets reset.

Microprocessors Questions and Answers – Register Set of 8051

1. Which of the following is an 8-bit register?

a) PSW(Program Status Word)

b) TCON(Timer Control Register)

c) Accumulator

d) all of the mentioned

Answer: d

Explanation: The registers, PSW, TCON and Accumulator are 8-bit registers.

2. Which of the following register can be addressed as byte?

a) P1

b) SCON

c) TMOD

d) TCON

Answer: c

Explanation: The registers, TMOD, SP, TH0, TH1, TL0, TL1 are to be addressed as bytes.

3. Which of the following is bit-addressable register?

a) SBUF

b) PCON

c) TMOD

d) SCON

Answer: d

Explanation: The registers, accumulator, PSW, B, P0, P1, P2, P3, IP, IE, TCON and SCON are all bit-addressable registers.

4. The higher and lower bytes of a 16-bit register DPTR are represented respectively as

a) LDPTR and HDPTR

b) DPTRL and DPTRH

c) DPH and DPL

d) HDP and LDP

Answer: c

Explanation: The registers, DPH and DPL are the higher and lower bytes of a 16-bit register DPTR.

5. The register that is used for accessing external data memory is

a) DPH

b) DPL

c) DPTR

d) NONE

Answer: c

Explanation: The Data pointer(DPTR) is used for accessing external data memory which means that it includes both DPH and DPL.

6. Among the four groups of register banks, the number of groups that can be accessed at a time is

a) 1

b) 2

c) 3

d) all the four

Answer: a

Explanation: At a time, only one of the four register banks can be accessed.

7. The number of 8-bit registers that a register bank contain is

a) 2

b) 4

c) 6

d) 8

Answer: d

Explanation: The 32, 8-bit registers are divided into four groups of 8 registers each, called register banks.

8. If RS1=1, RS0=0, then the register bank selected is

a) register bank 0

b) register bank 1

c) register bank 2

d) register bank 3

Answer: c

Explanation: If RS1=1, RS0=0, then the register bank selected is register bank 2.

9. If RS1=1, RS0=1, then the register bank selected is

a) register bank 0

b) register bank 1

c) register bank 2

d) register bank 3

Answer: d

Explanation: If RS1=1, RS0=1, then the register bank selected is register bank 3. If RS1=0, RS0=0, then selected bank is register bank 0.

10. The PCON register consists of

a) power mode bit

b) power idle bit

c) power ideal bit

d) power down bit and idle bit

Answer: d

Explanation: The power control register, PCON consists of power down bit and idle bit which activate the power down mode and idle mode in 80C51BH.

11. The on-chip oscillator is stopped in

a) power mode

b) power down mode

c) idle mode

d) ideal mode

Answer: b

Explanation: In power down mode, the on-chip oscillator is stopped.

12. In idle mode, the device that is disabled is

a) serial port

b) timer block

c) clock to CPU

d) all of the mentioned

13. The only way to terminate the power down mode is to

a) CLEAR

b) RESET

c) HOLD

d) HLT

14. The idle mode can be terminated by

a) PRESET

b) CLEAR

c) interrupt

d) interrupt or reset

Microprocessors Questions and Answers – Interrupt and Stack of 8051 -1

1. Which of the following is an external interrupt?

a) INT0(active low)

b) INT2(active low)

c) Timer0 interrupt

d) Timer1 interrupt

Answer: a

Explanation: INT0(active low) and INT1(active low) are two external interrupt inputs provided by 8051.

2. The interrupts, INT0(active low) and INT1(active low) are processed internally by flags

a) IE0 and IE1

b) IE0 and IF1

c) IF0 and IE1

d) IF0 and IF1

View Answer

Answer: a

Explanation: The interrupts, INT0(active low) and INT1(active low) are processed internally by the flags IE0 and IE1.

3. The flags IE0 and IE1, are automatically cleared after the control is transferred to respective vector, if the interrupt is

a) level-sensitive

b) edge-sensitive

c) in serial port

d) in parallel port

View Answer

Answer: b

Explanation: If the interrupts are programmed as edge sensitive, the flags IE0 and IE1 are automatically cleared after the control is transferred to respective vector.

4. If the external interrupt sources control the flags IE0 and IE1, then the interrupt programmed is

a) level-sensitive

b) edge-sensitive

c) in serial port

d) in parallel port

View Answer

Answer: a

Explanation: If the interrupts are programmed as level sensitive, then the flags IE0 and IE1 are controlled by external interrupt sources themselves.

5. The pulses at T0 or T1 pin are counted in

a) timer mode

b) counter mode

c) idle mode

d) power down mode

View Answer

Answer: b

Explanation: In counter mode, the pulses are counted at T0 or T1 pin.

6. In timer mode, the oscillator clock is divided by a prescalar

a) (1/8)

b) (1/4)

c) (1/16)

d) (1/32)

View Answer

Answer: d

Explanation: In timer mode, the oscillator clock is divided by a prescalar (1/32) and then given to the timer.

7. The serial port interrupt is generated if

a) RI is set

b) RI and TI are set

c) either RI or TI is set

d) RI and TI are reset

View Answer

Answer: c

Explanation: The serial port interrupt is generated if atleast one of the two bits, RI and TI is set.

8. In serial port interrupt, after the control is transferred to the interrupt service routine, the flag that is cleared is

a) RI

b) TI

c) RI and TI

d) none

Answer: d

Explanation: In serial port interrupt, after the control is transferred to the interrupt service routine, neither of the flags is cleared.

9. The atleast number of machine cycles for which the external interrupts that are programmed level-sensitive should remain high is

a) 1

b) 2

c) 3

d) 0

Answer: b

Explanation: The external interrupts, programmed level-sensitive should remain high for atleast 2 machine cycles.

10. If the external interrupts are programmed edge sensitive, then they should remain high for atleast

a) 0 machine cycle

b) 2 machine cycles

c) 1 machine cycle

d) 3 machine cycles

Answer: c

Explanation: If the external interrupts are programmed edge sensitive, then they should remain high for atleast one machine cycle and low for atleast one machine cycle, for being sensed.

Microprocessors Questions and Answers – Interrupt and Stack of 8051 -2

1. The timer generates an interrupt, if the count value reaches to

a) 00FFH

b) FF00H

c) 0FFFH

d) FFFFH

Answer: d

Explanation: the timer is an up-counter and generates an interrupt when the count has reached FFFFH.

2. The external interrupt that has the lowest priority among the following is

a) TF0

b) TF1

c) IE1

d) NONE

Answer: c

Explanation: The order of given interrupts from high to low priority is TF0, IE1 and TF1.

3. Among the five interrupts generated by 8051, the lowest priority is given to the interrupt

a) IE0

b) TF1

c) TF0

d) RI

Answer: d

Explanation: the interrupt, RI=TI (serial port) is given the lowest priority among all the interrupts.

4. Among the five interrupts generated by 8051, the highest priority is given to the interrupt

a) IE0

b) TF1

c) TF0

d) IE1

Answer: a

Explanation: the interrupt, IE0(External INT0) is given the highest priority among all the interrupts.

5. All the interrupts are enabled using a special function register called

a) interrupt priority register

b) interrupt register

c) interrupt function register

d) interrupt enable register

Answer: d

Explanation: All the interrupts are enabled using a special function register called interrupt enable register (IE) and their priorities are programmed using another special function register called interrupt priority register(IP).

6. The number of bytes stored on the stack during one operation of PUSH or POP is

a) 1

b) 2

c) 3

d) 4

Answer: a

Explanation: As 8051 stack operations are 8-bit wide i.e. in an operation using PUSH or POP instruction, one byte of data is stored on a stack or retrieved from the stack. For implementing 16-bit operations, two 8-bit operations are cascaded.

7. The step involved in PUSH operation is

a) increment stack by 2 and store 8-bit content to address pointed to by SP

b) decrement stack by 1 and store 16-bit content to address pointed to by SP

c) increment stack by 1 and store 8-bit content to address pointed to by SP

d) store 8-bit content to address pointed to by SP and then increment stack by 1

Answer: c

Explanation: The PUSH instruction follows two steps.

1. Increment stack by 1

2. Store 8-bit content of the 8-bit address specified in the instruction to the address pointed to by SP.

8. The step involved in POP operation is

a) decrement stack by 2 and store 8-bit content to address pointed to by SP

b) store 16-bit content to address pointed to by SP and decrement stack by 1

c) decrement stack by 1 and store content of top of stack to address pointed to by SP

d) store content of top of stack to address pointed to by SP and then decrement stack by 1

Answer: d

Explanation: The POP instruction follows two steps.

1. Store the contents of top of stack pointed to by SP register to the 8-bit memory specified in the instruction.

2. Decrement stack by 1.

9. The 8051 stack is

a) auto-decrement during PUSH operations

b) auto-increment during POP operations

c) auto-decrement during POP operations

d) auto-increment during PUSH operations

Answer: d

Explanation: The 8051 stack is opposite to that in 8085 or 8086 i.e. in 8085 it is auto-decrement while in 8051 it is auto-increment during PUSH operations.

10. After reset, the stack pointer(SP) is initialised to the address of

a) internal ROM

b) internal RAM

c) external ROM

d) external RAM

Answer: b

Explanation: The stack pointer(SP) is an 8-bit register and is initialized to internal RAM address 07H after reset.

Microprocessors Questions and Answers – Addressing Modes of 8051

1. Which of the following is not an addressing mode of 8051?

a) register instructions

b) register specific instructions

c) indexed addressing

d) none

Answer: d

Explanation: The six addressing modes of 8051 are

1. Direct addressing

2. Indirect addressing

3. Register instructions

4. Register specific(Register Implicit) instructions

5. Immediate mode

6. Indexed addressing

2. The symbol, ‘addr 16’ represents the 16-bit address which is used by the instructions to specify the

a) destination address of CALL

b) source address of JUMP

c) destination address of call or jump

d) source address of call or jump

Answer: c

Explanation: The symbol, ‘addr 16’ represents the 16-bit destination address which is used by the LCALL or LJMP instruction to specify the call or jump destination address, within 64 Kbytes program memory.

3. The storage of addresses that can be directly accessed is

a) external data RAM

b) internal data ROM

c) internal data RAM and SFRS

d) external data ROM and SFRS

Answer: c

Explanation: Only internal data RAM and SFRS can be directly addressed in direct addressing mode.

4. The address register for storing the 16-bit addresses can only be

a) stack pointer

b) data pointer

c) instruction register

d) accumulator

Answer: b

Explanation: The address register for storing the 16-bit addresses can only be data pointer.

5. The address register for storing the 8-bit addresses can be

a) R0 of selected bank of register

b) R1 of selected bank of register

c) stack pointer

d) all of the mentioned

Answer: d

Explanation: The registers R0 and R1 of the selected bank of registers or stack pointer can be used as address registers for storing the 8-bit addresses.

6. The instruction, ADD A, R7 is an example of

a) register instructions

b) register specific instructions

c) indexed addressing

d) none

Answer: a

Explanation: In register instructions addressing mode, operands are stored in the registers R0-R7 of the selected register bank. One of these registers is specified in the instruction.

7. The addressing mode, in which the instructions has no source and destination operands is

a) register instructions

b) register specific instructions

c) direct addressing

d) indirect addressing

Answer: b

Explanation: In register specific instructions addressing mode, the instructions donot have source and destination operands. Some of the instructions always operate only on a specific register.

8. The instruction, RLA performs

a) rotation of address register to left

b) rotation of accumulator to left

c) rotation of address register to right

d) rotation of accumulator to right

Answer: b

Explanation: The instruction, RLA rotates accumulator left.

9. The instruction, ADD A, #100 performs

a) 100(decimal) is added to contents of address register

b) 100(decimal) is subtracted from accumulator

c) 100(decimal) is added to contents of accumulator

d) none

Answer: c

Explanation: Immediate data 100(decimal) is added to the contents of accumulator.

10. In which of these addressing modes, a constant is specified in the instruction, after the opcode byte?

a) register instructions

b) register specific instructions

c) direct addressing

d) immediate mode

Answer: d

Explanation: In immediate mode, an immediate data, i.e. a constant is specified in the instruction, after the opcode byte.

11. The only memory which can be accessed using indexed addressing mode is

a) RAM

b) ROM

c) main memory

d) program memory

Answer: d

Explanation: Only program memory can be accessed using the indexed addressing mode.

12. The data address of look-up table is found by adding the contents of

a) accumulator with that of program counter

b) accumulator with that of program counter or data pointer

c) data register with that of program counter or accumulator

d) data register with that of program counter or data pointer

Answer: b

Explanation: The look-up table data address is found out by adding the contents of register accumulator with that of the program counter or data pointer.

Microprocessors Questions and Answers – 8051 Instruction Set -1

1. Which of the following is not an instruction of 8051 instructions?

a) arithmetic instructions

b) boolean instructions

c) logical instructions

d) none

Answer: d

Explanation: The 8051 instructions are categorised as

1. Data transfer instructions

2. Arithmetic instructions

3. Logical instructions

4. Boolean instructions

5. Control transfer instructions

2. The operations performed by data transfer instructions are on

a) bit data

b) byte data

c) 16-bit data

d) all of the mentioned

Answer: d

Explanation: The data transfer instructions implement a bit, byte, 16-bit data transfer operations between the SRC(source) and DST(destination) operands.

3. Which of the following is true while executing data transfer instructions?

a) program counter is not accessible

b) restricted bit-transfer operations are allowed

c) both operands can be direct/indirect register operands

d) all of the mentioned

4. The logical instruction that affect the carry flag during its execution is

a) XRL A;

b) ANL A;

c) ORL A;

d) RLC A;

Answer: d

Explanation: The logical instructions that does not affect the carry flag are, ANL, ORL and XRL. The logical instructions that affect the carry flag during its execution are RL, RLC, RRC and RR.

5. The instruction that is used to complement or invert the bit of a bit addressable SFR is

a) CLR C

b) CPL C

c) CPL Bit

d) ANL Bit

Answer: c

Explanation: The instruction, CPL Bit is used to complement or invert the bit of a bit addressable SFR or RAM.

6. The instructions that change the sequence of execution are

a) conditional instructions

b) logical instructions

c) control transfer instructions

d) data transfer instructions

Answer: c

Explanation: The control transfer instructions transfer the control of execution or change the sequence of execution conditionally or unconditionally.

7. The control transfer instructions are divided into

a) explicit and implicit control transfer instructions

b) conditional and unconditional control transfer instructions

c) auto control and self control transfer instructions

d) all of the mentioned

Answer: b

Explanation: The control transfer instructions are divided into conditional and unconditional control transfer instructions.

8. The conditional control transfer instructions check a bit condition which includes any bit of

a) bit addressable RAM

b) bit addressable SFRs

c) content of accumulator

d) all of the mentioned

Answer: d

Explanation: The conditional control transfer instructions check a bit condition which includes any bit of bit addressable RAM or bit addressable SFRs or content of accumulator for transferring the control to the specified jump location.

9. All conditional jumps are

a) absolute jumps

b) long jumps

c) short jumps

d) none

Answer: c

Explanation: All conditional jumps are short jumps.

10. The first byte of a short jump instruction represents

a) opcode byte

b) relative address

c) opcode field

d) none

Answer: a

Explanation: The short jump instruction has two byte instruction. The first byte represents opcode byte and second byte represents an 8-bit relative address.

11. In logical instructions, the immediate data can be an operand for

a) increment operation

b) decrement operation

c) single operand instruction

d) none

Answer: d

Explanation: In logical instructions, the immediate data can’t be an operand for increment/decrement or any other single operand instruction.

Microprocessors Questions and Answers – 8051 Instruction Set -2

1. If the most significant bit of relative address byte is 1, then the short jump instruction is

a) forward jump

b) back jump

c) either forward or back jump

d) none

Answer: b

Explanation: If the most significant bit of relative address byte is 1, then the short jump instruction is back jump, else it is considered as forward jump.

2. The first byte of an absolute jump instruction consists of

a) 3 LSBs of opcode and 5 MSBs of 11-bit address

b) 5 MSBs of opcode and 3 LSBs of 11-bit address

c) 6 MSBs of opcode and 1 LSB of 11-bit address

d) 5 LSBs of opcode and 3 MSBs of 11-bit address

Answer: d

Explanation: The first byte of an absolute jump instruction consists of 5 LSBs of opcode and 3 MSBs of 11-bit address. The next byte carries the least significant 8 bits of the 11-bit address.

3. The third byte of the long jump instruction is

a) opcode

b) 5 LSBs of opcode

c) higher byte of jump location or subroutine

d) lower byte of jump location or subroutine

Answer: c

Explanation: The third byte of the long jump instruction is higher byte of jump location or subroutine.

4. The absolute jump instruction is intended mainly for a jump within a memory space of

a) 2 bytes

b) 2 Kbytes

c) 2 Mbytes

d) none

Answer: b

Explanation: The absolute jump instruction is intended mainly for a jump within a memory space of 2 Kbytes.

5. The LJMP instruction is very useful in programming in the external code memory space of

a) 32 MB

b) 64 MB

c) 32 KB

d) 64 KB

Answer: d

Explanation: The LJMP instruction is very useful in programming in the external code memory space of 64 KB.

6. Which of the following is not an unconditional control transfer instruction?

a) JMP

b) RET

c) JNC

d) CALL

Answer: c

Explanation: The instructions, JMP, RET, RETI, CALL are the unconditional control transfer instructions.

7. The conditional control transfer instructions use

a) status flags

b) bits of bit addressable RAM

c) SFRs termed bit

d) all of the mentioned

Answer: d

Explanation: The conditional control transfer instructions use status flags or bits of bit addressable RAM or SFRs termed bit.

8. Which of the following is not a conditional control transfer instruction?

a) JC

b) JBC

c) JNC

d) NONE

Answer: d

Explanation: The instructions, JC, JBC, JNC, JB and JNB are the conditional control transfer instructions.

9. The mnemonic used to perform a subtraction of source with an 8-bit data and jumps to specified relative address if subtraction is non-zero is

a) DJNZ

b) CJNE

c) JZ

d) JNC

Answer: b

Explanation: The CJNE instruction perform a subtraction of source with an 8-bit data and jumps to specified relative address only if the result of the subtraction is non-zero, else continues to the next instruction.

10. The mnemonic, JNB is used to jump to the specified relative address only if

a) specified bit=1

b) specified bit=0

c) specified bit is non-recursive

d) none

Answer: a

Explanation: The mnemonic, JNB is used to jump to the specified relative address only if specified bit=1, else continues to the next instruction.

11. The type of operand that is not allowed to use in boolean instructions of 8051 is

a) direct register operands

b) indirect register operands

c) immediate bit

d) none

Answer: c

Explanation: In boolean instructions, immediate bit is not allowed as an operand.

12. In boolean instructions, the flag that is the only allowed destination operand for two operand instructions is

a) overflow flag

b) underflow flag

c) auxiliary flag

d) carry flag

Answer: d

Explanation: Carry flag(C) is the only allowed destination operand for two operand instructions in boolean instructions.