SRM UNIVERSITY
Faculty of Engineering and Technology

DEPARTMENT OF EIE

Course Code :15EI201
Course Title :DIGITAL PRINCIPLES AND SYSTEM DESIGN
Year& Semester : II / III
Course duration : ODD semester (June - Nov 2016)
Location :
Faculty Details:

Name of the staff	Section	Office	Office Hours	Mail ID
Mrs.N.Deepa	EIE	IT TECH PARK 14th floor	9.00am to 4.00pm	deepa.n@ktr.srmuniv.ac.in
Mrs.A.Asuntha	EIE	IT TECH PARK 14th floor	9.00am to 4.00pm	asuntha.a@ktr.srmuniv.ac.in

REFERENCE BOOKS

1. Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
2. Floyd, "*Digital Fundamentals*", 8th edition, Pearson Education, 2003.
3. Charles. H, Roth, "*Fundamentals Logic Design*", Jaico Publishing, IV edition, 2002.
4. John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
5. John Wakerly. F, "*Digital Design Principles and Practice*", 3rd edition, Pearson Education, 2002.

Web Resource:

- people.clarkson.edu/~tortmeye/.../Fundamentals%20of%20**Digital**%20**Electronics**
- www.forum.allaboutcircuits.com
- www.daenotes.com

Prerequisite :

NIL

Objective:

1. Simplify the mathematical expressions using Boolean functions and simple problem
2. Implement the combinational logic circuits
3. Design the various synchronous and asynchronous circuits.
4. Understand the various memory devices
5. Apply the circuits in real time application

Tentative test details and portions:

Cycle Test - I:	08.08.16	Unit I
Cycle Test –II:	23.08.16	Unit II & III
Cycle Test - III:	25.09.16	Unit IV & V

Assessment details

Cycle test I	10 Marks
Cycle test I	15 Marks
Cycle test - III	15 Marks
Surprise test	05 Marks
Quiz	05 Marks
TOTAL	50 Marks

Outcomes

Students who have successfully completed this course

Course outcome	Program outcome
Can develop digital circuits design • Sequential circuits and combinational circuits use in IC can be developed • Apply the knowledge of counters and shift registers practically • Introduction to asynchronous sequential circuits and state assignment for complex systems • Study of various memory devices and its applications.	A: The student will have a broad knowledge in Digital circuits. B: The student will have a potential to solve mathematical expressions using Boolean functions and simple problems. C:The student will implement combinational and sequential circuits D: Student will have a ability to design sequential circuits E : The student will have a broad knowledge to various memory devices.

Detailed Session Plan

Day	Name of the topics	Reference
	UNIT I: NUMBER SYSTEM & MINIMIZATION TECHNIQUES	
DAY 1	Review of number system	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.

DAY 2	Types and conversion	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 3	Codes :Weighted binary codes BCD,(8421)2421 Code	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 4	Non weighted code Excess 3 code,	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 5	Gray Codes,Conversion of Binary to gray and Gray to Binary code	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 6	Boolean algebra, Basic laws of Boolean Algebra De– Morgan's Theorem	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 7	Switching functions	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 8	Simplification using K Maps	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 9	Quine McCluskey method	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
	UNIT II: COMBINATIONAL CIRCUITS	
DAY10	Design of logic gates, Design of Combinational circuits	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 11	Half adder, Full Adder, Half subtractor ,Full subtractor	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 12	Parallel binary Adder, Subtractor, Serial Adder, BCD Adder	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.

DAY 13	Comparators , 4-bit magnitude comparator	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 14	Code converters : BCD to binary Converter, Binary to Gray code converters,Gray to Binary Converters	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 15	Encoders, Decoders	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 16	Surprise Test	
DAY 17	Multiplexers	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 18	Demultiplexers	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
	UNIT III: SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUIT	
DAY 19	Flip flops : SR Characteristic table and equation, D Characteristic table and equation	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 20	JK Characteristic table and equation T Characteristic table and equation	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 21	Realization of one flip flop using other flip flops JK,SR,T,D	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 22	Counters Up/Down counters	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 23	Modulo-n counter, Johnson counter	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 24	Shift registers , serial in serial out, Parallel in parallel out	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.

DAY 25	Design of synchronous and Asynchronous sequential circuits	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 26	State diagram, state reduction, state assignment, State minimization	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 27	Excitation table and maps, Circuit implementation	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
	UNIT IV: MEMORY DEVICES AND LOGIC FAMILIES	
DAY 28	Memory Organization, Capacity, Density, Signals Basic Operations, Read, Write, Address, data Signals	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 29	Memory Read, Write Cycle, Synchronous Burst SRAM, Dynamic RAM Burst.	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 30	Distributed Refresh, Types of DRAMs, ROM , Mask ROM	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 31	First In-First Out (FIFO) Memory last in-first out (LIFO) memory	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 32	Classification of memories - ROM RAM PROM – EPROM EEPROM	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 33	Digital logic families Logic and their characteristics TTL ,Tristate gates, ECL, CMOS	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 34	PLA	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY 35	PAL, PLD	Morris Mano M, "*Digital Logic and Computer Design*", 4th edition Prentice Hall of India, 2002.
DAY	Quiz	

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	UNIT V: DIGITAL APPLICATION	
DAY 37	Gate circuits, Game control circuits,	John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
DAY 38	Combinational circuit Odd prime number detector.	John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
DAY 39	Design of Now serving system	John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
DAY 40	Event detector circuit	John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
DAY 41	Fire place control circuits	John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
DAY 42	Seven segment display decoder	John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
DAY 43	Elevator Control System: Elevator State Diagram, State Table, Input and Output Signals, Input Latches .	John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
DAY 44	Traffic Signal Control System: Switching of Traffic Lights, Inputs and Outputs, State Machine	John Yarbrough. M, "*Digital Logic, Application & Design*", 4th edition ,Thomson, 2002.
DAY 45	Revision	