SRMUNIVERSITY
FACULTY OF ENGINEERING AND TECHNOLOGY

SCHOOL OF COMPUTING
DEPARTMENT OF CSE
COURSE PLAN

Course Code : CS0432
Course Title : REAL TIME SYSTEM DESIGN
Semester : VIII
Course Time : Dec–May2013

Day	D	
	Hour	Timing
Monday	1,2	8.45-9.25
Tuesday	3,4,6	10.35-12.15, 2.20-3.10
Wednesday	3,4	10.35-12.15
Thursday	-	
Friday	-	

Location : S.R.M.E.C – Tech Park (8th floor)
Faculty Details

Sec.	Name	Office	Office hour	Mail id
A,B, C,D	C.Santhanakrishnan	TP 703B	8.30-4.00 p.m	santhanakrishnan.c@ktr.srmuniv.ac.in

Required Text Books:

1. LaplantePhilip.A, "*Real-time systems design and analysis: An engineer's handbook*",2nd Edition, PHI.,1994.
2. C.M.Krishna, Kang G.Shin, "*Real-time systems*" – McGraw Hill, 1997.

Web resources

www.eventhelix.com/realtimemantra/basics
www.unix.ecs.umass.edu/~krishna
http://infoweb.vub.ac.be/infoef/ulbarch/
www.augustana.ab.ca/~mohrj/courses/2005.winter/cs380/slides.7e

Prerequisite : NIL

Objectives

1. Gives knowledge of Basics of Real time systems.
2. To understand the concepts of Real time systems and its applications.
3. Real time memory and design considerations.
4. Design of the above components.
5. Integration of Hardware and software in real time applications

Assessment Details

Attendance	:	5 Marks
Cycle Test – I	:	10 Marks
Surprise Test – I	:	5 Marks
Cycle Test – II	:	10 Marks
Model Exam	:	20 Marks

Test Schedule

S.No.	DATE	TEST	TOPICS	DURATION
1	**As per calendar**	**Cycle Test - I**	**Unit I & II**	**2 periods**
2		**Cycle Test - II**	**Unit III & IV**	**2 periods**
3		**Model Exam**	**All 5 units**	**3 Hrs**

Outcomes

Students who have successfully completed this course will have full understanding of the following concepts

Course outcome	Program outcome
To learn The basic of Real time systems. Theconcepts of Real time systems and its applications. Basic Real time systemsfunctions(operations) Real time memory and design considerations. Integration of Hardware and software in real time applications.	An ability to understand the basic functioning of Real time systems. To understand the concepts of Queuing models Reliability, testing and fault tolerance To learn structure of an RTOS. To implement real time kernels To understand various types of memory concepts Real time memory management.

Detailed Session Plan

UNIT-I INTRODUCTION

Basic real time concepts - Introduction, Real-time Versus Conventional Software, Computer Hardware for Monitoring and Control, Software Engineering Issues.

Session No.	Topics to be covered	Time (min)	Ref	Teaching Method	Testing Method
1	Basic real time concepts	50	1	PPT	Group discussion Quiz
2	Real time systemsTypes	50	1,2	PPT	Objective type test Quiz
3	Real-time Versus Conventional Software	50	1	PPT	Quiz
4	Real-time Versus Conventional Software	50	1	PPT	Quiz
5	Computer Hardware for Monitoring	50	1	PPT	Quiz
6	Computer Hardware for Control	50	1	PPT	Quiz Objective type test
7	Software Engineering Issues	50	1,2	PPT	Quiz, Assignment
8	Addressing modes	50	1,2	PPT	Group discussion

9	RISC versus CISC	50	1,2	PPT	Group discussion
UNIT-II DESIGN TECHNIQUES Real time specification and design techniques – structure of an RTOS - real time kernels – Intertask Communication and synchronization.					
10	Real time specification	50	1	PPT	Quiz
11	Real timedesign techniques	50	1	PPT	Quiz Brain storming
12	Process Scheduling	50	1,2	PPT	Quiz Surprise Test
13	Round-Robin Scheduling	50	1,2	PPT	Group discussion Quiz
14	Structure of an RTOS	50	1,2	PPT	Group discussion, Quiz
15	Real time kernels	50	1,2	PPT	Quiz, Assignment
16	Intertask Communication and synchronization.	50	1,2	PPT	Quiz
17	Intertask Communication and synchronization.	50	1,2	PPT	Quiz
18	Buffering	50	1,2	PPT	Quiz
UNIT-III MEMORY MANAGEMENT Real time memory management. System performance analysis and optimization.					
19	Real time memory management.	50	2	BB,PPT	Quiz Group discussion Objective type test
20	Process Stack Management	50	2	BB,PPT	Quiz Group discussion
21	Process Stack Management	50	2	BB,PPT	Quiz
22	Task-Control Block Model	50	1,2	BB,PPT	Quiz Surprise Test
23	Memory Management in the Task-Control-Block Model	50	1,2	BB,PPT	Quiz Group discussion
24	Replacement Algorithms	50	1,2	BB,PPT	Quiz
25	System performance analysis and optimization	50	1,2	BB,PPT	Quiz Group discussion
26	System performance analysis and optimization	50	1,2	BB,PPT	Quiz
27	CASE STUDY**: POSIX(**Portable Operating System Interface for Computer Environments)	50	1	BB,PPT	Quiz Brain storming
UNIT-IV QUEUING MODELS AND FAULT TOLERANT ARCHITECTURES Queuing models – Reliability, testing and fault tolerance, HW/SW faults, diagnosis, functional testing. Fault tolerant architectures: TMR systems - multiprocessing systems.					
28	Queuing models	50	1,2	BB	Group discussion Assignment
29	Application Of Queuing Theory – The M/M/1 Queue	50	1,2	BB	Group discussion Quiz
30	Response time modeling	50	1,2	BB	Group discussion Assignment
31	Reliability, testing	50	1,2	BB	Group discussion Assignment

32	Fault tolerance-HW/SW faults, diagnosis, functional testing.	50	1	BB	Objective type test Quiz Group discussion
33	Fault tolerant architectures	50	1	BB	Quiz Group discussion
34	TMR systems	50	1	BB	Objective type test
35	Multiprocessing systems	50	1	BB	Objective type test
36	Fault-Tolerant Design	50	1,2	BB	Quiz Group discussion
UNIT-V APPLICATIONS Hardware/Software integration, real time applications- case studies					
37	Introduction	50	1,2	BB	Group discussion
38	Hardware integration	50	1,2	BB	Objective type test
39	Software integration	50	1,2	BB	Brain storming
40	Goals of System Integration	50	1,2	BB	Brain storming
41	System Unification	50	2	BB	Surprise test Quiz
42	System Verification	50	2	BB	Assignment
43	Simple Integration Strategy	50	2	BB	Assignment
44	Patching	50	1	BB	Brain storming
45	The Probe Effect	50	1	BB	Brain storming

- BB-Black Board
- PPT-Power Point

Prepared by **Approved by**

C.SANTHANAKRISHNAN **HOD / CSE**