SRM UNIVERSITY
FACULTY OF ENGINEERING AND TECHNOLOGY
SCHOOL OF ELECTRONICS AND ELECTRICAL ENGINEERING

DEPARTMENT OF TCE
COURSE PLAN

Course Code : TE1202
Course Title : Digital Logic Circuits
Class : III Year
Semester : V Semester (Odd Semester2016-17)
Location : S.R.M.E.C – Tech Park

Faculty Details

SL. NO	NAME	OFFICE	OFFICE HOURS	E-MAIL ID
1.	Priyalakshmi.B	Tech Park 1306A	8.30am -5.00pm	Priyalakshmi.b@ktr.srmuniv.ac.in
2	N.SHOWME	Tech Park 13S4	8.30am -5.00pm	Showme.n@ktr.srmuniv.ac.in

TEXT BOOKS

1. Morris Mano.M, "Digital Design", Pearson Education, 2006.
2. Floyd and Jain, "Digital Fundamentals", Pearson Education, 8th edition, 2007.
3. Raj Kamal,"Digital systems-principles and design",Pearson education 2nd edition,2007

REFERENCES

4. John M.Yarbrough,"Digital Logic, Application & Design",Thomson,2002.
5. Charles H. Roth, "Fundamentals of Logic Design", JaicoPublishing,IV edition, 2002.
6. John F.Wakerly, "Digital design - Principles and Practices", Pearson Education, 3rd edition, 2002.

PREREQUISITE

Basic Electronics Engineering

OBJECTIVES

To understand the fundamentals of Combinational circuits and sequential circuits and to address a wide variety of memory devices and PLD's.

ASSESSMENT DETAILS

Cycle test -1	: 10Marks		Surprise test	:	5 Marks
Cycle test- II	: 10Marks		Attendance	:	5 Marks
Model Exam	: 20 Marks				

TEST SCHEDULE

SL.NO	DATE	TEST	TOPICS	DURATION
1		Cycle test- I	Unit1&2	2 HRS
2		Cycle test- II	Unit3&4	2 HRS
3		Model Exam	All 5 units	3 HRS

OUTCOMES

Students who have successfully completed this course will have able to do the following

Course outcome	Program outcome
• To study various number systems and to simplify the mathematical expressions using Boolean functions. • To study the implementation of combinational circuits • To study the design of various synchronous and asynchronous circuits. • To study various memory devices and PLD's.	• To get the knowledge about the basics of digital systems.

DETAILED SESSION PLAN

UNIT I - BOOLEAN ALGEBRA AND LOGIC GATES

Review of number systems and their conversion, Boolean algebra, De-Morgan's theorem, switching functions and simplification using Algebric,K-map &QuineMcCluskeymethod,Canonical and standard forms,SOP's and POS form, Minterm and Maxterm,Binarycodes,Logic Gates.

Session No	Topics to be covered	Reference	Teaching Method	Testing Method
1	Review of number systems and their conversion	1,2	BB	Brainstorming questions
2	Boolean algebra	1,2	BB	Self test questions
3	De-Morgan's theorem	1,2	BB	Asking questions by giving Key terms
4	switching functions and simplification using Algebric,K-map method	1,2	BB	Group discussion
5	QuineMcCluskey method	1,2	BB	Self test questions
6	Canonical and standard forms,SOP's and POS form,	1,2	BB	Comparative study
7	Minterm and Maxterm	1,2	BB	Self test questions
8	Binary codes	1,2	BB	Quiz Self test questions
9	Logic Gates	1,2	BB	Self test questions
UNIT II - COMBINATIONAL LOGIC CIRCUIT Adders, Subtractors,Magnitude Comparators, Code converters, Encoders, Decoders, Multiplexers and De-multiplexers, Design of combinational circuits.				
10	Adders	1,2	BB	Self test questions
11	Subtractors	1,2	BB	Self test questions
12	Magnitude Comparators	1,2	BB	Quiz Self test questions
13	Code converters	1,2	BB	seminar
14	Encoders	1,2	BB	Group discussion
15	Decoders	1,2	BB	Asking questions by giving Key terms
16	Multiplexers	1,2	BB	Brainstorming questions
17	De-multiplexers	1,2	BB	Comparative study

18	Design of combinational circuits.	1,2	BB	Group discussion
UNIT III - SYNCHRONOUS SEQUENTIAL LOGIC CIRCUIT Flip flops – SR, D, JK and T. Analysis of synchronous sequential circuits, Design of synchronous sequential circuits – Counters, state diagram, state reduction, state assignment.				
19	Flip flops – SR,	1,2	BB	Quiz Self test questions
20	Flip flops – D, JK	1,2	BB	Comparative study
21	Flip flops –T	1,2	BB	Brainstorming questions
22	Analysis of synchronous sequential circuits	1,2	BB	Quiz Self test questions
23	Design of synchronous sequential circuits	1,2	BB	Asking questions by giving Key terms
24	Counters	1,2	BB	Quiz Self test questions
25	state diagram	1,2	BB	Quiz Self test questions
26	state reduction	1,2	BB	Quiz Self test questions
27	state assignment.	1,2	BB	Quiz Self test questions
UNIT IV - ASYNCHRONOUS SEQUENTIAL LOGIC CIRCUIT Design of Asynchronous sequential circuits, Analysis of Asynchronous sequential machines, transition table ,Flow table, state assignment, Reduction of state and flow tables, Hazards.				
28	Introduction	1,2	BB	Brainstorming questions
29	Design of Asynchronous sequential circuits	1,2	BB	Quiz Self test questions
30	Analysis of Asynchronous sequential machines	1,2	BB	Quiz Self test questions
31	transition table	1,2	BB	Group discussion
32	Flow table	1,2	BB	Comparative study
33	state assignment	1,2	BB	Self test questions
34	Reduction of state tables	1,2	BB	Asking questions by giving Key terms
35	Reduction of flow tables	1,2	BB	Self test questions
36	Hazards	1,2	BB	Quiz
UNIT V- MEMORY AND PLDS **Memories:**Memory types and terminology –ROM architecture –ROM types– ROM applications-RAM architecture – Static RAM – Dynamic RAM**.** **PLD's*:*** Fundamentals of PLD – SPLDs – PAL – GAL – PLA-CPLD.				
37	**Memories:**Memory types and terminology	1,2	PPT	Quiz Self test questions
38	ROM architecture –ROM types– ROM applications	1,2	BB	Seminar
39	RAM architecture – Static RAM – Dynamic RAM	1,2	BB	Quiz Self test questions
40	**PLD's*:*** Fundamentals of PLD	1,2	PPT	Asking questions by giving Key terms

41	SPLDs	1,2	BB	Brainstorming questions
42	PAL	1,2	BB	Comparative study
43	GAL	1,2	BB	Quiz Self test questions
44	PLA	1,2	BB	Quiz Self test questions
45	CPLD	1,2	PPT	Group Discussion

- BB – Black Board
- PPT– Powerpoint
- Ref – 1,2 indicates the books to be referred