**SRM UNIVERSITY**
**FACULTY OF ENGINEERING AND TECHNOLOGY**
**SCHOOL OF COMPUTING**
**DEPARTMENT OF CSE**
**COURSE PLAN**

Course Code : **CS0252**
Course Title : **MICROPROCESSORS**
Semester : IV
Course Time : Dec 2011– May 2012

| Day | A | | Day | B | |
|---|---|---|---|---|---|
| | Hour | Timing | | Hour | Timing |
| Day1 | 2 | 9.35 – 10.25 | Day1 | 1 | 8.45 – 9.35 |
| Day2 | 2 | 9.35 – 10.25 | Day2 | 7 | 3.10 – 4.00 |
| Day3 | 5 | 1.30 – 2.20 | Day3 | 4 | 11.25-12.15 |
| | Tech Park (606) | | | Tech Park (701) | |

**Faculty Details:**

| Section | Name | Office | Office hour | Mail id |
|---|---|---|---|---|
| A | Mr.S.Saminathan | Tech Park 7Th Floor | Monday to Friday | saminathan.s@ktr.srmuniv.ac.in |
| B | Mrs.S.Krishnaveni | Tech Park 7Th Floor | Monday to Friday | krishnaveni.s@ktr.srmuniv.ac.in |

**Required Text Books**:
**TEXT BOOKS**
1. Barry B.Brey, The Intel Microprocessors 8086/8088, 80, 86, 80286, 80386 80486, Pentium, Pentium Pro Processor, Pentium II, Pentium III, Pentium 4, Architecture, Programming and interfacing, Prentice Hall of India Private Limited, New Delhi, 2003. (UNIT I, II and III)
2. John Peatman, Design with Microcontroller McGraw Hill Publishing Co Ltd, New Delhi. (UNIT IV)
3. Alan Clements, "The principles of computer Hardware", Oxford University Press, 3rd Edition, 2003. (UNIT V)

**REFERENCES**
1. Rajkamal, The concepts and feature of micro controllers 68HC11, 8051 and 8096; S Chand Publishers, New Delhi.
2. Mohamed Rafiquzzaman ,"Microprocessors and Microcomputer Based system design", Universal Booksl,2002.

**Assessment Details**

| | | |
|---|---|---|
| Cycle Test – I | : | 10 Marks |
| Cycle Test – II | : | 10 Marks |
| Surprise Test – I | : | 5 Marks |
| Assignment | : | 5 Marks |
| Model Exam | : | 20 Marks |

**PURPOSE**

To learn the architecture and programming of family of microprocessors and microcontrollers.

**INSTRUCTIONAL OBJECTIVES**

- To introduce the concepts in internal programming model of Intel family of microprocessors.
- To introduce the programming techniques using MASM, DOS and BIOS function calls.
- To introduce the basic architecture of Pentium family of processors.
- To introduce the architecture programming and interfacing of 16 bit microcontrollers.
- To introduce the concepts and architecture of RISC processor and ARM.

**Detailed Session Plan**

**UNIT 1 ADVANCED MICROPROCESSOR ARCHITECTURE 9**

Internal Microprocessor Architecture-Real mode memory addressing – Protected Mode Memory addressing –Memory paging - Data addressing modes – Program memory addressing modes – Stack memory addressing modes – Data movement instructions – Program control instructions- Arithmetic and Logic Instructions.

| Session No. | Topics to be covered | Time (min) | Ref | Teaching Method | Testing Method |
|---|---|---|---|---|---|
| 1 | Internal Microprocessor Architecture | 50 | 1 | BB/PP | Group discussion, Quiz |
| 2 | Real mode memory addressing | 50 | 1 | BB/PP | Quiz |
| 3 | Protected Mode Memory addressing | 50 | 1 | BB/PP | Assignment |
| 4 | Memory paging, Data addressing modes | 50 | 1 | BB/PP | Objective type test |
| 5 | Program memory addressing modes | 50 | 1 | BB/PP | Group discussion, Quiz |
| 6 | Stack memory addressing modes | 50 | 1 | BB/PP | Quiz |
| 7 | Data movement instructions | 50 | 1 | BB/PP | Assignment |
| 8 | Program control instructions | 50 | 1 | BB/PP | Objective type test |
| 9 | Arithmetic and Logic Instructions | 50 | 1 | BB/PP | Group discussion, Quiz |

**UNIT 2 MODULAR PROGRAMMING AND ITS CONCEPTS 9**

Modular programming –Using keyboard and Video display –Data Conversions- Disk files- Interrupt hooks- using assembly languages with C/ C++

| Session No. | Topics to be covered | Time (min) | Ref | Teaching Method | Testing Method |
|---|---|---|---|---|---|
| 10 | Modular programming | 50 | 1 | BB/PP | Group discussion, Quiz |
| 11 | Modular programming | 50 | 1 | BB/PP | Quiz |
| 12 | Using keyboard and Video display | 50 | 1 | BB/PP | Assignment |
| 13 | Using keyboard and Video display | 50 | 1 | BB/PP | Objective type test |
| 14 | Data Conversions | 50 | 1 | BB/PP | Group discussion, Quiz |
| 15 | Disk files | 50 | 1 | BB/PP | Quiz |
| 16 | Interrupt hooks | 50 | 1 | BB/PP | Assignment |
| 17 | Using assembly languages with C/ C++ | 50 | 1 | BB/PP | Objective type test |
| 18 | Using assembly languages with C/ C++ | 50 | 1 | BB/PP | Group discussion, Quiz |

**UNIT 3 PENTIUM PROCESSORS** **9**

Introduction to Pentium Microprocessor – Special Pentium registers- Pentium memory management – New Pentium Instructions –Pentium Processor –Special Pentium pro features – Pentium 4 processor

| Session No. | Topics to be covered | Time (min) | Ref | Teaching Method | Testing Method |
|---|---|---|---|---|---|
| 19 | Introduction to Pentium Microprocessor | 50 | 1 | BB/PP | Group discussion, Quiz |
| 20 | Introduction to Pentium Microprocessor | 50 | 1 | BB/PP | Quiz |
| 21 | Special Pentium registers | 50 | 1 | BB/PP | Assignment |
| 22 | Pentium memory management | 50 | 1 | BB/PP | Objective type test |
| 23 | New Pentium Instructions | 50 | 1 | BB/PP | Group discussion, Quiz |
| 24 | Pentium Processor | 50 | 1 | BB/PP | Quiz |
| 25 | Special Pentium pro features | 50 | 1 | BB/PP | Assignment |
| 26 | Pentium 4 processor | 50 | 1 | BB/PP | Objective type test |
| 27 | Pentium 4 processor | 50 | 1 | BB/PP | Group discussion, Quiz |

**UNIT 4 16-BIT MICRO CONTROLLER** **9**

8096/8097 Architecture-CPU registers –RALU-Internal Program and Data memory Timers-High speed Input and Output –Serial Interface-I/O ports –Interrupts –A/D converter-Watch dog timer –Power down feature –Instruction set- External memory Interfacing –External I/O interfacing.

| Session No. | Topics to be covered | Time (min) | Ref | Teaching Method | Testing Method |
|---|---|---|---|---|---|
| 28 | 8096/8097 Architecture | 50 | 2 | BB/PP | Group discussion, Quiz |
| 29 | CPU registers, RALU | 50 | 2 | BB/PP | Quiz |
| 30 | Internal Program and Data memory Timers | 50 | 2 | BB/PP | Assignment |
| 31 | High speed Input and Output | 50 | 2 | BB/PP | Objective type test |
| 32 | Serial Interface | 50 | 2 | BB/PP | Group discussion, Quiz |
| 33 | I/O ports, Interrupts | 50 | 2 | BB/PP | Quiz |
| 34 | A/D converter, Watch dog timer | 50 | 2 | BB/PP | Assignment |
| 35 | Power down feature, Instruction set | 50 | 2 | BB/PP | Objective type test |
| 36 | External memory Interfacing, External I/O interfacing | 50 | 2 | BB/PP | Group discussion, Quiz |

**UNIT 5 RISC PROCESSORS AND ARM** **9**

The RISC revolution – Characteristics of RISC Architecture – The Berkeley RISC – Register Windows – Windows and parameter passing – Window overflow – RISC architecture and pipelining – Pipeline buBB/PPles – Accessing external memory in RISC systems – Reducing the branch penalties – Branch prediction – The ARM processors – ARM registers – ARM instructions – The ARM built-in shift mechanism – ARM branch instructions – sequence control – Data movement and memory reference instructions.

| Session No. | Topics to be covered | Time (min) | Ref | Teaching Method | Testing Method |
|---|---|---|---|---|---|
| 37 | The RISC revolution | 50 | 3 | BB/PP | Group discussion, Quiz |
| 38 | Characteristics of RISC Architecture | 50 | 3 | BB/PP | Quiz |
| 39 | The Berkeley RISC, Register Windows, Windows and parameter passing, Window overflow | 50 | 3 | BB/PP | Assignment |
| 40 | RISC architecture and pipelining, Pipeline buBB/PPles | 50 | 3 | BB/PP | Objective type test |
| 41 | Accessing external memory in RISC systems | 50 | 3 | BB/PP | Group discussion, Quiz |
| 42 | Reducing the branch penalties, Branch prediction | 50 | 3 | BB/PP | Quiz |
| 43 | The ARM processors, ARM registers | 50 | 3 | BB/PP | Assignment |
| 44 | ARM instructions, The ARM built in shift mechanism | 50 | 3 | BB/PP | Objective type test |
| 45 | ARM branch instructions, sequence control, Data movement and memory reference instructions. | 50 | 3 | BB/PP | Group discussion, Quiz |

**BB – Blackboard**
**PP - Powerpoint**