		L	T	P	C
EC0306	**VLSI DEVICES AND DESIGN**	**2**	**2**	**0**	**3**
	Prerequisite : EC0205 & EC0203				

Course outcomes	Instructional objectives			
	Introduce the technology, design concepts, electrical properties and modeling of Very Large Scale Integrated circuits.	Basics of MOS Circuit Design & modeling	Basics of MOS process Technology	Understand the concepts of modeling a digital system using Hardware Description Language
a) Graduates will demonstrate knowledge of mathematics, science and engineering.	X	X		
b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems	X		X	X
c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data				X
d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.		X	X	X
i) Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues	X		X	
j) Graduate will develop confidence for self education and ability for life-long learning		X		X
k) Graduate will show the ability to participate and try to succeed in competitive examinations	X	X		X

Course designed by		Department of Electronics & Communication Engineering										
1	Program outcome	a	b	c	d	e	f	g	h	i	j	k
		x	x	x	x					x	x	x
2	Category	General (G)	Basic Sciences (B)		Engineering Sciences and Technical Arts(E)			Professional Subjects(P)				
								X				
3	Broad area (for 'P'category)	Communication	Signal Processing		Electronics			VLSI		Embedded		
								X				

4	Staff responsible for preparing the syllabus	Mrs. N. Saraswathi , Dr .J. Selvakumar
5	Date of preparation	December 2013

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Mapping of Program Educational Objectives Vs Program Outcomes

Program Outcomes	Educational Program objectives				
	1. To prepare students to compete for a successful career in their chosen profession through global education standards.	2. To enable the students to aptly apply their acquired knowledge in basic sciences and mathematics in solving engineering problems.	3. To produce skillful graduates to analyze, design and develop a system/component/process for the required needs under the realistic constraints.	4. To train the students to approach ethically any multidisciplinary engineering challenges with economic, environmental and social contexts	5. To create an awareness among the students about the need for life long learning to succeed in their professional career.
a) Graduates will demonstrate knowledge of mathematics, science and engineering.	X	X			
b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems	X	X	X		
c) Graduates will demonstrate the ability to design and conduct experiments, analyze and interpret data.		X	X		
d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications		X	X	X	
k)Graduates will show the ability to participate and try to succeed in competitive examinations	X	X			X

SRM University

Department of Electronics and Communication Engineering

Course Code : EC0306
Course Title : VLSI Devices and Design

INSTRUCTIONAL OBJECTIVE	PROGRAM OUTCOME	EVIDENCE
Introduce the technology, design concepts, electrical properties and modeling of Very Large Scale Integrated circuits	a) Graduates will demonstrate knowledge of mathematics, science and engineering.	Cycle test-II Lesson notes-Session no.3
	b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems	Cycle test-II Lesson notes-Session no.3
	i) Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues	Ability to model & design an IC for an application in a society
	k) Graduates will show the ability to participate and try to succeed in competitive examinations.	Tested with Objective Questions Capable of answering *competitive exams like JTO, GATE, IES etc.
Basics of MOS Circuit Design & modeling	a) Graduates will demonstrate knowledge of mathematics, science and engineering.	surprise test-II
	c) Graduates will demonstrate the ability to design and conduct experiments, analyze and interpret data.	Analysed and performed experiments (no.7,8,9) in VLSI lab
	d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications	Designed and performed experiments in VLSI LAB based on switching level modeling
	k)Graduates will show the ability to participate and try to succeed in competitive examinations.	Tested with Objective Questions Capable of answering *competitive exams like JTO, GATE, IES etc.
Basics of MOS process Technology	b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems	Model exam
	d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications	Analysed and performed experiments in VLSIDesign LAB
	i) Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues	Designed and performed experiments in VLSI Design LAB
Understand the concepts of modeling a digital system using Hardware Description Language	b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems	Cycle test-I & Surprise Test - I Lesson notes-Session no.3
	c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data	Analysed and performed experiments(no.1,2,3,5) in VLSI Design lab
	d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.	Analysed and performed experiments(no.5,6,7,8) in VLSI Design lab

	j) Graduate will develop confidence for self education and ability for life-long learning	Ability to learnt other HDL languages like ActiveHDL, AnalogVHDL, Vera, etc
	k) Graduate will show the ability to participate and try to succeed in competitive examinations	Tested with Objective Questions Capable of answering *competitive exams like JTO, GATE, IES etc.

EC0306P VLSI Devices and Design 3 0 0 3

PURPOSE

To introduce the technology, design concepts, electrical properties and modeling of Very Large Scale Integrated circuits.

INSTRUCTIONAL OBJECTIVES

To learn the basic MOS Circuits
To learn the MOS process technology
To learn the concepts of modeling a digital system using Hardware Description Language

INTRODUCTION TO MOS TECHNOLOGY

An overview of Silicon semiconductor technology- NMOS fabrication. CMOS fabrication: n-well, p-well - Twin tub and SOI Process - Interconnects. Circuit elements: Resistors- Capacitors- Bipolar transistors. Latch up and prevention.

MOS CIRCUIT DESIGN PROCESS

Basic MOS transistors: Symbols - Enhancement mode - Depletion mode transistor operation - Threshold voltage derivation - Body effect - Drain current Vs voltage derivation - Channel length modulation. NMOS and CMOS inverter - Determination of pull up to pull down ratio - Design of logic gates - Stick diagrams.

PRINCIPLES OF VHDL (ELEMENTARY TREATMENT ONLY)

Introduction to VHDL. Language elements: Identifiers - Data objects - Data types - Operators - Behavioral modeling - Dataflow modeling - Structural modeling - Examples - Sub programs and overloading - Package concepts.

VERILOG HDL (ELEMENTARY TREATMENT ONLY)

Hierarchical modeling concepts- Basic concepts: Lexical conventions - Data types - Modules and ports - Gate level modeling - Dataflow modeling - Behavioral modeling - Functions - UDP concepts

CMOS SUBSYSTEM DESIGN

Introduction - Design of Adders: carry look ahead, carry select, carry save, Parity generators. Design of multipliers: Array , Braun array , Baugh - Wooley Array , Wallace tree multiplier.

TEXT BOOKS

(1) Douglas A. Pucknell, "Basic VLSI Systems and Circuits", 3rd edition, Prentice Hall of India, 1993
(2) Samir Palnitkar, "Verilog HDL - Guide to Digital Design and Synthesis", 3rd Edition, Pearson Education, 2003
(3) J. Bhaskar, "VHDL Primer", 1st edition, BSP, 2002

REFERENCE BOOKS

(1) Weste & Eshraghian, "Principles of CMOS VLSI Design", 2nd edition, Addison Wesley, 1993
(2) Fabricious. E, "Introduction to VLSI Design", 1st edition, McGraw Hill, 1990
(3) Roth .C, "Digital Systems Design using VHDL", Thomson Learning, 2000

SRM UNIVERSITY
FACULTY OF ENGINEERING AND TECHNOLOGY

SCHOOL OF ELECTRONICS AND ELECTRICAL ENGINEERING
DEPARTMENT OF ECE
COURSE PLAN

Course Code : EC0306
Course Title : VLSI DEVICES AND DESIGN
Semester : VI
Course Time : Dec-2013 – May-2014
Location : S.R.M.E.C

Day Order	A	B	C	D	E	F	G	H
D1	--	4th hr (11.25am-12.15pm)	6th hr (2.20 – 3.10 pm)	7th hr (8.45 – 9.35 am)	4th hr (11.25am-12.15pm)	--	3rd & 4th hr (10.35am – 11.25pm)	5th & 6th hr (1.30 – 3.10pm)
D2	5th hr (1.30-2.20 pm)	--	--	5th hr (1.30-2.20pm)	4th hr (11.25am – 12.15pm)	6th & 7th hrs (2.20 – 4.00 pm)	7th hr (3.10-4.00pm)	--
D3	--	2nd & 3rd Hrs (9.35 -11.25am)	--	--	2nd hr (9.35-10.25am)	--	4th hr (11.25am – 12.15pm)	2nd Hr (9.35-10.25am)
D4	3rd & 4th hr (10.35am-12.15pm)	--	2nd & 3rd Hrs (9.35– 11.25am)	1st hr (8.45-9.35am)	3rd (10.35-11.25am)	2nd & 4th hrs (10.35am-12.15pm)	--	--
D5	1st hr (8.45am – 9.35am)	10.35-11.25 am	7th hr (3.10 – 4pm)	2nd hr (9.35-10.25am)	--	--	--	7th hr (3.10-4.00pm)

Faculty Details

Sec.	Name	Office	Mail id
A	Dr. J. Selvakumar	TP12S8	selvakumar.j@ktr.srmuniv.ac.in
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D	Mr. S. Nivash	TP1206A	nivash.s@ktr.srmuniv.ac.in
E	Mrs.T.V.Ananthalakshimi	TP1006A	ananthalakshimi.tv@ktr.srmuniv.ac.in
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H	Mrs.B.Sudha	TP101A	sudha.b@ktr,srmuniv.ac.in

Required Text Books:

(1) Douglas A. Pucknell, "Basic VLSI Systems and Circuits", 3rd edition, Prentice Hall of India, 1993
(2) Samir Palnitkar, "Verilog HDL - Guide to Digital Design and Synthesis", 3rd Edition, Pearson Education, 2003
(3) J. Bhaskar, "VHDL Primer", 1st edition, BSP, 2002
(4) J.Bhaskar, "A Verilog HDL Primer", 1st Edition, BSP2008
(5) Weste & Eshraghian, "Principles of CMOS VLSI Design", 2nd edition, Addison Wesley, 1993
(6) Fabricious. E, "Introduction to VLSI Design", 1st edition, McGraw Hill, 1990
(7) Roth .C, "Digital Systems Design using VHDL", Thomson Learning, 2000
(8) Jan M.Rabaey, Anantha Chandrakasan, "Digital Integrated Circuits – A Design Perspective", 2nd Edition, Prentice Hall of India, 2003.

Web Resources :

www.wikipedia.org
www.pa.msu.edu
www.tutorvista.com
www.globalspec.com
www.ee.bilkent.edu.tr

Prerequisite : Knowledge in the course EC0205

Objectives

1. Understand the basic concepts VLSI Technology and Devices.
2. Ambient Knowledge about the popular HDL, namely VHDL & Verilog HDL.
3. Thorough Knowledge of MOS & CMOS fabrication process.
4. Capabilities to design Digital Arithmetic Blocks.

Assessment Details

Cycle Test – I	:	10 Marks
Surprise Test – I	:	7.5 Marks
Cycle Test – II	:	10 Marks
Surprise Test – II	:	7.5 Marks
Model Exam	:	15 Marks

Test Schedule

S.No.	DATE	TEST	TOPICS	DURATION
1	05/02/2013	Cycle Test - I	Session # 1-12	2 Hrs
2	05/03/2014	Cycle Test - II	Session # 13-26	2 Hrs
3	15/4/2014	Model Exam	Session # 1- 48 (Excluding #13 & 38)	3 Hrs

Outcomes

Students who have successfully completed this course

Course outcome	Program outcome
1. Introduce the technology, design concepts, electrical properties and modeling of Very Large Scale Integrated circuits. 2. Basics of MOS Circuit Design & Models 3. Basics of MOS process technology 4. Understand the concepts of modeling a digital system using Hardware Description Language	a) Graduates will demonstrate knowledge of mathematics, science and engineering. b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications. i) Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues j) Graduate will develop confidence for self education and ability for life-long learning k) Graduate will show the ability to participate and try to succeed in competitive examinations

Detailed Session Plan

PRINCIPLES OF VHDL (ELEMENTARY TREATMENT ONLY)
Introduction to VHDL. Language elements: Identifiers - Data objects - Data types - Operators - Behavioral modeling - Dataflow modeling - Structural modeling - Examples - Sub programs and overloading - Package concepts.

Session No.	Topics to be covered	Text Book & Chapter No.	Instructional Objective	Program Outcome
1	Introduction to VHDL – Basic Terminology, Entity Declaration Architecture Body	" A VHDL Primer" by J.Bhaskar, Ch. 1, Pg. 1-28	4. Understand the concepts	d) Graduates will demonstrate the ability to design a system, component or process as per

			of modeling a digital system using Hardware Description Language	needs and specifications.
2	Component Instantiation, concurrent signal assignment, Event scheduling	" A VHDL Primer" by J.Bhaskar, Ch. 6, Pg. 125-136		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
3	Sequential Behavior, Process Statements, Sequential statements	" A VHDL Primer" by J.Bhaskar, Ch. 4, Pg. 70-85		c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data
4	Data Objects, Data Types, Data Operators with an example	" A VHDL Primer" by J.Bhaskar, Ch. 3, Pg. 34-61		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems
5	Introduction to Behavioral Modeling – Inertial Delay, Transport Delay, comparison between above ,Simulation Deltas	" A VHDL Primer" by J.Bhaskar, Ch. 4, Pg. 86-100		c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data
6	Architecture Body, Process Statement, Variable & Signal Assignment statement with an example	" A VHDL Primer" by J.Bhaskar, Ch. 4, Pg. 1-28		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
7	IF, Case, Loop, Next, Assertion and Block statement description with an example, Example program using session 6 & 7 statements	" A VHDL Primer" by J.Bhaskar, Ch. 4, Pg. 70-89		c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data
8	Concurrent Signal Assignment, Sequential Signal Assignment, comparison between the above, Delta Delay and Multiple Drivers, Concurrent Assertion Statement	" A VHDL Primer" by J.Bhaskar, Ch. 1, Pg. 1-28		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems
9	Example programs on Dataflow Modeling, Introduction to Structural Modeling,	" A VHDL Primer" by J.Bhaskar, Ch. 4, Pg. 67-122		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
10	Component Declaration & Instantiation. Example program on structural modeling. Full adder/Multiplexer program in Data, Structural & Behavioral Modeling	" A VHDL Primer" by J.Bhaskar, Ch. 1, Pg. 1-28		c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data
11	Subprogram, Functions, Procedures, Subprogram overloading- Examples	" A VHDL Primer" by J.Bhaskar, Ch. 8, Pg. 163-180		j) Graduate will develop confidence for self education and ability for life-long learning
12	Package Declaration & Body Deferred Constants, Examples based on package concept	" A VHDL Primer" by J.Bhaskar, Ch. 9, Pg. 183-189		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
13	***Surprise Test 1 - Based on session # 1-12. (To be conducted on same day for all classes)***	" A VHDL Primer" by J.Bhaskar		k) Graduate will show the ability to participate and try to succeed in competitive examinations
VERILOG HDL (ELEMENTARY TREATMENT ONLY) **Hierarchical modeling concepts- Basic concepts: Lexical conventions - Data types - Modules and ports - Gate level modeling - Dataflow modeling - Behavioral modeling - Functions - UDP concepts**				
14	Introduction to Verilog HDL, Module Definition, Delay types, Dataflow Styles, Behavioral Style, Structural Style Modeling.	"A Verilog HDL Primer", J.Bhaskar, Ch.2, pg. 7-22	4. Understand the concepts of modeling a digital system using Hardware Description Language	c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data
15	Language Elements- Identifier, Format, Complier Directives Value set, Data Types ,Parameters	"A Verilog HDL Primer", J.Bhaskar, Ch.2, pg. 25,26,27,38-54		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems
16	Introduction to Modules & ports, Hierarchical Modeling-example, Operands & Operator Types	"Verilog HDL - Guide to Digital Design and Synthesis",Palnitkar,		c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data

		Ch.1,pg. 2-14		
17	Introduction to Gate Delays, Built-in Primitive Gates, MIMO Gates, Tristate Gates, Array of Instances, Example program for Gate Level modeling	"A Verilog HDL Primer", J.Bhaskar, Ch.5, pg. 83-95		k) Graduate will show the ability to participate and try to succeed in competitive examinations
18	Introduction to Dataflow Modeling, Continuous Assignment Statement, Net Declaration Assignment	"A Verilog HDL Primer", J.Bhaskar, Ch.6, pg. 112-121		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
19	Introduction to Behavioral Modeling – initial, always statement. Timing Control- Delay & Event, Sequential and Parallel Block statement , Blocking & non-Blocking statement	"A Verilog HDL Primer", J.Bhaskar, Ch.8, pg. 122-138		c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data
20	Continuous Vs Procedural Assignment, Conditional statement, LOOP statement – A Suitable example	"A Verilog HDL Primer", J.Bhaskar, Ch.8, pg. 141-160		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
21	Functions-Definitions, Functional calls, constant Functions, Opening & Closing Files functions, Reading & Writing File Functions	"A Verilog HDL Primer", J.Bhaskar, Ch.10, pg. 204-219		j) Graduate will develop confidence for self education and ability for life-long learning
22	UDP Concept-Definition, Combinational UDP, Sequential UDP, Example	"A Verilog HDL Primer", J.Bhaskar, Ch.6, pg. 103-110		j) Graduate will develop confidence for self education and ability for life-long learning
INTRODUCTION TO MOS TECHNOLOGY **An overview of Silicon semiconductor technology- NMOS fabrication. CMOS fabrication: n-well, p-well - Twin tub and SOI Process - Interconnects. Circuit elements: Resistors- Capacitors- Bipolar transistors. Latch up and prevention.**				
23	Issues in Digital IC Design- Introduction to Manufacturing process	"Principle of CMOS VLSI Design", Neil Weste, Ch. 3, Pg.109	1. Introduce the technology, design concepts, electrical properties and modeling of Very Large Scale Integrated circuits. 3. Basics of MOS process technology	a) Graduates will demonstrate knowledge of mathematics, science and engineering.
24	NMOS fabrication process flowchart & components	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch. 2, pg.55		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems
25	Introduction to CMOS fabrication process, N-well fabrication process description	"Principle of CMOS VLSI Design", Neil Weste, Ch. 3, Pg.117.		a) Graduates will demonstrate knowledge of mathematics, science and engineering.
26	Introduction to P-well fabrication process and brief explanation on p-well process	"Principle of CMOS VLSI Design", Neil Weste, Ch. 3, Pg.123		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems
27	Detailed flow description of Twin-tub & SOI fabrication process. Introduction to Interconnect parameter – capacitance, Resistance, Inductance	"Principle of CMOS VLSI Design", Neil Weste, Ch. 3, Pg.123		i) Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues
28	Resistor & Capacitor fabrication steps in detail.	"Principle of CMOS VLSI Design", Neil Weste, Ch. 3, Pg.134		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems
29	NPN/PNP BJT fabrication process-flowchart & description, Latch up definition & description on its prevention methods	"Principle of CMOS VLSI Design", Neil Weste, Ch. 3, Pg.138		k) Graduate will show the ability to participate and try to succeed in competitive examinations
MOS CIRCUIT DESIGN PROCESS **Basic MOS transistors: Symbols - Enhancement mode - Depletion mode transistor operation - Threshold voltage derivation - Body effect - Drain current Vs Voltage derivation - Channel length modulation. NMOS and CMOS inverter - Determination of pull up to pull down ratio - Design of logic gates - Stick diagrams.**				
30	Basic MOS transistor symbols & operation in enhancement, depletion mode operation	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch.1 , pg.1-9		a) Graduates will demonstrate knowledge of mathematics, science and engineering..
31	MOS transistor under Static condition, MOS Threshold voltage derivation, Introduction to sub threshold conduction, velocity saturation	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch.2 ,	1. Introduce the	a) Graduates will demonstrate knowledge of mathematics, science and engineering.

		pg.25-50	technology, design concepts, electrical properties and modeling of Very Large Scale Integrated circuits. 2. Basics of MOS Circuit Design & Models	
32	Body Effect- Definition & Description, Hot carrier effects, Drain current Derivation for a MOS transistor in resistive, saturation & non-saturation regions	"Principle of CMOS VLSI Design", Neil Weste, Ch. 2, Pg.46		i) Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues
33	MOS transistor drain current Vs Voltage Derivation –Description & Derivation	"Principle of CMOS VLSI Design", Neil Weste, Ch. 2, Pg.48		c) Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data
34	Introduction to static CMOS Inverter – switching threshold, Noise Margins, robustness	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch.2 , pg.34-54		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
35	Derivation of a pull-down to pull up ratio for a NMOS & CMOS transistor	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch.2 , pg.34-54		a) Graduates will demonstrate knowledge of mathematics, science and engineering.
36	Design of Logic gates- 2/3/4 input NAND, NOR, AND, OR, EXOR. Introduction to logic styles such as Static CMOS, Dynamic CMOS.	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch.2 , pg.34-54		k) Graduate will show the ability to participate and try to succeed in competitive examinations
37	Stick Diagram-Introduction, Notation, Rules. Stick diagram for 2 input NAND, NOR, AND, OR and Boolean function.	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch.3, pg.56-85		i) Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues
38	Layout Diagram-Introduction, Notation, Rules. Stick diagram for 2 input NAND, NOR, AND, OR and Boolean function.	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch.3, pg.56-85		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
39	***Surprise Test 2 - Based on session # 30-38 (To be conducted on same day for all classes)***	"Basic VLSI Systems & Circuits" Douglas Pucknell, Ch.1,2,3		k) Graduate will show the ability to participate and try to succeed in competitive examinations
CMOS SUBSYSTEM DESIGN **Introduction - Design of Adders: carry look ahead, carry select, carry save, Parity generators. Design of multipliers: Array, Braun array , Baugh - Wooley Array , Wallace tree multiplier.**				
40	Introduction to Arithmetic Building Blocks- The Binary adder- Ripple Carry Adder- Description, Propagation Delay derivation	"Digital Integrated circuits", John Rabaey, Ch.11, pg.559	2.Basics of MOS Circuit Design & modeling	b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems k) Graduate will show the ability to participate and try to succeed in competitive examinations
41	Carry-Look ahead Adder-Conceptual & Schematic Diagram, carryout equation derivation	"Digital Integrated circuits", John Rabaey, Ch.11, pg.578		a) Graduates will demonstrate knowledge of mathematics, science and engineering
42	Carry-Save Adder- Conceptual & Schematic Diagram, carryout equation derivation	"Digital Integrated circuits", John Rabaey, Ch.11, pg.559		a) Graduates will demonstrate knowledge of mathematics, science and engineering
43	Introduction to CMOS based Parity generation design, Conceptual diagram & Description, Advantages of CMOS Implementation	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch. 6, pg.151		d) Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
44	The Multiplier- Definitions, Partial-Product Generation, Partial –Product Accumulation, Brief description on array multiplier	"Digital Integrated circuits", John Rabaey, Ch.11, pg.588		a) Graduates will demonstrate knowledge of mathematics, science and engineering.
45	Braun Array Multiplier- Architecture Description, PPG Unit, Delay equations & advantages	"Basic VLSI Systems & Circuits" Douglas A Pucknell, Ch.8 , pg.220-232		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems
46	Baugh Wooley Multiplier- Architecture Description, PPG Unit, Delay equations & advantages	"Basic VLSI Systems & Circuits" Douglas A. Pucknell, Ch.8 , pg.220-		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems

		232		
47	Wallace Tree Multiplier- Architecture Description, PPG Unit, Delay equations & advantages	"Digital Integrated circuits", John Rabaey, Ch.11, pg.594		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems
48	Booth Array Multiplier- Architecture Description, PPG Unit, Delay equations & advantages	"Basic VLSI Systems & Circuits" Douglas A. Pucknell, Ch.8 , pg.220-232		b) Graduates will demonstrate the ability to identify, formulate and solve engineering problems