



Course Handout

SRM University
 Faculty of Engineering and Technology
 Department of Electronics and Communication Engineering
EC0324 VLSI Design Laboratory
Sixth Semester, 2015 (even semester)

Course (catalog) description

The course explores the design aspects of various combinational circuits, counters, shift registers, multipliers, ALU, RAM and FSM. The experiments are related with the design of digital circuits and simulation using Modelsim, Xilinx and Questa software tool and verify the waveforms. The students will get a wide knowledge to use various VLSI simulation tools.

Compulsory/Elective course: Compulsory

Credit hours: 2 credits

Laboratory

VLSI Design Lab- TP12L4, VLSI Simulation Lab- TP11L4

Course coordinator(s)

Mrs.V.Sarada, A.P (Sr.), Department of ECE

Instructor(s)

Name of the instructor	Class handling	Office location	Office phone	Email (domain: @ktr.srmuniv.ac.in)
Mrs. Sabitha Gauni	VI SEM G1 Batch 1	TP9S4	2055	Sabitha.g
Mrs. A. Maria Jossy	VI SEM G1 Batch 2	TP12S5	2087	Mariajossy.a
Mr. R. Prithviraj	VI SEM G1 Batch 3	TP10S6	7960	Prithviraj.r
Mrs. V.Sarada	VI SEM G1 Batch 4	TP12S5	2087	Sarada.v
Mrs. E. Chitra	VI SEM G2 Batch 1	TP12S3	2087	Chitra.e
Mrs. N. Saraswathi	VI SEM G2 Batch 2	TP10S8	2085	Saraswathy.n
Mrs. K. Suganthi	VI SEM G2 Batch 3	TP10S7	2085	Suganthi.k
Mrs.Dr. A. Ruhan Bevi	VI SEM G2 Batch 4	TP12S4	2087	Ruhan.b

Prerequisite: EC0205 Digital Systems**Text book(s) and/or required materials**

1. J. Bhaskar, "VHDL Primer", 1st edition, BSP
2. Samir Palnitkar, "Verilog HDL - Guide to Digital Design and Synthesis", 3rd Edition, Pearson Education, 2003
3. Lab Manual

Computer usage

1. Modelsim 5.7
2. Xilinx ISE 7.1
3. QuestaSim

Class / Lab schedule: one 150 minutes lab session per week, for 14-15 weeks

Section	Venue	Scheduled
G1 Batch 1	TP12L4- VLSI Design Lab	Day 1-5,6,7 and Day 4-2,3,4
G1 Batch 2	TP11L4- VLSI Simulation Lab	Day 4-5,6,7 and Day 1-2,3,4
G1 Batch 3	TP11L4- VLSI Simulation Lab	Day 3-5,6,7 and Day 2-2,3,4
G1 Batch 4	TP12L4- VLSI Design Lab	Day 3-5,6,7 and Day2-2,3,4
G2 Batch 1	TP11L4- VLSI Simulation Lab	Day 4-5,6,7 and Day 1-2,3,4
G2 Batch 2	TP12L4- VLSI Design Lab	Day 4-5,6,7 and Day 1-2,3,4
G2 Batch 3	TP11L4- VLSI Simulation Lab	Day 2-5,6,7 and Day 3-2,3,4
G2 Batch 4	TP12L4- VLSI Design Lab	Day 2-5,6,7 and Day 3-2,3,4

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area: Communication | Signal Processing | Electronics | **VLSI** | Embedded

Course objectives

The objectives of this course is to	Correlates to Program Objective
To design and simulate the various digital circuits	(3), (4)

Course Learning Outcome

This course provides the design of various digital circuits using different VLSI simulation software tools like Modelsim, Xilinx and Questa. The outcome of this course to learn VHDL and Verilog language and also learn the usage of different tools.	Correlates to program outcome		
	H	M	L
1. To design and simulate list of combinational and sequential digital circuits using Modelsim & Xilinx –VHDL language	d,f	c	b,k
2. To design and simulate the brawn array multiplier and ALU using Modelsim and Xilinx-Verilog language	d,f		
3. To design RAM and FSM using Questa software	f		
4. Acquire teamwork skills for working effectively in groups	e		

H: high correlation, M: medium correlation, L: low correlation

Course Topics

No.	Lab Experiments	Sessions
<i>I. Design and simulate using Modelsim/Xilinx-VHDL Language</i>		
1	Design of logic gates	1
2	Design of 4 bit Adders cum subtractors	1
3	Design of 8x1 Multiplexer using 4x1 and 2x1 MUX	1
4	Design of 4x2 priority encoder using behavioral model	1
5	Design of flip flop	1
6	Design of SISO and PIPO using behavioral and structural model	1
7	Design of up down counter and decade counter	1
8	Design of brawn array multiplier using structural model	1
9	Design of ALU using behavioral model	1
<i>II. Design and simulate using Modelsim/Xilinx-Verilog</i>		
10	Design of 4 bit Adders cum subtractors	1
11	Design of SISO and PIPO using behavioral and structural model	1
<i>III. Design and simulate using Questa</i>		
12	Design of RAM	1
13	Design of FSM	2
Total number of sessions		14

Evaluation methods

Attendance	-	5%
Pre-lab questions	-	10%
In-lab experiment	-	20%
Post-lab questions	-	10%
Record	-	10%
Model exam	-	20%
End semester exam	-	25%
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Total	-	100%

EC0324 Laboratory Policies and Report Format

Reports are due at the beginning of the lab period. The reports are intended to be a complete documentation of the work done in preparation for and during the lab. The report should be complete so that someone else familiar with digital design could use it to verify your work. The prelab and postlab report format is as follows:

1. A neat thorough pre-lab must be presented to your Staff In-charge at the beginning of your scheduled lab period. Lab reports should be submitted on A4 paper. Your report is a professional presentation of your work in the lab. Neatness, organization, and completeness will be rewarded. Points will be deducted for any part that is not clear.

2. In this laboratory students will work in teams of three. However, the lab reports will be written individually. Please use the following format for your lab reports.

a. Cover Page: Include your name, Subject Code, Section No., Experiment No. and Date.

b. Objectives: Enumerate 3 or 4 of the topics that you think the lab will teach you. **DO NOT REPEAT** the wording in the lab manual procedures. There should be one or two sentences per objective. Remember, you should write about what you will learn, not what you will do.

c. Design and simulation: This part contains all the steps required to arrive at your final stage. This should include all input and output waveforms, explanations, etc.

d. This section should also include a clear and error free program description of your design process. Simply including a circuit schematic is not sufficient.

e. Questions: Specific questions (Prelab and Postlab) asked in the lab should be answered here. Retype the questions presented in the lab and then formally answer them.

3. Your work must be original and prepared independently. However, if you need any guidance or have any questions or problems, please do not hesitate to approach your staff in-charge during office hours. Copying any pre-lab /post-lab will result in a grade of 0. The incident will be formally reported to the University and the students should follow the dress code in the Lab session.

4. Each laboratory exercise (simulation results) must be completed and demonstrated to your Staff In-charge in order to receive working design model credit. This is the procedure to follow:

a. Design model works: If the design model works during the lab period (3 hours), call your staff in-charge and he/she will sign and date it. This is the end of this lab, and you will get a complete grade for this portion of the lab.

b. Design model does not work: If the Design model does not work, you must make use of the open times for the lab room to complete your experiment. When your design model is ready, contact your staff in-charge to set up a time when the two of you can meet to check your simulation.

5. Attendance at your regularly scheduled lab period is required. An unexpected absence will result in loss of credit for your lab. If for valid reason a student misses a lab, or makes a reasonable request in advance of the class meeting, it is permissible for the student to do the lab in a different section later in the week if approved by the staff in-charge of both the sections. Habitually late students (i.e., students late more than 15 minutes more than once) will receive 10 point reductions in their grades for each occurrence following the first.

6. Final grade in this course will be based on laboratory assignments. All labs have an equal weight in the final grade. Grading will be based on pre-lab work, laboratory reports, post-lab and in-lab performance (i.e., completing lab, answering laboratory related questions, etc.). The Staff In-charge will ask pertinent questions to individual members of a team at random. Labs will be graded as per the following grading policy:

Pre-Lab Work	10 Marks
In-Lab Performance	20 Marks
Post Lab Work	10 Marks
Laboratory Report	10 Marks

7. Reports Due Dates: Reports are due one week after completion of the corresponding lab.

8. Systems of Tests: Regular laboratory class work over the full semester will carry a weight age of 75%. The remaining 25% weightage will be given by conducting an end semester practical examination for every individual student if possible or by conducting a 1 to 1 ½ hours duration common written test for all students, based on all the experiment carried out in the semester.

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Prepared by: Mrs.V.Sarada, A.P (Sr.), Department of ECE

Dated: 2nd January 2015 **Revision No.:** 05 **Date of revision:** NA
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Addendum

ABET Outcomes expected of graduates of B.Tech / ECE / program by the time that they graduate:

- a. Graduates will demonstrate knowledge of mathematics, science and engineering.
- b. Graduates will demonstrate the ability to identify, formulate and solve engineering problems.
- c. Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data.
- d. Graduates will demonstrate the ability to design a system, component or process as per needs and specifications.
- e. Graduates will demonstrate the ability to visualize and work on laboratory and multi-disciplinary tasks.
- f. Graduate will demonstrate the skills to use modern engineering tools, software's and equipment to analyze problems.
- g. Graduates will demonstrate the knowledge of professional and ethical responsibilities.
- h. Graduate will be able to communicate effectively in both verbal and written form.
- i. Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues.
- j. Graduate will develop confidence for self education and ability for life-long learning.
- k. Graduate will show the ability to participate and try to succeed in competitive examinations.

Program Educational Objectives

1. To prepare students to compete for a successful career in Electronics and Communication Engineering profession through global education standards.
2. To enable the students to aptly apply their acquired knowledge in basic sciences and mathematics in solving Electronics and Communication Engineering problems.
3. To produce skillful graduates to analyze, design and develop a system/component/ process for the required needs under the realistic constraints.
4. To train the students to approach ethically any multidisciplinary engineering challenges with economic, environmental and social contexts
5. To create awareness among the students about the need for lifelong learning to succeed in their professional career as Electronics and Communication Engineers.