Academic Course Description

SRM University
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

EM2002 Microprocessors and Microcontrollers

First Semester, 2014-15 (ODD semester)

Course (catalog) description

This course enables the students to know the strong fundamentals of advanced processor such as Pentium, ARM, also enable the students to learn the programming concepts in Embedded C and Embedded OS (ESOS). A strong foundation on NUVOTON ARM Processor & programming is also provided.

Compulsory/Elective course: Compulsory for ECE students

Credit hours: 3 credits

Course coordinator(s)

Dr. J Selvakumar, Assitant Professor (S.G), Department of ECE.

Instructor

Name of the instructor	Office location	Office phone	Email	Consultations
Dr. J. Selvakumar	TP12S8		selvakumar.j@ktr.srmuniv.ac.in	

Relationship to other courses

Pre-requisites : EC0309

Assumed knowledge : Fundamentals of 8086 Microprocessors and 8051 Microcontrollers

Following courses : NIL

References

1. Daniel Tabak, “Advanced Microprocessors-SIE”, Tata McGraw Hill. Inc., 2011.
2. James L. Antonakos, “The Pentium Microprocessor”, Pearson Education, 2002.
3. Steave Furber, “ARM System - On - Chip architecture”, Addison Wesley, 2000.
4. Andrew N. Sloss, Dominic Symes, Chris Wright and John Rayfield, “ARM System Developer's Guide, Designing and Optimizing System Software”, Elsevier, 2004.
5. David Seal, “ARM Architecture Reference Manual”, Pearson Education, 2007.
6. Michael J. Pont, “Embedded C”, Addison Wesley, 2002.

7. Jivan S. Parab, Vinod G. Shelake, Rajanish K. Kamot, and Gourish M. Naik, "Exploring C for Microcontrollers- A Hands on Approach", Springer, 2007.
8. www.nuvoton.com.

Class schedule: Four 50 minutes lecture sessions per week.

Section	Schedule
A	Day1: 4th Hr ;Day2: 3rd ; Day3: 6th ; Day4: 1st .

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area: Communication | Signal Processing | Electronics | VLSI | **Embedded**

Test Schedule

S. No.	Test	Portions	Date
1	Cycle Test		4th week of Aug'14
2	Term paper		1st week of Sep'14
3	Model Test		4th week of Oct'14

Daily Teaching plan

Session No.	Topics to be covered	Time (min)	Study Material Reference/Chapter
1	ARM: The ARM architecture -	50	Ref.[4], Chapter 2
2	ARM organization and implementation -	50	Ref.[4], Chapter 3
3	The ARM instruction set – Data Transfer instruction set, Branch Instruction set	50	Ref.[4], Chapter 4
4	The ARM instruction set – Arithmetic & Logical Instruction set, Coprocessor Control Instrcution	50	Ref.[4], Chapter 5
5	The thumb instruction set – such as DATA transfer, Arithmetic ARM CPU cores. (Ref. 3 and 4)	50	Ref.[4], Chapter 8
6	Basic ARM Assembly language program: 7-segment LED display using ARM Nuvoton Cortec M0 processor instructions	50	Ref.[4], Chapter 9
7	Introduction to ARM CPU cores such as ARM710,720,740 cores basic architectures description	50	Ref.[3], Chapter 6

8	Introduction to ARM CPU cores such as ARM710,720,740 cores basic Cache memory design description	50	Ref.[3], Chapter 6
9	Introduction to ARM CPU cores such as StrongARM, ARM820 cores basic architecture description	50	Ref.[3], Chapter 6
10	Introduction to ARM CPU cores such as StrongARM, ARM820 cores basic Cache memory design description	50	Ref.[3], Chapter 7
11	The AMULET asynchronous ARM Processors – Introduction & Architecture brief.	50	Ref.[3], Chapter 8
12	Embedded Operating Systems –Introduction and the feature of ESOS in real-time systems.	50	Ref.[3], Chapter 8
13	Embedded Operating Systems : Principle Components	50	Ref.[3], Chapter 8
14	Embedded Operating Systems – Application case study	50	Ref.[3], Chapter 8
15	**VLSI Ruby II** Advanced communication processor-Introduction & architectural analysis.	50	Ref.[3], Chapter 9
16	Introduction to CORTEX-M0 Processor Architecture & its instruction set in details.	50	Ref.[8]
17	Supporting tool sets for Nuvoton Cortex M0 Processor & its addressing modes	50	Ref.[8]
18	Programming the Nuvoton Cortex M0 target board	50	Ref.[8]
19	Basics of sEOS – Timer Design consideration using sEOS-Multistate system design.	50	Ref.[5], Chapter 10
20	Implementation of Traffic light sequencing using onchip UART for RS-232 communication	50	Ref.[5], Chapter 10
21	Memory requirements for real-time systems. Case study specifications	50	Ref.[5], Chapter 10
22	Intruder alarm systems- Brief study with programming	50	Ref.[7], Chapter 4
23	HyperTerminal based control-packet based control for LED interfacing	50	Ref.[7], Chapter 4
24	Security challenges and authentication process for Embedded Systems.	50	Ref.[7], Chapter 5
25	Instruction set - Data formats - Instruction formats - Addressing modes	50	Ref.[5], Chapter 10
25	Memory Hierarchy - Register File - Cache	50	Ref.[1], Chapter 4
26	Virtual memory and paging - Segmentation	50	Ref.[1], Chapter 4
27	Pipelining- The instruction pipeline - pipeline hazards	50	Ref.[1], Chapter 4
28	Instruction level parallelism – Reduced Instruction set	50	Ref.[1], Chapter 4
29	Computer principles - RISC versus CISC	50	Ref.[1], Chapter 4
30	RISC properties – RISC evaluation	50	Ref.[1], Chapter 4
31	On-chip register files versus cache evaluation.	50	Ref.[1], Chapter 5
32	Simple Problem on cache capacity and paging technique	50	Ref.[1], Chapter 5

33	The software model - functional description	50	Ref.[1], Chapter 4
34	CPU pin descriptions - RISC concepts	50	Ref.[1], Chapter 4
35	Basic Bus operations - Super scalar architecture - pipelining - Branch Prediction	50	Ref.[2], Chapter 4
36	Branch prediction - The instruction and caches - Floating Point unit.	50	Ref.[2], Chapter 5
37	Protected mode operation - Segmentation - paging	50	Ref.[2], Chapter 5
38	Protection - multitasking - Exception and interrupts	50	Ref.[2], Chapter 5
39	Input/Output - Virtual 8086 model - Interrupt processing	50	Ref.[2], Chapter 5
40	Instruction types - Addressing modes - Processor flags	50	Ref.[2], Chapter 5
41	Instruction set - Basic programming the Pentium Processor	50	Ref.[2], Chapter 6
42	Virtual memory and paging - Segmentation	50	Ref.[2], Chapter 6
43	Exception and interrupts – Input/ Output - Virtual 8086 model Set .	50	Ref.[2], Chapter 6
44	Interrupt processing - Instruction types - Addressing modes - Processor flags -	50	Ref.[2], Chapter 6
45	Instruction set and basic programming of the Pentium Processor	50	Ref.[2], Chapter 6

Evaluation methods

Attendance	-	5%
Cycle Test	-	25%
Term paper	-	10%
Model Test	-	25%
Surprise Test	-	5%
Final exam	-	30%

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Prepared by: Dr. J.Selvakumar, Assistant Professor (S.G), Department of ECE

Dated: 25th June 2014 **Revision No.:** 00 **Date of revision:** NA

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