M. Tech (Full Time) – VLSI DESIGN (FULL TIME)

Curriculum and Syllabus

(2018-19 and onwards)

FACULTY OF ENGINEERING AND TECHNOLOGY
SRM Institute of Science and Technology
SRM Nagar, Kattankulathur – 603 203
M. Tech. VLSI DESIGN (FULL TIME)
Curriculum and Syllabus
Batch 2018-19 and onwards

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Category</th>
<th>No. of Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I Semester</td>
<td>II Semester</td>
</tr>
<tr>
<td>1</td>
<td>Core Courses</td>
<td>12</td>
</tr>
<tr>
<td>2</td>
<td>Program Elective Courses</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>Supportive Courses</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>Interdisciplinary</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>Career Advancement Courses</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>Seminar</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>Project Work</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Credits per semester</td>
<td>19</td>
</tr>
</tbody>
</table>

Total Credits 74

* Main Project-Phase I
** Main Project-Phase II

Core courses

<table>
<thead>
<tr>
<th>Course code</th>
<th>Course Title</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>VL2001</td>
<td>Digital Systems Design using Verilog</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>VL2002</td>
<td>MOS Device Modeling</td>
<td>4</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>VL2003</td>
<td>Digital Signal processing structures for VLSI</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>VL2004</td>
<td>CMOS Analog VLSI</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>VL2005</td>
<td>VLSI Design Automation</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VL2006</td>
<td>VLSI Technology</td>
<td>4</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>VL2007</td>
<td>Testing of VLSI Circuits</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VL2008</td>
<td>Reconfigurable Architectures for VLSI</td>
<td>4</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>

Program Electives

<table>
<thead>
<tr>
<th>Course code</th>
<th>Course Title</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>VL2101</td>
<td>Digital System Synthesis and Verification</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2102</td>
<td>Nano Electronics</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2103</td>
<td>Low Power VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2104</td>
<td>Neural Networks for VLSI</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2105</td>
<td>VLSI Digital Signal Processing systems</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2106</td>
<td>ASIC Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2107</td>
<td>CMOS Mixed signal Circuit Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2108</td>
<td>DSP Architectures and Applications</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2109</td>
<td>Design of Semiconductor Memories</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2110</td>
<td>System-on-Chip design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2111</td>
<td>Genetic Algorithms and their Applications in VLSI</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>Course code</td>
<td>Course Title</td>
<td>L</td>
<td>T</td>
<td>P</td>
<td>C</td>
</tr>
<tr>
<td>------------</td>
<td>--------------------------------------------------</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>VL2112</td>
<td>Reliability Engineering</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2113</td>
<td>Fundamentals and Applications of MEMS</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2114</td>
<td>RF VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2115</td>
<td>High Speed VLSI</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2116</td>
<td>Magneto-electronics</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2117</td>
<td>VLSI interconnects and its design techniques</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2118</td>
<td>Digital HDL Design and Verification</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2119*</td>
<td>Computational Aspects of VLSI</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2120*</td>
<td>Computational Intelligence</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2121*</td>
<td>Chromatic Graph Theory</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2122*</td>
<td>Solar Cells and Thin Film Technologies</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2123*</td>
<td>Next Generation Photovoltaics</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2124*</td>
<td>Quantum Computation and Information</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2125*</td>
<td>Superconductivity: Theory and its Effects</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>VL2126*</td>
<td>Multicore Processors and Scheduling Algorithms</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

* Ph.D coursework subjects

**Supportive Courses**

<table>
<thead>
<tr>
<th>Course code</th>
<th>Course Title</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA2010</td>
<td>Graph theory and optimization techniques</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>EM2101</td>
<td>Computer Architecture</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>CO2105</td>
<td>Electromagnetic Interference and Compatibility in System Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

**Other Courses**

<table>
<thead>
<tr>
<th>Course code</th>
<th>Course Title</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAC2001</td>
<td>Career Advancement Course for Engineers –I</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>CAC2002</td>
<td>Career Advancement Course for Engineers –II</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>CAC2003</td>
<td>Career Advancement Course for Engineers –III</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>VL2047</td>
<td>Seminar</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>VL2049</td>
<td>Project Work – Phase - I</td>
<td>0</td>
<td>0</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>VL2050</td>
<td>Project Work – Phase – II</td>
<td>0</td>
<td>0</td>
<td>32</td>
<td>16</td>
</tr>
</tbody>
</table>
HDL programming being fundamental for VLSI design this course concentrates on delivering the necessary concepts and features.

**INSTRUCTIONAL OBJECTIVES**

1. The student will learn the different abstract levels in Verilog for modeling digital circuits.
2. The student will learn the basic CMOS circuit, characteristics and performance.
3. The student will learn the designing of combinational and sequential circuits in CMOS.

**UNIT I - BASIC CONCEPTS - VERILOG**

Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters, Operands, Operators, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Switch level modeling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP. Introduction to synthesis, Verilog HDL synthesis-Synthesis Design flow Test bench-lab exercise.

**UNIT II – BASICS OF MOS TRANSISTORS**

MOS transistors- Threshold voltage- characteristics of MOS transistor-channel length modulation- short channel effects- Design of Logic gates using NMOS, PMOS and CMOS, Stick diagrams- Transfer characteristics of CMOS inverter- Power dissipation – Delay and sizing of inverters- Lab exercise.

**UNIT III - CMOS – COMBINATIONAL CIRCUITS**

Static CMOS design-complementary CMOS - static properties- complementary CMOS design-

**UNIT IV - CMOS – SEQUENTIAL CIRCUITS**

Timing metrics for sequential circuit - latches Vs registers -static latches and registers - Bistability principle - multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non-Bistable sequential circuit-Schmitt trigger-mono stable -Astable -sequential circuit - choosing a clocking strategy.. Lab exercise in Switch level modeling

**UNIT V – SUB-SYSTEM DESIGN/ SYSTEM VERILOG**

REFERENCES

<table>
<thead>
<tr>
<th>VL2002</th>
<th>MOS DEVICE MODELING</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>L</td>
</tr>
<tr>
<td>Total Contact Hours - 60</td>
<td></td>
</tr>
<tr>
<td>Prerequisites : Nil</td>
<td></td>
</tr>
</tbody>
</table>

PURPOSE
This course deals with the modeling of MOS devices and their fundamental working concepts.

INSTRUCTIONAL OBJECTIVES
1. To make the student understand how MOSFET and other semiconductor devices are modeled.
2. To impart knowledge to simulate MOSFET for various operational requirements.
3. To impart a knowledge on advanced structures of MOSFETs like SOIFET, FinFET.

UNIT I - ELECTRON AND HOLE DENSITIES IN EQUILIBRIUM (12 hours)
Fermi – Dirac Statistics, Carrier concentration, Fermi level at equilibrium, recombination, Mobility of carriers, charge transport in semiconductors.

UNIT II - PN JUNCTION (12 hours)
PN Junction under thermal equilibrium under applied bias, Transient Analysis, Injection and Transport model, Diode small signal and large signal model.

UNIT III – MOSFET (12 hours)
Operation of Ideal MOS diode, Effects of mobile Ionic charges, Oxide charges and Interface states, C-V Characteristics, Threshold voltage of MOSFET, Bulk charge model, square law method (Level 1 is SPICE), Level 3 model in SPICE, BSIM Models.

UNIT IV - SECOND ORDER EFFECTS IN MOSFET (12 hours)
Effect of Gate voltage on carrier mobility, Effect of Drain voltage on carrier mobility, Channel length modulation, Breakdown and punch through, Subthreshold current, Short channel effects, Meyer’s model, Small signal model.

UNIT V - ADVANCED TOPICS (12 hours)
MOSFET scaling, Non-uniform doping in channel, SOI MOSFET, Buried channel MOSFET, Fin FET.
REFERENCES

VL2003

| DIGITAL SIGNAL PROCESSING STRUCTURES FOR VLSI |
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Total Contact Hours - 60
Prerequisite : Nil

PURPOSE
DSPs are used in many application areas and hence has become an essential part of VLSIs. Hence to introduce the student about DSP structures, this subject is included.

INSTRUCTIONAL OBJECTIVES
1. To understand the fundamentals of DSP
2. To learn various DSP structures and their implementation.
3. To know designing constraints of various filters.

UNIT I - INTRODUCTION TO DIGITAL SIGNAL PROCESSING (12 hours)
Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters- Filter Realizations. Representation of DSP Algorithms-Block diagram-SFG-DFG.

UNIT II - ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER (12 hours)

UNIT III - FAST CONVOLUTION AND ARITHMETIC STRENGTH REDUCTION IN FILTERS (12 hours)
UNIT IV - PIPELINED AND PARALLEL RECURSIVE FILTERS  
(12 hours)
Pipeline Interleaving in Digital Filters- Pipelining in 1st Order IIR Digital Filters- Pipelining in Higher-Order IIR Filters-Clustered Look ahead and Stable Clustered Look ahead- Parallel Processing for IIR Filters and Problems.

UNIT V - SCALING AND ROUNDOFF NOISE:  
(12 hours)

REFERENCES

<table>
<thead>
<tr>
<th>VL2004</th>
<th>CMOS ANALOG VLSI</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>L</td>
</tr>
<tr>
<td>Total Contact Hours - 75</td>
<td>3</td>
</tr>
<tr>
<td>Prerequisites : Nil</td>
<td></td>
</tr>
</tbody>
</table>

PURPOSE
Analog circuits are essential in interfacing and building amplifiers and low pass filters. This course introduces design methods for CMOS analog circuit.

INSTRUCTIONAL OBJECTIVES
1. To understand CMOS analog circuits design
2. To simulate Analog circuits using H SPICE.
3. To learn noise modeling of CMOS analog circuits

UNIT I - ANALOG CMOS SUB-CIRCUITS  
(12 hours)
Introduction to analog design, Passive and active current mirrors, band-gap references, Switched Capacitor circuits - basic principles, sampling switches, switched capacitor integrator, switched capacitor amplifier, simulation of CMOS sub circuits using SPICE.

UNIT II - CMOS SINGLE STAGE AMPLIFIERS  
(17 hours)
Common-Source stage (with resistive load, diode connected load, current-source load, triode load, source degeneration), source follower, common-gate stage, cascode stage, folded cascode stage. Frequency responses of CS stage, CD stage, CG stage, cascode stage, simulation of CMOS amplifiers using SPICE.

UNIT III - DIFFERENTIAL AMPLIFIER and OPERATIONAL AMPLIFIERS  
(16 hours)
Single-ended and differential operation, basic differential pair – qualitative and quantitative analyses, common-mode response, differential pair with MOS loads, Performance parameters of op-amp, one stage op-amp, two-stage CMOS op-amp, Gain boosting, slew rate, power supply rejection, Simulation of differential amplifiers using SPICE.
UNIT IV - OSCILLATORS (15 hours)
General considerations, Ring oscillators, LC oscillators – cross-coupled oscillators, Colpitts oscillator, One-port oscillator, and voltage controlled oscillators. Simulation of oscillators using SPICE.

UNIT V - NOISE CHARACTERISTICS (15 hours)
Statistical characteristics of noise, Types of noise - thermal noise, flicker noise, Representation of noise in circuits, noise in single-stage amplifiers (CS, CD and CG stages), noise bandwidth.

REFERENCES

<table>
<thead>
<tr>
<th>VL2005</th>
<th>VLSI DESIGN AUTOMATION</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Total Contact Hours - 60</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>Prerequisite</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MA2010</td>
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</tbody>
</table>

PURPOSE
There is a great need for methods to automate VLSI design methods. This course introduces the automation techniques.

INSTRUCTIONAL OBJECTIVES
1. To impart knowledge on implementation of graph theory in VLSI
2. To impart knowledge on automation methods for VLSI physical design
3. To impart knowledge on automation methods on VLSI interconnects.

UNIT I - DATA STRUCTURES AND BASIC ALGORITHMS (12 hours)
Basic terminology – Complexity Issues and NP-Hardness: algorithms for NP-hard problems-
Basic algorithms: Graph algorithms, computational Geometry algorithms- Basic data structures-
Graph algorithms for physical design: classes of graphs in physical design, relationship between graph classes, graph problems in physical design, algorithms for Interval graphs, permutation graphs and circle graphs.

UNIT II - PARTITIONING AND CLUSTERING (12 hours)
Partitioning and Clustering Metrics -Move-Based Partitioning Methods -Mathematical Partitioning Formulations -Clustering :Hierarchical Clustering ,Agglomerative Clustering -Multilevel Partitioning.

UNIT III - FLOORPLANNING AND PLACEMENT (12 hours)
Floorplanning: Early research-Silicing floorplan - Floorplan representation-Packaging floorplan representation-Recent advances in floorplanning.
Placement- Introduction- Problem formulation- Simulation based placement algorithms- Partitioning based placement algorithms-cluster growth- Quadratic assignment-resistive network optimization.

UNIT IV – ROUTING and COMPACTION (12 hours)

UNIT V - ISSUES ON INTERCONNECTS (12 hours)
Timing driven Interconnect synthesis- Buffer insertion basics-Generalised buffer insertion- Buffering in layout environment- Global interconnect planning. Introduction to physical design for 3D circuits.

REFERENCES
4. To understand Concepts of thermal oxidation and Si/SiO2 interface.

5. To learn concepts of dopant solid solubility, diffusion macroscopic point, different solutions to diffusion equation. Design and evaluation of diffused layers and its measurement methods.

6. To learn concepts of ion implantation, role of the crystals structures, high-energy implants, ultralow energy implants and ion beam heating methods.

UNIT I - CRYSTAL GROWTH, WAFTER PREPARATION, EPITAXY AND OXIDATION (12 hours)
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism And kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopant At interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II - LITHOGRAPHY AND RELATIVE PLASMA ETCHING (12 hours)
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments,

UNIT III - DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALLIZATION (12 hours)

UNIT IV - PROCESS SIMULATION AND VLSI PROCESS INTEGRATION (12 hours)

UNIT V - ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES (12 hours)

REFERENCES
The purpose of testing a design is twofold: 1. To ensure that, before fabrication, the circuit behavior satisfies the intent of the designer. 2. To detect faulty devices, after fabrication.

**INSTRUCTIONAL OBJECTIVES**

1. To gain knowledge on digital testing as applied to VLSI design.
2. To acquire knowledge on testing of algorithms for digital circuits.
3. To learn various testing methods for digital circuits.

**UNIT I - BASICS OF TESTING AND FAULT MODELING**

Introduction - Principle of testing - types of testing - DC and AC parametric tests - fault modeling - Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation

**UNIT II - TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS**

Test generation basics - test generation algorithms - path sensitization - Boolean difference – D-algorithm – PODEM - Testable combinational logic circuit design.

**UNIT III - TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS**

Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan

**UNIT IV - MEMORY, DELAY FAULT AND IDDQ TESTING**

Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults - Delay test- IDDQ testing - testing methods - limitations of IDDQ testing

**UNIT V - BUILT-IN SELF-TEST**

Test pattern generation of Built-in Self-Test (BIST) - Output response analysis - BIST architectures.

**REFERENCES**

PURPOSE
The purpose of reconfigurable architectures for VLSI ensures to understand the different configuration patterns, high speed computing and the usage of optical and run time configuration.

INSTRUCTIONAL OBJECTIVES
1. To gain knowledge on run time computing and its applications to VLSI.
2. To learn optical reconfigurable models.
3. To know the knowhow of various multi core architectures.

UNIT I - RECONFIGURABLE COMPUTING HARDWARE (12 hours)
Logic- computational fabric, Array and interconnect-Extended logic- Configuration- Reconfigurable processing fabric architectures-RPF integration into traditional computing systems- operating system support for reconfigurable computing- Evolvable FPGA

UNIT II - MAPPING DESIGNS INTO RECONFIGURABLE PLATFORMS (12 hours)
Structural mapping- integrated mapping- mapping for heterogeneous resources-Placement problem – clustering- simulated annealing – partition based placement – analytical placement- partitioning for granularity- partitioning of parallel programs- instance specific design

UNIT III - COMPUTATIONAL ARCHITECTURES FOR FPGA (12 hours)
Precision analysis for fixed point computation- Distributed arithmetic for FPGA – CORDIC architectures for FPGA- Boolean satisfiability – SAT solvers

UNIT IV - OPTICAL RECONFIGURATION MODELS (12 hours)
Simulation and scalability- Models, Basic algorithmic techniques- optical models – complexities of optical models- run time reconfigurability- Design and implementation

UNIT V - MULTI CORE ARCHITECTURES (12 hours)
Multi core and many core architectures-state of the art multi core operating systems-parallelism and performance analysis

REFERENCES
VL2101

DIGITAL SYSTEM SYNTHESIS AND VERIFICATION

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<thead>
<tr>
<th>L</th>
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Total Contact Hours – 45
Prerequisite : Nil

PURPOSE
HDL programming is fundamental for VLSI design and hence this course is given.

INSTRUCTIONAL OBJECTIVES
1. To gain knowledge on Verilog HDL language
2. To get an insight on system C
3. To understand the object oriented features on Verilog

UNIT –I VERILOG - BASIC CONCEPTS (9 hours)
Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters, Operands, Operators, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Test bench-lab exercise.

UNIT-II VERILOG - ADVANCED FEATURES (9 hours)
Tasks and Functions, Timing and delays, Switch level modeling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP, lab exercise. Introduction to synthesis, Verilog HDL synthesis-Synthesis Design flow –lab exercise.

UNIT-III SYSTEM VERILOG - INTRODUCTION (9 hours)

UNIT-IV OBJECT ORIENTED ANALYSIS IN SYSTEM VERILOG (9 hours)

UNIT- V SYSTEM VERILOG – ADVANCED FEATURES (9 hours)
Interprocessor synchronization - communication- scheduling semantics-clocking blocks-assertions- Hierarchy-Interfaces- System Tasks and functions – system Verilog assertion API and coverage API.

REFERENCES
PURPOSE
As a new and expanding field, with many implications, nanotechnology and nano electronics is going to pave way for new technologies. Hence this course introduced.

INSTRUCTIONAL OBJECTIVES
1. To learn the various limitation on MOSFETS and the alternates.
2. To gain knowledge on SET and Carbon nano tubes in the design of transistors
3. To learn the basics of molecular electronics and spintronics.

UNIT I - LIMITATION OF MOSFETS (9 hours)
Classical mechanics and its drawbacks, Quantum mechanics, 1D problem - particle in a box, electron tunneling., MOSFET scaling, Non-uniform doping in channel, high K dielectrics, SOI MOSFET, Buried channel MOSFET, Fin FET.

UNIT II - SINGLE ELECTRONICS (9 hours)
Coulomb blockade, Electron tunnelling devices, Single electron transistors , Resonant Tunneling Diodes- principle and applications, Quantum computing, Quantum cellular automata

UNIT III- CARBON NANO TUBES (9 hours)
Carbon nano tubes – Basic structures, CNTFETs, Applications.

UNIT IV - MOLECULAR ELECTRONICS (9 hours)
Molecular wire conductance - Theories of Coherent Electron Transport in molecular junctions, Evaluation of the conductance for coherent transport, Incoherent transport and vibronic coupling, Molecular circuit elements, Circuits.

UNIT V - SPINTRONICS (9 hours)
Spin Vs charge, AMR, GMR, TMR, Spin devices- Spin valves, Magnetic tunnel junctions, Applications – memories (MRAM, STRAM), Logic device, and microwave oscillators.

REFERENCES
UNIT I - INTRODUCTION TO LOW POWER VLSI DESIGN and ANALYSIS (9hours)
Introduction to low power VLSI design-Need for low power-CMOS leakage current-static current-Basic principles of low power design-probabilistic power analysis-random logic signal-probability and frequency-power analysis techniques-signal entropy.

UNIT II - CIRCUIT LEVEL AND LOGIC LEVEL DESIGN TECHNIQUES (9hours)
Circuit - transistor and gate sizing - pin ordering - network restructuring and reorganization - adjustable threshold voltages - logic-signal gating - logic encoding. Pre-computation logic.

UNIT III - SPECIAL LOW POWER VLSI DESIGN TECHNICQUES (9 hours)
Power reduction in clock networks - CMOS floating node - low power bus - delay balancing Switching activity reduction - parallel voltage reduction - operator reduction -Adiabatic computation - pass transistor logic

UNIT IV - LOW VOLTAGE LOW POWER MEMORIES (9 hours)
Basics of SRAM- Memory cell –Pre-charge and equalization circuit decoder-ATD Sense amplifier-Output latch-Low power SRAM technologies-types of DRAM –Basics of DRAM-Cell refresh circuit-HVG-BBG-BVG-RVG-VDC

UNIT V - SOFTWARE DESIGN AND POWER ESTIMATION (9 hours)
Low power circuit design style - Software power estimation - co design, for low power.

REFERENCES
PURPOSE
The purpose of this course is
1. To introduce neural network concepts to the student
2. To apply artificial neural network concepts in VLSI

INSTRUCTIONAL OBJECTIVES
1. To gain knowledge on neural networks, its theory and various types.
2. To acquire knowledge on implementation of neural networks for VLSI problems.
3. To learn Pulse stream technique in neural networks.

UNIT I - INTRODUCTION AND BASIC CONCEPTS (9 hours)
Introduction- Humans and Computers, the structure of the brain, learning in machines, the differences. The basic neuron- Introduction, modeling the single neuron, learning in simple neurons, the perception: a vectorial perspective, the perception learning rule, proof, limitations of perceptrons.

UNIT II - Multilayer Networks (9 hours)
The multi layer perceptron: Introduction, altering the perception model, the new model, the new learning rule, multi layer perception algorithm, XOR problem. Multi layer feed forward networks, error back propagation training algorithm: problems with back propagation, Boltzman training, Cauchy training, combined back propagation, Cauchy training.

UNIT III - NeurAl VLSI (9 hours)

UNIT IV - Pulse Stream Technique (9 hours)
Pulse encoding of information, Pulse stream arithmetic – addition and multiplication, Pulse stream communication, Pulse stream case studies – Edinburg SADMANN/ EPSILON work, The EPSILON chip, Process invariant summation and multiplication – the synapse, Pulse frequency modulation neuron, Pulse width modulation neuron, Switched-capacitor design, Per-pulse computation, EPSILON – The chosen neuron/synapse cells and results
UNIT V - APPLICATIONS OF NEURAL VLSI (9 hours)

REFERENCES

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<tr>
<th>VL2105</th>
<th>VLSI DIGITAL SIGNAL PROCESSING SYSTEMS</th>
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PURPOSE
As DSP has become an essential component of VLSI applications, this Course discusses implementation methods and problems in optimization algorithm of VLSI DSP Systems.

INSTRUCTIONAL OBJECTIVES
1. To know the various methods for implementation of DSP systems.
2. To understand the various implementations of VLSI DSP architectures for Arithmetic operations.
3. To gain knowledge on low power DSP architectures.

UNIT I - UNFOLDING (9 hours)

UNIT II - DIGITAL MULTIPLIER ARCHITECTURES (8 hours)
Parallel Multipliers- Interleaved Floor-plan and Bit-Plane-Based Digital Filters- Bit-Serial Multipliers- Bit-serial Filter Design and Implementation- Canonic Signed Digit Arithmetic- Distributed Arithmetic.

UNIT III - REDUNDANT ARITHMETIC (11 hours)
UNIT IV - SYNCHRONOUS AND ASYNCHRONOUS PIPELINING (9 hours)
Synchronous Pipelining and Clocking Styles- Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs- Wave Pipelining- Constraint Space Diagram and Degree of Wave Pipelining- Implementation of Wave-Pipelined Systems- Asynchronous Pipelining- Signal Transition Graphs- Use of STG to Design Interconnection Circuits- - Implementation of Computational Units.

UNIT V - LOW POWER VLSI DSP SYSTEMS (8 hours)
Theoretical Background- Scaling Versus Power Consumption- Power Analysis- Power Reduction Techniques- Power Estimation Approaches.-Simulation Based Approach.

REFERENCES

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PURPOSE
As VLSI implementation is largely in ASIC this subject is introduced here.

INSTRUCTIONAL OBJECTIVES
1. To learn the fundamentals of ASIC and its design methods
2. To gain knowledge on programmable architectures for ASICs
3. To understand the physical design of ASIC.

UNIT I - INTRODUCTION TO ASIC’S (7 hours)
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture.

UNIT II - PROGRAMMABLE ASIC’S (9 hours)
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC and AC inputs and outputs - Clock and Power inputs - Xilinx I/O blocks.

UNIT III - PROGRAMMABLE ASIC LOGIC CELLS (9 hours)
UNIT IV - ASIC FLOOR PLANNING, PLACEMENT AND ROUTING  (11 hours)
ASIC Construction: Physical Design- System Partitioning- FPGA Partitioning- Partitioning
Routing: Global Routing - Detailed Routing- Special Routing. Design checks

UNIT V - OPTIMIZATION ALGORITHMS  (9 hours)
Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length
and bend minimization technique-over the cell(OTC) Routing-multichip modules(MCM)-
Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D
compaction-2D compaction

REFERENCES
2. Farzad Nekoogar and Faranak Nekoogar, “From ASICs to SOCs: A Practical

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<tr>
<th>VL2107</th>
<th>CMOS MIXED SIGNAL CIRCUIT DESIGN</th>
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PURPOSE
As many real life applications involve both analog and digital circuits, this course aims to
introduce the problems in implementing Analog and Digital Circuits in a single silicon wafer.

INSTRUCTIONAL OBJECTIVES
1. To know mixed signal circuits like DAC, ADC, PLL etc.
2. To gain knowledge on filter design in mixed signal mode.
3. To acquire knowledge on design different architectures in mixed signal mode.

UNIT I - PHASE LOCKED LOOP  (9 hours)
Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL
- simple PLL, charge-pump PLL, applications of PLL.

UNIT II - SAMPLING CIRCUITS  (9 hours)
Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits,
different types of sampling switches. Sample-and-Hold Architectures- Open-loop and closed-
loop architectures, open-loop architecture with miller capacitance, multiplexed-input
architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

UNIT III - D/A CONVERTER ARCHITECTURES  (9 hours)
Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter,
D/A converter in terms of voltage, current, and charge division or multiplication, switching
functions to generate an analog output corresponding to a digital input. Resistor-Ladder
architectures, current-steering architectures.
UNIT IV - A/D CONVERTER ARCHITECTURES (9 hours)
Input/output characteristics and quantization error of an A/D converter, performance metrics of pipelined architectures, Successive approximation architectures, interleaved architectures.

UNIT V - INTEGRATOR BASED FILTERS (9 hours)
Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-c integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

REFERENCES

VL2108

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<th>DSP ARCHITECTURE AND APPLICATIONS</th>
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PURPOSE
This course introduces Digital Signal processors.

INSTRUCTIONAL OBJECTIVES
1. To know various DSP architectures and their applications.
2. To gain technical knowhow of various DSP processors

UNIT I - OVERVIEW OF DIGITAL SIGNAL PROCESSING (9 hours)
Advantages of DSP over analog systems, salient features and characteristics of DSP systems, applications of DSP systems. Common features of DSP processors, numeric representations in DSP processor, data path of a DSP processor, memory structures in DSP processors, VLIW architecture, special addressing modes in DSP processors, pipelining concepts, on-chip peripherals found in DSP processors.

UNIT II - TMS320C5X PROCESSORS (9 hours)
Architecture of TMS320C5X Processors- Assembly Instructions- Addressing Modes- Pipelining and Peripherals-Lab exercises

UNIT III - TMS320C3X PROCESSORS (9 hours)
Architecture of TMS320C3X- Instruction Set- Addressing Modes- Data Formats- Floating Point Operation- Pipelining and Peripherals- Lab exercises
UNIT IV - BLACK FIN PROCESSOR  
Introduction to Black fin processor- Architecture overview-processor core-addressing modes-instruction sets-Targeted applications - Lab exercises.

UNIT V - SHARC PROCESSOR  

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PURPOSE
Memory is an important part in many digital circuits and microcontrollers. This course discusses implementation methods and problems in designing and making semiconductor memories.

INSTRUCTIONAL OBJECTIVES
1. To know the design of MOS memories and the various precautionary methods to be used in their design.
2. To gain knowledge on various testing methods of semiconductor memories.
3. To get an overview on reliability of semiconductors.

UNIT I - RAM  
SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

UNIT II - NONVOLATILE MEMORIES  
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-AdvancedFlash Memory Architecture.
UNIT III - MEMORY FAULT MODELING AND TESTING  
RAM Fault Modelling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-
Non-volatile Memory Modelling and Testing-IDDQ Fault Modelling and Testing-Application
Specific Memory Testing

UNIT IV - SEMICONDUCTOR MEMORY RELIABILITY  
General Reliability Issues-RAM Failure Modes and Mechanism-Non-volatile Memory
Reliability-Reliability Modelling and Failure Rate Prediction-Design for Reliability-Reliability
Test Structures-Reliability Screening and Qualification.

UNIT V - ADVANCED MEMORY TECHNOLOGIES  
Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs - Analog
Memories-Magneto-resistive Random Access Memories (MRAMs)-Experimental Memory
Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM
Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future
Directions.

REFERENCES

VL2110 SYSTEM-ON-CHIP DESIGN

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Total Contact Hours – 45
Prerequisite : Nil

PURPOSE
IP cores and application specific design is becoming the order of the day. Because of
usefulness of this for both VLSI and embedded students this subject is provided.

INSTRUCTIONAL OBJECTIVES
1. To learn System on chip fundamentals, their applications.
2. To gain knowledge on NOC design.
3. To learn the various computation models of SOCs

UNIT I - INTRODUCTION  
Introduction to SoC Design., Platform-Based SoC Design., Multiprocessor SoC and Network on
Chip, Low-Power SoC Design

UNIT II - SYSTEM DESIGN WITH MODEL OF COMPUTATION AND CO-DESIGN  
System Models, Validation and Verification, Hardware/Software Codesign Application
Analysis, Synthesis.
UNIT III - COMPUTATION–COMMUNICATION PARTITIONING AND NETWORK ON CHIP-BASED SOC (9 hours)

UNIT IV - NOC DESIGN (9 hours)

UNIT V - NOC /SOC CASE STUDIES (9 hours)
Real Chip Implementation-BONE Series-, BONE 1-4, Industrial Implementations-, Intel’s Tera-FLOP 80-Core NoC, Intel’s Scalable Communication Architecture, Academic Implementations- FAUST, RAW; design case study of SoC –digital camera

REFERENCES

VL2111

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<th>GENETIC ALGORITHMS AND APPLICATIONS IN VLSI</th>
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PURPOSE
Optimization methods are necessary for making circuits and making device layouts. This course deals with Genetic Algorithm as an optimization application for VLSI design.

INSTRUCTIONAL OBJECTIVES
1. To gain knowledge on Genetic algorithms
2. To learn implementation of genetic algorithms for VLSI physical design problems
3. To understand implementation of genetic algorithms for testing of VLSI circuits and technology mapping.

UNIT I - FUNDAMENTALS OF GENETIC ALGORITHM (9 hours)

UNIT II - PARTITIONING (9 hours)
Problem description – Circuit partitioning by genetic algorithms – hybrid genetic algorithms for ratio-cut partitioning.
UNIT III - PLACEMENT AND ROUTING  
(9 hours)
Placement: Standard cell placement – Macro cell placement – Standard cell placement on a network of workstations
Routing: Steiner problem in graph – macro cell global routing

UNIT IV - GENETIC ALGORITHMS IN VLSI TESTING  
(9 hours)
Problem description – test generation frame work – test generation for test applications time reduction – deterministic/genetic test generators sequences-dynamic test sequence compaction – parallel algorithms for ATPG

UNIT V - FPGA TECHNOLOGY MAPPING and PEAK POWER ESTIMATION  
(9 hours)

REFERENCES

RELIABILITY ENGINEERING

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Total Contact Hours - 45
Prerequisites : Nil

PURPOSE
For any system reliability is an essential parameter. For evaluating reliability of designs, it is necessary to know reliability analysis methods.

INSTRUCTIONAL OBJECTIVES
1. To learn basics of reliability evaluation methods
2. To understand its application to electronic circuit.
3. To understand the various Failure modes of many electronic components.

UNIT I - RELIABILITY AND RATES OF FAILURE  
(9 hours)
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques - Weibull, extreme value, hazard, binomial data; Analysis of load - strength interference, Safety margin and loading roughness on reliability.

UNIT II - STATISTICAL EXPERIMENTS  
(9 hours)
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, petric Nets, State space Analysis, Monte Carlo simulation, Design analysis methods - quality function deployment, load strength analysis, failure modes, effects and criticality analysis.
UNIT III - ELECTRONIC SYSTEMS AND SOFTWARE RELIABILITY (9 hours)
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV - RELIABILITY TESTING (9 hours)
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V - RELIABILITY IN MANUFACTURE AND MAINTENANCE (9 hours)
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

REFERENCES

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<th>VL2113</th>
<th>FUNDAMENTALS AND APPLICATIONS OF MEMS</th>
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PURPOSE
MEMS technology offers many exciting opportunities in miniaturization of elements in a wide range of applications. MEMS based sensors and actuators are constantly introduced into new products and new markets are expected to become affected by MEMS technology in the near future. The diversity and complexity of this technology demands a wide knowledge base from a prospect researcher. The goal of this course is to provide the student the needed background to comprehend existing technology, the tools to execute MEMS fabrication and the expertise to approach the development of new MEMS tools.

INSTRUCTIONAL OBJECTIVES
1. To familiarize with MEMS Materials and Scaling Laws in Miniaturization.
3. To study Microsystems Fabrication Process.
4. To familiarize with Microsystems Design, Assembly and Packaging.
5. To explore on various Case Study of MEMS Devices.
UNIT I - OVERVIEW OF MEMS AND MICROSYSTEMS, MEMS MATERIALS AND SCALING LAWS IN MINIATURATION (9 hours)

Materials For MEMS - Substrate & wafer, Si as a substrate material, Si compound, Si Piezo-resistors, Gallium Arsenide, quartz, Piezoelectric crystals, polymers packaging Materials.

Scaling Laws in Miniaturization-Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer

UNIT II - ENGINEERING MECHANICS AND THERMOFLUID ENGINEERING FOR MICROSYSTEMS DESIGN (9 hours)
Atomic structure of matter, Ions and ionization, Molecular theory of matter and intermolecular forces, Doping of semiconductors, Diffusion process, Plasma physics, Electrochemistry, Static bending of thin plates, Mechanical vibration analysis, Thermo mechanical analysis, Overview of finite element analysis.


UNIT III - MICROSYSTEMS FABRICATION PROCESS (9 hours)

UNIT IV - MICROSYSTEMS DESIGN, ASSEMBLY AND PACKAGING (9 hours)
Micro system Design - Design consideration, process design, Mechanical design, Mechanical design using MEMS. Mechanical packaging of Microsystems, Microsystems packaging, interfacings in Microsystems packaging, packaging technology, selection of packaging materials, signal mapping and transduction.

UNIT V - CASE STUDY OF MEMS DEVICES (9 hours)
Case study on strain sensors, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes, RF MEMS Switch, phase shifter, and smart sensors. Case study of MEMS pressure sensor Packaging.

REFERENCES
**PURPOSE**
The explosive growth in wireless telecommunications, expects the design of RF circuits with low power consumption and low noise. This course aims to introduce the design of CMOS RF circuits suitable for transmitter and receiver architectures.

**INSTRUCTIONAL OBJECTIVES**
1. To explore the various performance measures of RF circuits.
2. To acquire knowledge on the design of RF filters, amplifiers and oscillators

**UNIT I - PERFORMANCE PARAMETERS OF RF CIRCUITS** (9 hours)
Gain Parameters, Non-linearity parameters, Noise figure, Phase Noise, Dynamic range, RF front end performance parameters, performance trade offs in an RF circuit.

**UNIT II - FILTER DESIGN** (9 hours)
Modern filter design, Frequency and impedance scaling, High Pass filter design, Band pass filter design, Band reject filter design, the effects of finite Q.

**UNIT III - HIGH FREQUENCY AMPLIFIER DESIGN** (9 hours)
Zeros as Bandwidth enhances, Shunt-series Amplifier, Bandwidth enhancement with frequency Doublers, Tuned amplifiers, Neutralization and unilateralization, cascaded Amplifiers, LNA Topologies.

**UNIT IV - MIXERS AND OSCILLATORS** (9 hours)
Mixer fundamentals, Non linear systems as Linear mixers, multiplier based mixers, Subsampling mixers.
Problems with purely linear oscillators, Tuned oscillator, Negative Resistance oscillators, frequency synthesis.

**UNIT V - RF POWER AMPLIFIERS** (9 hours)
General considerations, Class A, AB, B and C Power amplifier, Class D, E and F amplifiers, modulation of power amplifiers, RF Power amplifier design examples.

**REFERENCES**
PURPOSE
This course is aimed at providing high speed design techniques for use in VLSI design.

INSTRUCTIONAL OBJECTIVES
1. To gain knowledge on circuits and techniques involved in high speed VLSI circuits.
2. To explore various design strategies to be followed for designing a high speed VLSI circuits.
3. To understand the logic styles for designing a high speed VLSI circuit.

UNIT I - CLOCKED LOGIC STYLES (9 hours)
Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic Non Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families.

UNIT II - CIRCUIT DESIGN MARGINING AND DESIGN VARIABILITY (9 hours)
Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

UNIT III - LATCHING STRATEGIES (9 hours)

UNIT IV - INTERFACE TECHNIQUES (9 hours)
Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design

UNIT V - CLOCKING STYLES (9 hours)
Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

REFERENCES
2. Evan Sutherland, Bob Stroll, David Harris,” Logical Efforts, Designing Fast CMOS Circuits”, Kluwer Academic Publishers, 1999
UNIT I - INTRODUCTION TO MAGNETOELECTRONICS (9 hours)
Introduction – What is magnetoelectronics – Key Engineering Issues Magnetoelectronics must solve – Spin vs Charge – Transport in Semiconductors, Metals- Spin-Polarized Current – Spin-Dependent Tunneling in Magnetic Tunnel Junction

UNIT II - SPIN VALVES (9 hours)

UNIT III - MAGNETIC TUNNEL JUNCTION (9 hours)

UNIT IV - MAGNETORESISTIVE RANDOM ACCESS MEMORY (9 hours)

UNIT V - MICROMAGNETIC SIMULATION (9 hours)

REFERENCES
VLSI INTERCONNECTS AND ITS DESIGN TECHNIQUES

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Total Contact Hours – 45
Prerequisites : Nil

PURPOSE
VLSI interconnects modeling is playing vital role in the IC design.

INSTRUCTIONAL OBJECTIVES
1. To gain knowledge on VLSI Interconnects
2. To get an insight on Transmission line parameters of VLSI interconnects
3. To understand the novel solutions on interconnects.

UNIT –I PRELIMINARY CONCEPTS OF VLSI INTERCONNECTS (9 hours)
Interconnects for VLSI applications-copper interconnections –method of images- method of moments- even and odd capacitances- transmission line equations- miller’s theorem- Resistive interconnects as ladder network- Propagation modes in micro strip interconnects- slow wave propagations- Propagation delay.

UNIT-II PARASITIC RESISTANCES, CAPACITANCE & INDUCTANCE (9 hours)

UNIT- II INTERCONNECTION DELAYS (9 hours)
Metal insulator semiconductor micro strip line- transmission line analysis for single level interconnections- transmission line analysis for parallel multilevel interconnections- analysis of crossing interconnections- parallel interconnection models for micro strip line- modelling of lossy parallel and crossing interconnects- high frequency losses in micro strip line- Expressions for interconnection delays- Active interconnects.

UNIT-IV CROSS TALK ANALYSIS (9 hours)
Lumped capacitance approximation- coupled multi conductor MIS micro strip line model for single level interconnects- frequency domain level for single level interconnects- transmission line level analysis of parallel multi level interconnections.

UNIT-V NOVEL SOLUTIONS FOR PROBLEMS IN INTER (9 hours)
Optical interconnects – carbon Nano tubes / Graphenes vs. Copper wires.

REFERENCES
5. Hall S H, G W Hall and J McCall, High speed digital system design, Wiley inter-science

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<tr>
<th>VL2118</th>
<th>DIGITAL HDL DESIGN AND VERIFICATION</th>
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<td>Total Contact Hours – 45</td>
<td>3</td>
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<td>3</td>
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<td>Pre-requisites - VL2001</td>
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**PURPOSE**

HDL programming is fundamental for VLSI design and hence this course is given.

**INSTRUCTIONAL OBJECTIVES**

1. To gain knowledge on VHDL
2. To get an insight on Advanced VHDL
3. To understand the System C

**UNIT-I VHDL- BASIC CONCEPTS**

Operators, Basic concepts, Entity and Architecture design, System task and functions, Value set, Data types, Operands, Operators, Entity and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Test Bench - lab exercise.

**UNIT-II VHDL- ADVANCED FEATURES**

Packages and Functions, Sub-Program, User Defined Attributes, Specifications and Configurations, Delay modeling- pin-to-pin delay and distributed delay modeling- Timing delay analysis- FSM design and Synthesis-UART –lab exercise.

**UNIT-III SYSTEM C – INTRODUCTION**

Introduction to System C- Design methodology – Data Types – Bit, Logic, Integer, Precision signed type and resolved types, user defined data type- Data operators – Logical, arithmetic, relational operators, vectors and ranges- sequential statements – IF, LOOP, SWITCH statements- methods – structures.

**UNIT-IV COMBINATIONAL and SYNCHRONOUS LOGIC DESIGN IN SYSTEM C**

SC_module – File Structure, Reading and writing port signals. Miscellaneous logic – modeling basic combinational logic circuits (Multiplexer, Decoder, encoder, memory model, modeling an FSM- Moore’s and Mealy FSM – Universal Shift Register.
UNIT-V SYSTEM C – ADVANCED FEATURES (9 hours)

REFERENCES

UNIT I - ANALYSIS AND DESIGN OF ALGORITHMS (9 hours)

UNIT II - VLSI MODELS (9 hours)
Integrated circuits and the mead Conway rules-VLSI implementation of logic-Abstraction of VLSI circuits. Lower bounds on area and time: Introduction to lower bound arguments-information and crossing sequence- probabilistic circuits and algorithms – circuits with repetitive inputs.

UNIT III - ALGORITHM FOR VLSI Design (9 hours)
Algorithms for layout –organization with high area- Compilation and optimization algorithms.

UNIT IV - OVERVIEW OF VLSI DESIGN SYSTEMS (9 hours)
UNIT V - ALGORITHMS FOR VLSI DESIGN TOOLS  (9 hours)

REFERENCES


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<tr>
<td>COMPUTATIONAL INTELLIGENCE</td>
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<td>Total Contact Hours - 45</td>
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<td>Prerequisites : Nil</td>
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PURPOSE

The purpose of this course is to make the student understand the various optimization techniques and the evolutionary algorithms.

INSTRUCTIONAL OBJECTIVES

1. To understand the concept of computational intelligence
2. To explore genetic and evolutionary algorithms
3. To learn the knowhow of differential evolution
4. To understand the concept of Particle swarm optimization and ant colony algorithms

UNIT I - INTRODUCTION TO COMPUTATIONAL INTELLIGENCE  (9 hours)
Computational intelligence paradigms: Artificial Neural networks, evolutionary Computation, swarm intelligence, artificial immune systems and fuzzy systems. Introduction to Evolutionary computation: Genetic evolutionary algorithms, Representation, Initial population, fitness function, selection, reproduction of operators, stopping conditions and evolutionary computation versus classical optimization.

UNIT II - GENETIC ALGORITHMS AND PROGRAMMING  (9 hours)
Genetic algorithms: Canonical GA, crossover, mutation, control parameters, GA variants, applications Genetic programming: Tree based representation, initial population, fitness function, cross over operators, mutation operators, building block in Genetic programming.

UNIT III - EVOLUTIONARY PROGRAMMING AND ITS STRATEGIES  (9 hours)
Basic of Evolutionary programming- operators- strategy parameters- implementations- Genetic evolutionary strategy algorithms-strategy parameters and self adoption- evolution strategy variants.

UNIT IV - DIFFERENTIAL EVOLUTION  (9 hours)
UNIT V - COMPUTATIONAL SWAM INTELLIGENCE (9 hours)

Particle swarm optimization: Basics- social network structures- Basic variations- PSO parameters- single solution PSO- applications
Ant algorithms: ant colony optimization Meta-Heuristic- Cemetery organization and brood care- division of labor- Applications

REFERENCES

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</thead>
<tbody>
<tr>
<td>CHROMATIC GRAPH THEORY</td>
<td>3</td>
<td>0</td>
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<tr>
<td>Total Contact Hours - 45</td>
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PURPOSE
The purpose of this course is to make the student understand the basic concepts of graph theory and the coloring of graphs and role of it in VLSI CAD.

INSTRUCTIONAL OBJECTIVES
1. To understand the concept of vertex coloring and edge coloring
2. To understand the concept of coloring on surfaces

UNIT I - INTRODUCTION TO GRAPHS (9 hours)
Trees and connectivity, Eulerian and Hamiltonian Graphs- Matching and factorization.

UNIT II - INTRODUCTION TO VERTEX COLORING (9 hours)
Chromatic number of a graph, applications of coloring, perfect graphs- restricted vertex coloring: uniquely colorable graphs, list coloring, pre-coloring extensions of graphs.
Case studies: VLSI Partitioning as vertex coloring problem, a chaotic neural network for the graph coloring problem in VLSI channel routing and on rectangle intersection and overlap graphs for VLSI floor planning

UNIT III - BOUNDS OF CHROMATIC NUMBERING (9 hours)
Bounds for the chromatic number: color-critical graphs, upper bounds and greedy coloring, upper bounds and oriented graphs, the chromatic number of Cartesian product.
Coloring graphs on surfaces: four color problem, conjecture of Hajos and Hadwiger, chromatic polynomials, Heawood map-coloring.

UNIT IV - EDGE COLORING OF GRAPH (9 hours)
Edge coloring of graphs- monochromatic and rainbow colorings-complete coloring–distinguish coloring.
Case study: Fast approximation algorithms on max cut, k-coloring, and k-color ordering for VLSI applications and interval graph algorithms for 2D multiple folding of array based VLSI circuits

UNIT V - SPECIAL TYPES ON COLORING

Coloring, distance and domination: T-coloring, Radio coloring, Hamiltonian coloring, domination coloring.

Case study: A new graph coloring algorithm for constrained via minimization in VLSI circuits and Hybrid symbolic-explicit techniques for the graph coloring problem

REFERENCES


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<tbody>
<tr>
<td>SOLAR CELLS AND THIN FILM TECHNOLOGIES</td>
<td>3</td>
<td>0</td>
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<td>3</td>
</tr>
<tr>
<td>Total Contact Hours - 45</td>
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<td>Prerequisites</td>
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PURPOSE

Generation of electricity through solar energy is among the top priority issues in today's world. Photovoltaic cells convert solar energy into electrical energy by separating the photo-generated electron and holes. Over the last decade, the field has emerged as an application of recognized potential and has attracted the interest of students and researchers. Newer materials and structures are being studied and new solar cell industries are coming up. In view of this there is a need to offer a dedicated elective course on this subject to the students at undergraduate/post-graduate level.

INSTRUCTIONAL OBJECTIVES

The course objectives are to make sure each student:
1. understands the basics of light and solar irradiance
2. understands the basics of PN junction
3. understands solar cell designs
4. understands solar cell operation
5. acquires knowledge of the various solar cells technologies

UNIT-I: SOLAR IRRADIANCE

(9 hours)


Solar Radiation: The Sun, solar radiation in space, solar radiation outside the earth’s atmosphere, terrestrial solar radiation, solar radiation at the earth’s surface, atmospheric effects, air mass, motion of the sun, solar time, declination angle, elevation angle, azimuth angle, the sun’s position, solar radiation on a tilted surface, arbitrary orientation and tilt, calculation of solar insulation, measurement of solar radiation.
UNIT-II: PN JUNCTION
(9 hours)
**Basics**: Semiconductor materials, semiconductor structure, conduction in semiconductor, band gap, intrinsic carrier concentration, doping, and equilibrium carrier concentration.
**Generation**: Absorption of light, absorption coefficient, absorption depth, generation rate.
**Recombination**: Types of recombination, life time, diffusion length, surface recombination.
**Carrier Transport**: movement of carriers in semiconductor, diffusion, drift.
**PN Junction**: Formation of a PN junction, PN junction diode, bias of PN junctions, diode equations, diode equation for PV, ideal diode equation derivation, basic equations, applying basic equations to a PN junction, solving for depletion region and quasi-neutral regions, finding total current.

UNIT-III: SOLAR CELLS
(9 hours)
**Principles of solar cell operation**: Electrical characteristics, optical properties, typical solar cell structures, ideal efficiencies.
**Crystalline silicon solar cells**: Manufacturing and properties of Crystalline silicon, high-efficiency laboratory cells, screen-printed cells, laser-processed cells, HIT cell, rear-contacted cells, thin silicon solar cells – light trapping, voltage enhancements, silicon deposition and crystal growth.

UNIT-IV: THIN-FILM SILICON SOLAR CELLS
(9 hours)
Hydrogenated amorphous silicon (a-Si:H) layers, hydrogenated microcrystalline silicon (μSi:H) layers, p-i-n and n-i-p structures, tandem and multi-junction solar cells.

UNIT-V: RECENT ADVANCES IN THIN-FILM SOLAR CELLS
(9 hours)
CdTe based thin film solar cells, CuInSe₂ (CIS) based thin-film solar cells, thin-film GaAs solar cells, Chalcopyrite Based Solar Cells, concentrator silicon solar cells, dye-sensitized thin-film solar cells, organic solar cells

REFERENCES
PURPOSE
Photovoltaics are regarded by many as the most likely candidate for long-term sustainable energy production. This course discusses about the new novel concepts to produce a new generation of low-cost, high performance photovoltaics that make improved use of the solar spectrum. The topics in this course include discussions on high efficiency III-V multi-junction solar cells, and new concept design solar cells including quantum well, quantum dots, intermediate-band solar cells, thermophotovoltaic cells, and other nanostructured devices. ‘Next Generation Photovoltaics’ will be an essential course for graduate students and researchers working with solar cell technology.

INSTRUCTIONAL OBJECTIVES
The course objectives are to:
1. review multijunction solar cells and the use of concentrated light
2. understand the potential of plasma polaritons and to master the light management
3. give an overview of new novel concepts and trends to produce low-cost, high performance photovoltaics

UNIT-I: TRENDS IN THE DEVELOPMENT OF PHOTOVOLTAICS (9 hours)
Simple structures and simple technologies, nanostructures and ‘high technologies’, multi-junction solar cells, concentration of solar radiation, concentrators in space, non-solar photovoltaics, concepts of solar cells with ultra-high frequencies – thermophotovoltaic conversion, hot carrier cells, tandem cells, intermediate level cells, photon up- and down-conversion.

UNIT-II: HIGH EFFICIENCY SOLAR DEVICES (9 hours)
III-V Multi-junction solar cells: Basic principles of multi-junction solar cells, triple-junction, four-junction, five- and six-junction solar cells, prospects of multi-junction solar cells
High concentration PV technology (HCPV): Classification, merits and status of CPV, overview of HCPV modules, RandD,

UNIT-III: THERMOPHOTOVOLTAIC (TPV) CONVERTERS (9 hours)
Progress in thermophotovoltaic converters: TPV based on III/V low-bandgap photocells, TPV in residential heating systems, progress in TPV with silicon photocells, design of a novel thin-film TPV system.
Solar cells for TPV converters: Predicted efficiency of TPV cells, Ge-based TPV cells, Si-based TPV cells, TPV cells based on InAs- and GaSb- related materials, TPV cells based on InGaAs/InPheterostructures.
UNIT-IV: NEW CONCEPTS BASED SOLAR CELLS   (9 hours)
Quantum Well Cells: QW cells, strain compensation, QWs in tandem cells, QWCs with light trapping, QWCs for thermophotovoltaics
Quantum Dot solar cells: Silicon-QD solar cell, III-V multi-junction QD solar cells
Intermediate-Band Solar Cells: Preliminary concepts and definitions, IBSC model, QD IBSC
Nanowire (NW) solar cells: Silicon NW solar cells, compound semiconductor NW solar cells
NW-polymer hybrid solar cells: InP nanowire-polymer (P3HT) hybrid solar cell, microcrystalline silicon nanorods / P3HT hybrid solar cells, TiO2 nanotube arrays in DSCs

UNIT-V: OTHER CONCEPTS       (9 hours)
Light management in thin-film solar cell, Hot carrier solar cells, plasmonics photovoltaics, nanostructured materials for thin film solar cells, crystalline silicon on glass (CSG) solar cells.

REFERENCES

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<th>VL2124</th>
<th>QUANTUM COMPUTATION AND INFORMATION</th>
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<td>Total Contact Hours - 45</td>
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<td>Pre-requisites: Nil</td>
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PURPOSE
The purpose of this course is to make the student understand the computational aspects and information for designing.

INSTRUCTIONAL OBJECTIVES
1. To understand the Quantum computing and Quantum information
2. To learn Quantum search algorithm.
3. To understand Quantum information theory and cryptography

UNIT-I: INTRODUCTION   (9 hours)

UNIT-II: QUANTUM CORRELATIONS   (9 hours)
Bell Inequalities And Entanglement - Schmidt Decomposition - Super-Dense Coding - Teleportation - PPT Criterion.
UNIT-III: QUANTUM GATES AND ALGORITHMS (9 hours)

UNIT-IV: QUANTUM INFORMATION THEORY (9 hours)

UNIT-V: QUANTUM CRYPTOGRAPHY (9 hours)
Private Key Cryptography - Quantum Key Distribution - Entropic Uncertainty Relations – The Security of Quantum Key Distribution

TEXT-BOOKS
3. Lecture notes by Prof. John Preskill, California Institute of Technology

REFERENCES

VL2125

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<tbody>
<tr>
<td>SUPERCONDUCTIVITY: THEORY &amp; ITS EFFECTS</td>
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<td>0</td>
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<tr>
<td>Total Contact Hours - 45</td>
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<td>Pre-requisites: Nil</td>
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PURPOSE
The purpose of this course is to make the student understand the basics in superconductivity

INSTRUCTIONAL OBJECTIVES
1. To learn different types of superconductor types
2. To understand superconductor theory
3. To understand superconductor Effects

UNIT-I: INTRODUCTION (9 hours)
Basic Phenomena - Perfect Conductivity - Perfect Diamagnetism - Critical Temperature – Fields and Currents - Type-I and Type-II - High-Temperature Superconductors.
UNIT-II: BCS THEORY

UNIT-III: GINZBURG-LANDAU THEORY
GL Free Energy – GL Differential Equation – Critical Current of Thin Wire or Film – Linearized GL Equation

UNIT-IV: JOSEPHSON EFFECT-I

UNIT-V: JOSEPHSON EFFECT-II: PHENOMENA UNIQUE TO SMALL JUNCTION

TEXT-BOOKS

REFERENCES
PURPOSE
Recent Trends in developing embedded systems are multi core processors. This course gives you knowledge about real time embedded systems.

INSTRUCTIONAL OBJECTIVES
1. To gain knowledge in embedded multi core architecture
2. To learn real time scheduling Algorithm
3. To know details about multi core applications

UNIT-I MULTI CORE PROCESSORS (9 hours)

UNIT-II-REAL TIME SCHEDULING ALGORITHM (9 hours)

UNIT-III-EXECUTION TIME AND ENERGY ESTIMATION (9 hours)

UNIT-IV-DESIGN OF EMBEDDED COMPONENTS (9 hours)
Hardware Components-Firmware Components-RTOS Systems-Software Mechanisms-Software Application Components-Debugging Components-Performance Tuning-High Reliability Design.

UNIV-V-CASE STUDIES (9 hours)
System Life Cycle Application-Media Application-Robotic Application-Computer Vision Applications.

REFERENCES
2. Maryline Chetto ”Real Time system scheduling” ISTE Wiley and John Sons, Oxford University, 1st edition 2014.
ADVANCED SEMICONDUCTOR PHYSICS  

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Total Contact Hours: 45  
Prerequisite: Nil

PURPOSE  
This course helps to review the fundamentals of semiconductor physics and focuses on the advanced physical principles and operational characteristics of modern semiconductor electronic devices such as metal-oxide systems, bipolar, high-electron mobility, and field-effect transistors.

INSTRUCTIONAL OBJECTIVES  
1. To understand the advance physics of semiconductor material and electronic devices.
2. To be familiar with the parameters of electronic devices that governs their performance and limitation.
3. To understand the tendency in contemporary microelectronics and principles of the nano-scale electronic devices.

UNIT I - BASICS OF SEMICONDUCTOR DEVICES  

UNIT II - QUANTITATIVE THEORY OF P-N JUNCTIONS  
Excess carrier decay and recombination, charge injection, continuity equation, quasi-Fermi level p-n junction: static behavior (depletion width, field profile), p-n junction under forward and reverse bias, current equations, generation-recombination current and reference to typical devices.

UNIT III - OXIDE LAYERS  
Zener and avalanche breakdown, Capacitance-voltage profiling, metal/semiconductor junction – Ohmic and Schottky contacts, reference to device applications. MOS capacitor, charge/field/energy bands, accumulation, inversion, C-V (high and low frequencies), deep depletion, Real MOS cap: Flat-band & threshold voltage, Si/SiO2 system.

UNIT IV - MOSFET AND HEMT  
MOSFET: structure and operating principle, derivation of I-V, gradual channel approximation, substrate bias effects, sub-threshold current and gate oxide breakdown. Control of threshold voltage, short channel effects. Moore’s Law and CMOS scaling Introduction to compound semiconductors & alloys, commonly used compound semiconductors, heterostructure band diagrams and basics of MODFET and HEMT, introduction to quantum well, applications of heterostructure device technologies.
UNIT V - BJT AND HBT (9 hours)
BJT: working principle, DC parameters and current components, base transport factor, Early Effect, charge control equation & current gain, need for HBT. Applications of BJTs/HBTs in real-life. (Basics of) - transistors for high-speed logic, transistors for high frequency (RF), transistors for high power switching, transistors for memories, transistors for low noise, transistors for the future.

REFERENCES

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<tbody>
<tr>
<td></td>
<td>GRAPH THEORY AND OPTIMIZATION TECHNIQUES</td>
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<td>Total Contact Hours - 45</td>
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PURPOSE
This course is aimed at providing graph theory and optimization techniques for use in VLSI design.

INSTRUCTIONAL OBJECTIVES
1. To impart a knowledge on basics of graph theory and its algorithms
2. To impart a knowledge on basic optimization techniques.
3. To impart a knowledge on various statistical methods in analyzing a sample.

UNIT–I: BASICS OF GRAPH THEORY (9 hours)

UNIT–II: CLASSES OF GRAPH (9 hours)
Eulerian graphs and Hamiltonian graphs - standard theorems- planar graphs- Euler’s formula – five color problem- coloring of graphs- chromatic number (vertex and edge) properties and examples- directed graphs

UNIT–III: GRAPH ALGORITHMS (9 hours)
Computer representation of graphs-Basic graph algorithms- minimal spanning tree algorithm - Kruskal and prim’s algorithm- shortest path algorithms- Dijsktra’s algorithm- DFS and BFS algorithms.
UNIT–IV: OPTIMIZATION TECHNIQUES (9 hours)
Linear programming- graphical methods- simplex method (Artificial variables not included) - transportation and assignment problems.

UNIT-V: STATISTICS (9 hours)

REFERENCES

EM2101
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<tr>
<th>COMPUTER ARCHITECTURE</th>
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<tr>
<td>Total Contact Hours – 45</td>
<td>3</td>
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PURPOSE
To introduce students with general concepts of computer architecture basics to enable them to use the processors effectively.

INSTRUCTIONAL OBJECTIVES
1. To familiarize with fundamentals of computer design.
2. To learn parallel and pipeline architectures.
3. To learn principles of parallel programming.

UNIT I - PROCESSOR AND MEMORY HIERARCHY (9 hours)

UNIT II - FUNDAMENTALS OF COMPUTER DESIGN (9 hours)

UNIT III - PARALLEL AND SCALABLE ARCHITECTURES (9 hours)
Techniques – Principles of Multithreading – Scalable and Multithreaded Architectures - The Tera Multiprocessor System.

UNIT IV - PIPELINING AND SUPER SCALAR TECHNIQUES  (9 hours)

UNIT V - SOFTWARE FOR PARALLEL PROGRAMMING  (9 hours)

REFERENCES

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<th>CO2105</th>
<th>ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN</th>
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<td>Total Contact Hours – 45</td>
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<td>Prerequisites : Nil</td>
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PURPOSE
The purpose of this course is to expose the students to the basics and fundamentals of Electromagnetic Interference and Compatibility in System Design.

INSTRUCTIONAL OBJECTIVES
At the end of the course, student should be able to know:
1. EMI Environment
2. EMI Coupling Principles
3. EMI Specification, Standards and Limits
4. EMI Measurements and Control Techniques
5. EMC Design of PCBs

UNIT I - INTRODUCTION AND SOURCES OF EMI  (9 hours)
EMI/ EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.
UNIT II - TYPES OF ELECTROMAGNETIC COUPLING (9 hours)
Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT III - EMI MEASUREMENTS (9 hours)
EMI Shielded Chamber, Open Area Test Site, TEM Cell, GTEM cell Sensors/ Injectors/ Couplers, LISN, voltage probe, Current probe Test beds for ESD and EFT.

UNIT IV - EMI MITIGATION TECHNIQUES (9 hours)
Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT V - EMC SYSTEM DESIGN (9 hours)

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</thead>
<tbody>
<tr>
<td>Career Advancement Course for Engineers -I</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>Total Contact Hours - 30</td>
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<td>Prerequisite: Nil</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PURPOSE
To enhance holistic development of students and improve their employability skills

INSTRUCTIONAL OBJECTIVES
1. To improve aptitude, problem solving skills and reasoning ability of the student.
2. To collectively solve problems in teams and group.
3. Understand the importance of verbal and written communication in the workplace.
4. Understand the significance of oral presentations, and when they may be used.
5. Practice verbal communication by making a technical presentation to the class.
6. Develop time management Skills.

UNIT I–BASIC NUMERACY: Types and Properties of Numbers, LCM, GCD, Fractions and decimals, Surds
UNIT II-ARITHMETIC – I: Percentages, Profit and Loss, Equations
UNIT III-REASONING – I: Logical Reasoning
UNIT IV-SOFT SKILLS – I: Presentation skills, E-mail Etiquette
UNIT V-SOFT SKILLS – II: Goal Setting and Prioritizing

ASSESSMENT

Soft Skills (Internal)
Assessment of presentation and writing skills.

Quantitative Aptitude (External)
- Objective Questions- 60 marks
- Descriptive case lets- 40 marks*
- Duration: 3 hours
*Engineering problems will be given as descriptive case lets.

REFERENCES
1. Quantitative Aptitude by Dinesh Khattar – Pearsons Publicaitons
2. Quantitative Aptitude and Reasoning by RV Praveen – EEE Publications
3. Quantitative Aptitude by Abijith Guha – TATA Mc GRAW Hill Publications
4. Soft Skills for Everyone by Jeff Butterfield – Cengage Learning India Private Limited
5. Six Thinking Hats is a book by Edward de Bono - Little Brown and Company
6. IBPS PO - CWE Success Master by Arihant - Arihant Publications(I) Pvt.Ltd - Meerut

<table>
<thead>
<tr>
<th>CAC2002</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Career Advancement Course for Engineers -II</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Total Contact Hours - 30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Prerequisite: CAC2001</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PURPOSE
To enhance holistic development of students and improve their employability skills

INSTRUCTIONAL OBJECTIVES
1. To improve aptitude, problem solving skills and reasoning ability of the student
2. To collectively solve problems in teams and group
3. Understand the importance of verbal communication in the workplace
4. Understand the significance of oral presentations, and when they may be used
5. Understand the fundamentals of listening and how one can present in a group discussion
6. Prepare or update resume according to the tips presented in class

UNIT-I: ARITHMETIC – II: Ratios and Proportions, Mixtures and Solutions
UNIT-II: MODERN MATHEMATICS: Sets and Functions, Data Interpretation, Data Sufficiency
UNIT-III: REASONING – II: Analytical Reasoning
UNIT-IV: COMMUNICATION – I: Group discussion, Personal interview
UNIT-V: COMMUNICATION – II: Verbal Reasoning test papers
ASSESSMENT

1. Communication (Internal)
   - Individuals are put through formal GD and personal interviews.
   - Comprehensive assessment of individuals’ performance in GD and PI will be carried out.

2. Quantitative Aptitude (External)
   - Objective Questions- 60 marks (30 Verbal +30 Quants)
   - Descriptive case lets- 40 marks*
   - Duration: 3 hours
   - *Engineering problems will be given as descriptive case lets.

REFERENCES

1. Quantitative Aptitude by Dinesh Khattar – Pearson Publicaitons
2. Quantitative Aptitude and Reasoning by RV Praveen – EEE Publications
3. Quantitative Aptitude by Abijith Guha – TATA Mc GRAW Hill Publications
4. General English for Competitive Examination by A.P. Bharadwaj – Pearson Educaiton
5. English for Competitive Examination by Showick Thorpe - Pearson Educaiton
6. IBPS PO - CWE Success Master by Arihant - Arihant Publications(I) Pvt.Ltd - Meerut
7. Verbal Ability for CAT by Sujith Kumar - Pearson India
8. Verbal Ability and Reading Comprehension by Arun Sharma - Tata McGraw - Hill Education

<table>
<thead>
<tr>
<th>CAC2003</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Career Advancement Course For Engineers - III</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Total Contact Hours - 30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Prerequisite: Nil</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PURPOSE
To develop professional skills abreast with contemporary teaching learning methodologies

INSTRUCTIONAL OBJECTIVES
At the end of the course the student will be able to

1. acquire knowledge on planning, preparing and designing a learning program
2. prepare effective learning resources for active practice sessions
3. facilitate active learning with new methodologies and approaches
4. create balanced assessment tools
5. hone teaching skills for further enrichment

UNIT-I: DESIGN
Planning and Preparing a learning program, Planning and Preparing a learning session

(2 hrs)

UNIT-II: PRACTICE
Facilitating active learning , Engaging learners

(2 hrs)

UNIT-III: ASSESSMENT
Assessing learner’s progress, Assessing learner’s achievement

(2 hrs)

UNIT-IV: HANDS ON TRAINING
Group activities – designing learning session, Designing teaching learning resources, Designing

(10 hrs)
assessment tools, Mock teaching session

UNIT-V: TEACHING IN ACTION  
Live teaching sessions, Assessments  

ASSESSMENT (Internal)  

Weightage:  
Design - 40%  
Practice – 40%  
Quiz – 10%  
Assessment – 10%  

REFERENCES  
1. Cambridge International Diploma for Teachers and Trainers Text book by Ian Barker - Foundation books  

<table>
<thead>
<tr>
<th>VL2047</th>
<th>SEMINAR</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
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</table>

Every student will be required to present a seminar talk on a topic approved by the Department. The Committee constituted by the Head of the Department will evaluate the presentation and will award the marks based on  
- Comprehensible arguments and organization.  
- Accessible delivery  
- Accessible visuals in support of arguments.  
- Question and Answers.

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<thead>
<tr>
<th>VL2049</th>
<th>PROJECT WORK – PHASE - I</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Total Contact Hours - 12</td>
<td>0</td>
<td>0</td>
<td>12</td>
<td>6</td>
</tr>
</tbody>
</table>

Student has to identify the faculty supervisor (Guide), topic, objectives, deliverables and work plan. The topic should be of advanced standing requiring use of knowledge from program core and be preferably hardware oriented. Students are evaluated on monthly basis, by conducting reviews by the department throughout the project period. Student has to submit a report describing his/her project work. End semester examination/ Viva-voce will be conducted by the Department.
Student has to continue the project work he/she was doing in phase –I. The Student will be evaluated with monthly reviews and an end semester examination / viva-voce. The students are encouraged to submit his/her project work in Conference/Journal and due weightage will be given in their evaluation.