ACADEMIC CURRICULA

POSTGRADUATE DEGREE PROGRAMMES

Master of Technology in VLSI Design

Two Years(Full-Time)

Learning Outcome Based Education

Choice Based Flexible Credit System

Academic Year

2020 - 2021

SRM
INSTITUTE OF SCIENCE & TECHNOLOGY
(Deemed to be University u/s 3 of UGC Act, 1956)

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Chengalpattu District 603203, Tamil Nadu, India

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M.Tech in VLSI Design (2020 Regulations)

1.	Department Vision Statement
Stmt - 1	*Department of ECE is dedicated to create and disseminate knowledge in the area of Electronics and Communication Engineering through internationally accredited educational process.*
Stmt - 2	*The Department will offer a unique learning experience to the students.*
Stmt - 3	*The Department is determined to prepare them as highly ethical and competent professionals, who in turn will work for the betterment of mankind through technology innovation and management.*

2.	Department Mission Statement
Stmt - 1	*Build an educational process that is well suited to local needs as well as satisfies the international accreditation requirements.*
Stmt - 2	*Attract the right people and retain them by building an environment that foster work freedom and empowerment.*
Stmt - 3	*With the right talent pool, create knowledge and disseminate get involved in collaborative research with reputed universities and produce competent graduants.*

3.	Program Education Objectives (PEO)
PEO - 1	*To provide the Graduates of VLSI design, knowledge in Analog, Digital Circuits and System Design , Design Automation, Hardware Design and Scripting Language*
PEO - 2	*To Practice VLSI design engineering in the design of high performance and low power system through the acquired knowledge, Skills and tools.*
PEO - 3	*To apply the electronics engineering foundation for success in Higher Studies/ Research, Technical careers in Industry, academia, Entrepreneurial and consultancy.*
PEO - 4	*To promote the development of Intellectual property through research in the specific area by means of high impact factor journal publication and patents.*
PEO - 5	*To prepare the graduate for Lifelong learning in order to adapt themselves for professional activities and to take the advantage of opportunities in their profession.*

4. Consistency of PEO's with Mission of the Department					
	Mission Stmt. - 1	Mission Stmt. - 2	Mission Stmt. - 3	Mission Stmt. - 4	Mission Stmt. - 5
PEO - 1	H	M	-	-	-
PEO - 2	M	-	H	-	-
PEO - 3	M	-	H	-	-
PEO - 4	-	-	H	-	-
PEO - 5	-	H	-	-	-

H – High Correlation, M – Medium Correlation, L – Low Correlation

5. Consistency of PEO's with Program Learning Outcomes (PLO)															
	Program Learning Outcomes (PLO)														
	1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.
PEO - 1	H	M	H	M	H	H	H	M	L	L	H	H	M	L	H
PEO - 2	H	M	H	H	H	H	M	M	H	M	M	M	H	M	H
PEO - 3	M	H	M	H	H	H	M	L	M	H	H	H	H	M	H
PEO - 4	M	M	H	H	H	H	H	M	H	M	M	M	H	M	M
PEO - 5	H	M	M	M	M	H	M	M	L	H	H	H	M	M	H

H – High Correlation, M – Medium Correlation, L – Low Correlation

6. Programme Structure (70 Total Credits)

1. Professional Core Courses (C)
(5 Courses)

Course Code	Course Title	Hours/Week L	T	P	C
20MAC507T	Applied Mathematics for VLSI	4	0	0	4
20ECC531J	Digital Systems Design Using HDL	3	0	2	4
20ECC532J	Solid State Devices and Modeling	3	0	2	4
20ECC533J	Analog Circuits and System Design	3	0	2	4
20ECC534J	VLSI Physical Design Automation	3	0	2	4
Total Learning Credits					**20**

2. Professional Elective Courses (E)
(4 Courses)

Course Code	Course Title	Hours/Week L	T	P	C
20ECE531T	Signal processing Techniques for VLSI	3	1	0	4
20ECE532T	Hardware Design and Scripting Language				
20ECE533T	Low-Power CMOS Circuit Design	3	1		
20ECE534T	Reconfigurable Computing Systems	3	1	0	4
20ECE535T	Cryptography and Hardware Security in VLSI	4	0		
20ECE536T	Process and Device Simulation using CAD	3	1		
20ECE537T	Diagnosis and Reliable Design of Digital Systems	3	1	0	4
20ECE538T	High Performance ASIC Design	4	0		
20ECE631T	Mixed Signal IC Design	3	1		
20ECE632T	Radio Frequency VLSI	3	1	0	4
20ECE633T	Machine Learning in VLSI	3	1		
Total Learning Credits					**16**

3. Skill Enhancement Courses(S)
(2 Courses)

Course Code	Course Title	Hours/Week L	T	P	C
20GNS501J	Research Publishing and Presenting Skills	*1*	*0*	*2*	*2*
20ECS500T	Research Methodology for Electronics and Communication Engineers	*3*	*0*	*0*	*3*
Total Learning Credits					**5**

4. Open Elective Courses (O)
(Any 1 Course)

Course Code	Course Title	Hours/Week L	T	P	C
20MBO601T	*Business Analytics*	*3*	*0*	*0*	*3*
20MEO601T	*Industrial Safety*	*3*	*0*	*0*	*3*
20MAO601T	*Operations Research*	*3*	*0*	*0*	*3*
20MBO602T	*Cost Management*	*3*	*0*	*0*	*3*
20NTO601T	*Composite Materials*	*3*	*0*	*0*	*3*
20CEO601T	*Waste to Energy*	*3*	*0*	*0*	*3*
20GNP620T	*Massive Open Online Courses (MOOC)*	*3*	*0*	*0*	*3*
Total Learning Credits					**3**

5. Project Work, Internship In Industry / Higher Technical Institutions(P)

Course Code	Course Title	Hours/Week L	T	P	C
20ECP601L	*Internship (4-6 weeks during 2nd sem vacation) Or*	-	-	-	*4*
20ECP602L	*Minor Project*	*0*	*0*	*8*	
20ECP603L	*Project Work Phase I*	*0*	*0*	*12*	*6*
20ECP604L	*Project Work Phase II*	*0*	*0*	*32*	*16*
Total Learning Credits					**26**

6. Audit Courses (A)
(Any 2 Courses)

Course Code	Course Title	Hours/Week L	T	P	C
20CEA501J	*Disaster Management*	*1*	*0*	*1*	*0*
20LEA501J	*Constitution of India*	*1*	*0*	*1*	*0*
20LEA502J	*Value Education*	*1*	*0*	*1*	*0*
20GNA501J	*Physical and Mental Health using Yoga*	*1*	*0*	*1*	*0*

7. Mandatory Courses (M)
(3 Courses)

Course Code	Course Title	Hours/Week L	T	P	C
20PDM501T	*Career Advancement for Engineers – I*	*1*	*0*	*1*	*0*
20PDM502T	*Career Advancement for Engineers – II*	*1*	*0*	*1*	*0*
20PDM601T	*Career Advancement for Engineers –III*	*1*	*0*	*1*	*0*

7. Implementation Plan

Semester - I

Code	Course Title	Hours/ Week			C
		L	T	P	
20MAC507T	Applied Mathematics for VLSI	4	0	0	4
20ECC531J	Digital Systems Design Using HDL	3	0	2	4
20ECC532J	Solid State Devices and Modeling	3	0	2	4
20ECE531T	Signal processing Techniques for VLSI	3	1	0	4
20ECE532T	Hardware Design and Scripting Language	3	1		
20GNS501J	*Research Publishing and Presenting Skills*	*1*	*0*	*2*	*2*
20PDM501T	*Career Advancement for Engineers – I*	*1*	*0*	*1*	*0*
	Audit Course - I	*1*	*0*	*1*	*0*
Total Learning Credits					18

Semester - II

Code	Course Title	Hours/ Week			C
		L	T	P	
20ECC533J	Analog Circuits and System Design	3	0	2	4
20ECC534J	VLSI Physical Design Automation	3	0	2	4
20ECE533T	Low-Power CMOS Circuit Design	3	1	0	4
20ECE534T	Reconfigurable Computing Systems	3	1		
20ECE535T	Cryptography and Hardware Security in VLSI	4	0		
20ECE536T	Process and Device Simulation using CAD	3	1	0	4
20ECE537T	Diagnosis and Reliable Design of Digital Systems	3	1		
20ECE538T	High Performance ASIC Design	4	0		
20ECS500T	*Research Methodology for Electronics and Communication Engineers*	*2*	*0*	*2*	*3*
20PDM502T	*Career Advancement for Engineers – II*	*1*	*0*	*1*	*0*
	Audit Course - II	*1*	*0*	*1*	*0*
Total Learning Credits					19

Semester - III

Code	Course Title	Hours/ Week			C
		L	T	P	
20ECE631T	Mixed Signal IC Design	3	1	0	4
20ECE632T	Radio Frequency VLSI	3	1		
20ECE633T	Machine Learning in VLSI	3	1		
	Open Elective	*3*	*0*	*0*	*3*
	MOOC	-	-	-	
20ECP601L	*Internship (4-6 weeks during 2nd Sem vacation)*	-	-	-	*4*
20ECP602L	*Minor Project*	*0*	*0*	*8*	*4*
20ECP603L	*Project Work Phase I*	*0*	*0*	*12*	*6*
20PDM603T	*Career Advancement for Engineers – III*	*1*	*0*	*1*	*0*
Total Learning Credits					17

Semester - IV

Code	Course Title	Hours/ Week			C
		L	T	P	
20ECP604L	*Project Work Phase II*	*0*	*0*	*32*	*16*
Total Learning Credits					16

8. Program Articulation Matrix

Course Code	Course Name	Programme Learning Outcomes														
		Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
20MAC507T	Applied Mathematics for VLSI	L	M	M	M	L	-	M	M	M	-	-	-	-	-	H
20ECC531J	Digital Systems Design Using HDL	H	H	H	-	H	H	-	-	-	-	-	-	-	-	H
20ECC532J	Solid State Devices and Modeling	-	H	-	H	-	-	H	-	-	-	-	-	-	-	-
20ECC533J	Analog Circuits and System Design	H	M	H	M	M	-	-	M	-	-	-	-	-	-	-
20ECC534J	VLSI Physical Design Automation	M	H	M	M	H	-	-	-	-	-	-	-	-	-	-
20ECE531T	Signal processing Techniques for VLSI	L	M	H	M	M	-	-	-	M	-	-	-	H	-	L
20ECE532T	Hardware Design and Scripting Language	L	H	-	H	H	-	-	-	H	-	-	-	H	-	-
20ECE533T	Low-Power CMOS Circuit Design	H	H	H		H	-	-	-	-	-	-	-	-	-	-
20ECE534T	Reconfigurable Computing Systems	H	H	H	H	H	-	-	-	-	-	-	-	-	-	H
20ECE535T	Cryptography and Hardware Security in VLSI	H	H	H	H	H	-	-	-	-	-	-	-	-	-	-
20ECE536T	Process and Device Simulation using CAD	H	-	H	-	-	-	-	-	-	-	-	-	-	-	H
20ECE537T	Diagnosis and Reliable Design of Digital Systems	H	H	H	H	H	-	M	-	-	-	-	-	-	-	H
20ECE538T	High Performance ASIC Design	L	M	H	M	M	-	-	-	M	-	-	-	H	-	L
20ECE631T	Mixed Signal IC Design	H	H	H	H	H	H	H	M	L	-	M	-	M	-	L
20ECE632T	Radio Frequency VLSI	H	H	H	H	M	M	H	M	M	-	L	-	L	-	-
20ECE633T	Machine Learning in VLSI	H	H	M	M	H	-	-	-	-	-	-	-	-	-	-
20ECE634T	Fundamentals of Solar Cell	H	H	H	H	-	-	H	-	-	-	-	-	-	-	-
20MAC5XXT	Applied Mathematics for Vlsi	L	M	L	-	M	-	-	M	M	-	-	-	-	-	H
20GNS501J	Research Publishing and Presenting Skills	L	H	H	M	M	-	L	H	M	-	H	-	L	-	M
20ECS500T	Research Methodology for Electronics and Communication Engineers	H	H	-	H	-	-	-	-	-	-	-	-	-	-	-
20ECP601L	Internship (4-6 weeks during 2nd sem vacation)	H	H	H	M	H	H	M	L	H	L	M	-	H	H	-
20ECP602L	Minor Project	H	H	H	M	H	H	M	L	H	L	M	-	H	-	-
20ECP603L	Project Work Phase I	H	H	H	M	H	H	M	L	H	L	M	L	H	L	H
20ECP604L	Project Work Phase II	H	H	H	M	H	H	M	L	H	L	M	L	H	L	H
	Program Average	H	H	H	M	H	H	M	M	M	L	M	L	H	L	M

H – High Correlation, M – Medium Correlation, L – Low Correlation

Course Code	20ECC531J	Course Name	DIGITAL SYSTEMS DESIGN USING HDL	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engg	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1 :	To understand behavioral and RTL modeling of digital circuits
CLR-2 :	To understand the basic CMOS circuit, characteristics and performance.
CLR-3 :	To learn the designing of combinational circuits using different CMOS logic
CLR-4 :	To learn the designing of sequential circuits and FSM
CLR-5 :	To get an idea about designing datapath and memory systems and how to implement such design
CLR-6 :	To learn the trends in digital circuit design, characterstic of MOSFET, power dissipation, design of circuit using various CMOS logic and subsystem.

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	model digital systems in verilog HDL at different levels of abstraction	3	80	70	H	H	H	H	M	-		-	-	-	-	-	-	-	H
CLO-2 :	Understand the basic CMOS circuit, characteristics and performance.	3	85	80	H	-	-	L	L	-		-	-	-	-	-	-	-	H
CLO-3 :	summarize circuit design of combinational circuits using different CMOS logic	3	75	70	H	H	H	M	M	-		-	-	-	-	-	-	-	H
CLO-4 :	summarize circuit design of latches ,flip-flops and FSM	3	80	75	H	H	H	M	M	-		-	-	-	-	-	-	-	H
CLO-5 :	summarize various optimization methods , circuit design of datapath and memory sysyem	3	85	80	H	H	H	M	M	-		-	-	-	-	-	-	-	H
CLO-6 :	Understand the digital circuit design using various CMOS logic,characterstic of MOSFET,power dissipation and subsystem design	3	85	80	H	H	H	H	H	-		-	-	-	-	-	-	-	H

Duration (hour)		Basic Concepts - Verilog	Principle of MOS Tranistors and CMOS inverter	CMOS – Combinational Circuits	CMOS – Sequential Circuits	Datapath and Memory System Design
		15	15	15	15	15
S-1	SLO-1	Basic concepts, Identifiers, Value set	MOS transistors	Static CMOS design	Timing metrics for sequential circuit	Adder –carry select adder
	SLO-2	Data types,Parameters, Operands	Threshold voltage	complementary CMOS	latches Vs registers -static latches and registers Bistability principle	Adder –carry save adder
S-2	SLO-1	Operators, Modules and ports	characteristics of MOS transistor	static properties	multiplexer based latches	Multiplier –Baugh-Wooley
	SLO-2	Gate-level Modeling	Derivation of Drain Current	complementary CMOS design	master slave edge triggered registers	Multiplier – Wallace Tree
S-3	SLO-1	Behavioral Modeling	short channel effects	Power consumption in CMOS logic gates	non-ideal clock signals	Booth Multiplier
	SLO-2	**Design example**	short channel effects	dynamic or glitching transitions	low voltage static latches-static SR flip flop	Analyze the performance of the multiplier
S 4-5	SLO-1	Design and simulate Adders and subtractor circuit	Design and verify circuit using Switch level modeling	Design and implement Booth Multiplier	Design and simulate Multiplier – Wallace Tree	Design and simulate Universal Shift Register
	SLO-2					
S-6	SLO-1	Tri state gates, MOS Switches, Bidirectional switches	Transfer characteristics of CMOS inverter	Design techniques to reduce switching activity	Dynamic latches and registers	Register Files
	SLO-2	Switch level modeling	Transfer characteristics of CMOS inverter	Radioed logic-DC VSL - pass transistor logic	C^2MOS register	FIFOs
S-7	SLO-1	Combinational UDP	Design of Logic gates circuit using NMOS	Differential pass transistor logic	Dual edge registers-	Universal Shift Register
	SLO-2	**Design example**	Design of Logic gates using PMOS	Design using Differential pass transistor logic	True single phase clocked registers	Barrel Shifter
S-8	SLO-1	Sequential UDP and design	Design of Logic gates using CMOS	Sizing of level restorer	pipelining to optimize sequential circuit	Memory – RAM Static RAM

	SLO-2	**Design example**	Design of circuit using CMOS	-Sizing in pass transistor-Dynamic CMOS design	pipelining to optimize sequential circuit	Memory – RAM Static RAM
S 9-10	**SLO-1**	Design and verify Circuit using UDP	Design and verify Sequential circuits	Design and simulate FSM design	Design and verify pipelined based circuit	Design and simulate memory circuits
	SLO-2					
S- 11	**SLO-1**	System task	Stick diagrams	Basic principles - Domino logic optimization of Domino logic	latch Vs register based pipelines non-Bistable sequential circuit	Dynamic RAM Serial Access Memory – ROM
	SLO-2	System functions	Stick diagrams example			
S-12	**SLO-1**	Introduction to synthesis	Power dissipation	NPCMOS-logic style selection	Schmitt trigger-mono stable	Content Addressable Memory
	SLO-2	Verilog HDL synthesis	CMOS Power dissipation		Astable -sequential circuit	Content Addressable Memory
S 13	**SLO-1**	Synthesis Design flow	Delay	Designing logic for reduced supply voltages	choosing a clocking strategy Problem Solving	Finite-State Machines
	SLO-2		Delay and sizing of inverters	Design and analyze low power circuit	Design circuit using pipeline concept	Types of Finite-State Machines
S 14-15	**SLO-1**	Design and Implementation using task and function.	Design and simulate Sequential circuits	Design and verify ALU design	Design and implement Fir Filter/ Fir Filter With Pipelinig	Design a traffic light controller for an intersection with a main street, a side street, and a pedestrian crossing or a Vending Machine
	SLO-2					

Learning Resources	1. Samir palnitkar, "Verilog HDL", Pearson education, Second Edition,20O3. 2. Jan.M.Rabaey., Anitha Chandrakasan Borivoje Nikolic, "Digital Integrated Circuits", Second Edition 3. Michael D. Ciletti,Advanced Digital Design with Verilog HDL, Second Edition, Pearson,2011.	4. Neil H.E Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Addition Wesley, 1998. 5. Sung Mu Kang, Yusuf Leblebici "CMOS Digital Integrated Circuits", 3rd edition, Tata McGraw-Hill, 2002.

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	15	15	15	15	15	15	15	15
Level 2	Apply Analyze	20	20	20	20	20	20	20	20
Level 3	Evaluate Create	15	15	15	15	15	15	15	15
	Total	100 %		100 %		100 %		100 %	

 # CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	*Internal Experts*
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	1. Dr. V. Sarada, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	

Course Code	20ECC532J	Course Name	SOLID STATE DEVICES AND MODELING	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engg	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Identify the basic concept of quantum mechanics			
CLR-2 :	Identify the applications of quantum mechanics in devices			
CLR-3 :	Identify the applications of optical devices			
CLR-4 :	Create insights to the concepts nano and optical devices			
CLR-5 :	Analyze the working principle of homo and hetero junctions			
CLR-6 :	Utilize the concepts in physics for the understanding of VLSI technology			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Identify the principle of Schrodinger's Wave Equation	2	80	70	H	H	-	-	-	-	-	-	-	-	-	-	-	-	H
CLO-2 :	Analyze the concept of energy band diagram	2	85	75	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CLO-3 :	Apply quantum theory to semiconductors and model it for CAD tools	2	75	70	H	H	-	H	-	-	-	-	-	-	-	-	-	-	-
CLO-4 :	Apply physical effects in PN Junctions and model it using CAD tools	2	85	80	H	H	-	-	-	-	-	-	-	-	-	-	-	-	-
CLO-5 :	Identify the basic concepts used in MOSFET and design it using CAD tools	2	85	75	H	-	H	-	-	-	-	-	-	-	-	-	-	-	-
CLO-6 :	Apply the concepts of quantum physics in optical devices	2	80	70	-	H	-	H	-	-	H	-	-	-	-	-	-	-	H

Duration (hour)		Introduction to Quantum Mechanics (15 Hours)	Unit-II: Semiconductor in Equilibrium and Non-equilibrium (15 Hours)	Unit-III: The P-N and Metal Semiconductor Junction (15 Hours)	Unit-IV: Metal Insulator Semiconductor Devices (15 Hours)	Unit-V: Optical Devices (15 Hours)
S-1	SLO-1	Principles of Quantum Mechanics &Energy Quanta	Charge Carriers in Semiconductors	Basic Structure of the PN Junction	Energy-Band Diagrams	Optical Absorption
	SLO-2	Wave-Particle Duality	Equilibrium Distribution of Electrons and Holes	Built-in Potential Barrier at zero bias	Depletion Layer Thickness	Photon Absorption Coefficient
S-2	SLO-1	Schrodinger's Wave Equation	The n_o and p_o, Equations	Electric Field at zero bias	Work Function Differences	The PN Junction Solar Cell
	SLO-2	Physical Meaning of the Wave Function	The Intrinsic Carrier Concentration & The Intrinsic Fermi-Level Position	Problem Solving	Problem Solving	The Heterojunction Solar Cell
S-3	SLO-1	Applications of Schrodinger's Wave Equation	The Extrinsic Semiconductor	Space charge width at zero bias	Threshold Voltage	Amorphous Silicon Solar Cells
	SLO-2	Electron in Free Space	Equilibrium Distribution of Electrons and Holes	Reverse Applied Bias	Flat-Band Voltage	Problem Solving
S 4-5	SLO-1	Lab 1: Introduction to CAD Tool	Lab 4: Learning to Design Doping and Meshing	Lab 7: Learning to Design 2D PN-Junction Structure	Lab 10: Learning to Design 2D MOSFET Structure	**Lab 13:** Design and Analyze DC and AC Characteristics of **N-Type lightly doped drain (LDD) MOSFET**
	SLO-2					
S-6	SLO-1	The Infinite Potential Well	The $n_o p_o$, Product	Space Charge Width and Electric Field at reverse bias	Capacitance-Voltage Characteristics	Photodetectors
	SLO-2	Allowed and Forbidden Energy Bands	The Fermii-Dirac Integral	Nonuniformly Doped Junctions	Problem Solving	PIN Photodiode
S-7	SLO-1	The Kronig-Penney Model	Position of Fermi Energy Level	One-Sided Junctions	Ideal C-V Characteristics	Avalanche Photodiode
	SLO-2	The k-Space Diagram	Degenerate and Nondegenerate	Problem Solving	Problem Solving	Problem Solving

			Semiconductors			
S-8	SLO-1	The Energy Band and	Carrier Generation	Linearly Graded Junction	Frequency Effects	Photoluminescence
	SLO-2	The Band Model		Hyperabrupt Junctions	Problem Solving	Applications of Photoluminescence
S 9-10	SLO-1	Lab 2: Learning to Design 2D Boundaries	Lab 5: Learning to Design 3D Structure using CAD Tool	Lab 8: Learning the overview of Sentaurus Workbench and Device Physics	Lab 11: Design and Analyze DC and AC Characteristics of MOSFET using Workbench	Lab 14: Learning to Design 3D MOSFET Structure
	SLO-2					
S-11	SLO-1	Drift Current	Carrier Recombination	PN Junction Current	The Basic MOSFET Operation	Electroluminescence
	SLO-2	Problem Solving	Problem Solving	Problem Solving	Problem Solving	Problem Solving
S-12	SLO-1	Electron Effective Mass	Characteristics of Excess Carriers	The Schottky Barrier Diode ts	Nonideal Effects	Light Emitting Diodes
	SLO-2	Problem Solving	Problem Solving		Problem Solving	Applications of LED
S-13	SLO-1	Concept of the Hole	Ambipolar Transport	Metal-Semiconductor Ohmic Contac	Radiation and Hot-Electron Effects	Generation of Light
	SLO-2	Problem Solving	Problem Solving	Problem Solving	Problem Solving	Problem Solving
S 14-15	SLO-1	Lab 3: Learning to Design 2D Structures	Lab 6: Designing Process simulation using CAD workbench	Lab 9: Design and Analyze Characteristics of PN Junction using Workbench	Lab 12: Learn to Design 2D N-Type lightly doped drain (LDD) MOSFET using Workbench	Lab 15: Design and Analyze DC and AC Characteristics of 3D MOSFET using Workbench
	SLO-2					

Learning Resources	1. Donald Neamen, Dhrubesh Biswas, Semiconductor Physics and Devices, McGraw Hill, 4th ed, 2012 2. S. M. Sze, Physics of Semiconductor Devices, John Wiley, 3rd ed, 2005 3. Pallab Bhattacharya, Semiconductor Opto electronics Devices, 2nd ed, PHI, 2017	4. Nandita Dasgupta and Amitav Dasgupta , Semiconductor Devices : Modelling and Technology Prentice-Hall of India Pvt.Ltd; 1st ed, 2004 5. Sentaurus Device user guide, Synopsys, 2015

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)				Final Examination (50% weightage)
		CLA – 1 (10%)	CLA – 2 (15%)	CLA – 3 (15%)	CLA – 4 (10%)#	
		Theory	Theory	Theory	Theory	Theory
Level 1	Remember	40%	40%	40%	40%	30%
	Understand					
Level 2	Apply	40%	40%	40%	40%	40%
	Analyze					
Level 3	Evaluate	20%	20%	20%	20%	30%
	Create					
	Total	100 %	100 %	100 %	100 %	100 %

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	1. Dr. Soumyaranjan Routray, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	2. Dr. Maria Jossy, SRMIST
3.	3.	3. Dr. P. Aruna Priya, SRMIST

Course Code	20ECC533J	Course Name	ANALOG CIRCUITS AND SYSTEM DESIGN	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Utilize basics of analog CMOS sub-circuits and its design			
CLR-2 :	Understand the operation and design of different MOS amplifier circuits			
CLR-3 :	Characterize the basics of differential amplifier and knowledge of various operational amplifiers			
CLR-4 :	Understand and analyze the different oscillator circuits to determine the frequency of oscillation			
CLR-5 :	Identify the various components of PLL and its operation			
CLR-6 :	Gain hands-on experience to put theoretical concepts learned in the course to practice			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Understand the operation of CMOS current mirrors, biasing circuits and filters	3	80	70	H	M	H	M	M	-	-	M	L	-	-	-	-	-	-
CLO-2 :	Analyze and design of MOS amplifier circuits under various load and understand the frequency response	3	85	80	H	M	H	M	M	-	-	M	L	-	-	-	-	-	-
CLO-3 :	Design basic differential and operational amplifier	3	80	70	H	M	H	M	M	-	-	M	L	-	-	-	-	-	-
CLO-4 :	Elucidate and design oscillator circuits to meet certain specifications	3	80	70	H	M	H	M	M	-	-	M	L	-	-	-	-	-	-
CLO-5 :	Illustrate the function of PLL and its performance	3	85	80	H	M	H	M	M	-	-	M	L	-	-	-	-	-	-
CLO-6 :	Analyze and design analog CMOS circuits and systems and compare experimental results in the laboratory with theoretical analysis	3	85	75	H	M	H	M	M	-	-	M	L	-	-	-	-	-	-

Duration (hour)		Current Sources & Current Mirror 15	CMOS Amplifiers 15	Differential amplifier 15	Operational Amplifier 15	Oscillators & Phase Locked Loops 15
S-1	SLO-1	Passive current mirrors	Analog Design Process flow, Analog Design Octagon	Single-ended operation	Performance parameters of op-amp	Ring oscillator
	SLO-2	Active current mirrors	Performance parameters	Significance of Differential operation	Block Diagram of Op-amp	Two stage and three stage ring oscillator
S-2	SLO-1	Basic Current mirror	Common source Amplifier: Resistive load,	Basic differential pair	one stage op-amp	LC oscillators: Colpitt
	SLO-2	Matching considerations in current mirrors	Diode connected load	Qualitative analysis of differential amplifier	Telescopic op-amp	Cross coupled oscillator
S-3	SLO-1	Cascode current mirrors	Common source Amplifier: Current-source load, triode load	Quantitative analysis	Two Stage op-amp	Voltage controlled oscillators
	SLO-2	Problem solving on basic current mirror	Common source amplifier with source degeneration	Problems on Differential amplifier	Input common range and output swing	Tuning range of VCOs
S 4-5	SLO-1	Lab 1: Simulation of Basic current mirror, Cascode Current mirror.	Lab 4: Simulation of Common source amplifiers with different loads	Lab 7: Simulation of Differential amplifiers	Lab 10: Simulation of Ring Oscillators	Lab 13: Simulation of Phase detector
	SLO-2					
S-6	SLO-1	Problem solving on cascode mirror	Source Follower	Common-mode response	Voltage gain of two stage op-amp	**Phase Locked Loop:** Basic PLL topology & Characteristic parameters
	SLO-2	**Reference circuits:** Performance Parameters	Common Gate amplifier	CMRR - Derivation	Frequency response of op-amp	Phase detector
S-7	SLO-1	Voltage reference circuits using Resistor & BJT	Noise in CS amplifiers	Differential pair with MOS loads	Slew rate	Charge Pump PLL
	SLO-2	Voltage reference circuits using MOS transistor	Noise in CD amplifiers	Problem solving on common mode response	Power supply rejection ratio	Problem of lock acquisition
S-8	SLO-1	Voltage reference circuits using Zener diode	Noise in CG amplifiers	Frequency response of Differential amplifier	Gain Boosting	Non ideal effects in PLL: PFD/CP

	SLO-2	*Problem solving on Voltage reference circuits*	*Cascode Amplifier*	*Frequency response of Differential amplifier-Continuation*	*Problem solving on Op-amp*	*Jitter in PLLs*
S 9-10	**SLO-1**	*Lab 2: Simulation of Voltage Reference circuits*	*Lab 5: Simulation of source follower*	*Lab 8: Simulation of one stage operational amplifier*	*Lab 11: Simulation of Cross-coupled Oscillators*	*Lab 14: Simulation of VCO*
	SLO-2					
S-11	**SLO-1**	*Band gap reference circuits: Block Diagram*	*Folded Cascode amplifier*	*Analysis of Resistively loaded differential amplifier*	*Folded Cascode CMOS op-amp*	*Transient response of PLL in the locked state*
	SLO-2	*Supply Independent Biasing*	*Noise in Cascode stage*	*Active- loaded MOS amplifier*	*Voltage gain and frequency response of folded cascode*	*Problem solving on PLLs*
S-12	SLO-1	*Temperature independent Reference circuit*	*Frequency response of CS amplifier*	*Noise in differential amplifier*	*Rail to rail input operation*	*Delay Locked Loops*
	SLO-2	*Constant –Gm biasing*	*Frequency response of CD amplifier*	*Noise in differential amplifier-continuation*	*Wide swing current mirror - topology*	*Delay Locked Loops-Continuation*
S-13	SLO-1	*Problem solving on Band gap reference circuits*	*Frequency response of CG amplifier*	*Problem Solving on frequency response of differential amplifier*	*Noise in op-amps*	*Applications of PLL : Frequency multiplication*
	SLO-2	*Problem solving on Band gap reference circuits*	*Frequency response of Cascode amplifier*	*Problem Solving on noise in differential amplifier*	*Problem Solving on folded cascade op-amp*	*Skew reduction and jitter reduction*
S 14-15	SLO-1	*Lab 3: Simulation of Band gap reference circuit*	*Lab 6: Simulation of Common gate amplifier*	*Lab 9: Simulation of two stage operational amplifier*	*Lab 12: Simulation of Colpitts Oscillators*	*Lab 15: Simulation of PLL*
	SLO-2					

Learning Resources	1. Allen, Holberg, "CMOS analog circuit design", 3rd Edition, Oxford University Press, 2004. 2. Behzad Razavi, "Design of analog CMOS integrated circuits", 2nd Edition, McGraw Hill, 2017.	3. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog Integrated Circuits", 5th Edition, Willey International, 2009. 4. Adel S. Sedra, Kenneth C. Smith, **"Microelectronic Circuits"** 7th Edition, Oxford University Press,2015

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	15	15	15	15	15	15	15	15
	Understand								
Level 2	Apply	20	20	20	20	20	20	20	20
	Analyze								
Level 3	Evaluate	15	15	15	15	15	15	15	15
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr .J .Manjula, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Mrs. Ferents Koni Jiavana, SRMIST*

Course Code	20ECC534J	Course Name	VLSI Physical design Automation	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	understand all the graph theory concepts required for physical design of a VLSI system IC			
CLR-2 :	Learn the methods involved in partitioning and clustering of a design layout			
CLR-3 :	Learn the representation used in Floorplanning and Placement process			
CLR-4 :	Describe the Routing algorithms and Timing Analysis			
CLR-5 :	Gain knowledge of practical physical design issues on physical layout			
CLR-6 :	Learn and understand the design challenges in VLSI physical design automation			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Utilize mathematical tools for physical design problems	3	80	70	H	H	H	H	H	-	-	-	-	-	-	-	-	-	-
CLO-2 :	Expose to hierarchical modeling concepts and the necessary knowledge to perform partitioning and clustering algorithms.	3	80	70	H	H	H	H	H	-	-	-	-	-	-	-	-	-	-
CLO-3 :	To design a compact IC using floorplanning and placement methodologies	3	70	65	M	H	H	H	H	-	-	-	-	-	-	-	-	-	-
CLO-4 :	Analyze the routing process to achieve the performance of the digital design	3	70	65	M	H	L	M	H	-	-	-	-	-	-	-	-	-	-
CLO-5 :	Design performance aware VLSI layout	3	80	70	M	H	L	M	H	-	-	-	-	-	-	-	-	-	-
CLO-6 :	Understand and develop physical design algorithms in optimization of VLSI layout	3	70	65	M	H	M	M	H	-	-	-	-	-	-	-	-	-	-

Duration (hour)		Data Structures And Basic Algorithms 15	Partitioning And Clustering 15	Floorplanning And Placement 15	Routing And Compaction 15	Practical Design Issues 15
S-1	SLO-1	VLSI Physical design flow	Introduction to Partitioning	Introduction to Floorplanning	Global Routing	Elmore Delay based routing constructions
	SLO-2	Challenges in VLSI design flow	Types of Partitioning	Floorplanning problem formulation and classification	Problem Formulation	Examples on Elmore delay
S-2	SLO-1	Basic Graph theory	Metrics of Partitioning	Floorplan topologies	Classification of Global Routing	Non- Hunan Interconnect synthesis
	SLO-2	Complexity analysis	Metrics of Clustering	Metrics of Floorplanning	Maze routing algorithm	Optimization of Non- Hunan
S-3	SLO-1	Complexity issues	Mathematical Partitioning Formulations	Floorplan slicing methods	Lee's algorithm	Wire-sizing
	SLO-2	Analysis in NP hardness	Introduction to Move-based partitioning algorithms	Algorithms for Slicing floorplan	Line Probe algorithms	Non-tree routing
S 4-5	SLO-1	Lab 1:Functional verification of a combinational circuit using GPDK library.	Lab 4:Implementation of KL algorithm in EDA environment.	Lab 7: Implementation of Non-slicing (B tree) floorplan in EDA environment	Lab 10:Static timing analysis - Placement of standard cells and sizing to achieve positive WNS.	Lab 13:Generation of Clock tree for a target skew using Van Ginneken's Algorithm.
	SLO-2					
S-6	SLO-1	Graph search algorithms	KL algorithm	Floorplan representation: Corner block list	Shortest Path algorithms: Steiner Tree based algorithms	Van Ginneken's algorithm
	SLO-2	Spanning tree algorithms	Problems in KL algorithm	Problems in Corner block list	Separability Based Algorithm	Optimization of Van Ginneken's algorithm
S-7	SLO-1	Shortest path algorithms	FM Algorithm	Non-slicing methods: O-tree	Detailed Routing:Problem formulation	Two phase approach and buffer aware tree construction: C algorithm
	SLO-2	Min- cut and max-cut algorithms, and Steiner tree algorithms	Problems in FM algorithm	Problems in O-tree	Classification of Detailed routing	Buffer aware tree generation
S-8	SLO-1	Computational Geometry Algorithms: Line sweep	Challenges in Clustering	Non-slicing methods: B-tree	Single layer routing	Buffered path with blockage avoidance: Dynamic programming approach
	SLO-2	Extended line sweep	Hierarchical Clustering	Problems in B-tree	Single row routing	Buffered path with blockage avoidance:

						Graph-based approach
S 9-10	SLO-1	Lab 2:Functional verification of a sequential circuit using GPDK library.	Lab 5: Implementation of FM algorithm in EDA environment.	Lab 8: Implementation of Non-slicing O-tree floorplan in EDA environment	Lab 11: Analysis on effect of useful skew-based placement.	Lab 14: Generation of Clock tree for a target skew.
	SLO-2					
S-11	SLO-1	Basic Graph Structures: Atomic operations of Layout Editors	Agglomerative Clustering	Introduction to Placement	Two-layer channel routing algorithms: Left Edge algorithm	Buffered tree with blockage avoidance: Tree adjustment and simultaneous tree and buffer insertion approach
	SLO-2	Basic Graph Structures: Linked list of blocks	Rajaraman and Wong algorithm	Problem formulation and classification	Dogleg Routing algorithm	Buffered tree with blockage avoidance: Dynamic programming, and Graph-based approach
S-12	SLO-1	Basic Graph Structures: Bin-based, and Neighbor pointers	Introduction: Multi-level coarsening algorithm-Edge coarsening	Top –down partition-based placement frame work	Clock routing schemes: H-tree based algorithm	Routabilty driven buffer planning
	SLO-2	Corner Stitching: Introduction	Hyperedge coarsening	Enhancement of Min- cut placement	Compaction: Classification and constraint-based compaction	Noise aware buffer planning
S-13	SLO-1	Atomic operations using Corner stitching	Modified Hyperedge coarsening	Placement algorithm using Simulated annealing	Virtual grid-based compaction and recent trend in Compaction	Flip flop and buffer planning
	SLO-2	Graph problems in Physical design	Practice problems in Clustering	Placement algorithm using Genetic algorithm	3/2 and 2D Compaction	Physical design in 3D circuits
S 14-15	SLO-1	Lab 3:Generate RTL netlist for a digital circuit and analyze the performance.	Lab 6: Placement of Standard cells and timing report generation.	Lab 9: IR drop analysis in pre-placement stage.	Lab 12: IR drop analysis in post-placement stage.	Lab 15: H-tree based Clock tree synthesis for a target skew.
	SLO-2					

Learning Resources	1. Naveed Sherwani, Algorithms for VLSI physical design Automation, Kluwer Academic Publishers, 2010. 2. Sung Kyu Lim, "Practice Problems in VLSI physical design Automation",Springer, 2008	3. Charles J . Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, "Hand book of algorithms of Physical design Automation ", CRC press, 2009. 4. Sadiq M .Sait, Habib Youssef, "VLSI Physical design automation theory and Practice", World Scientific Publishing, 1999

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	15	15	15	15	15	15	15	15
	Understand								
Level 2	Apply	20	20	20	20	20	20	20	20
	Analyze								
Level 3	Evaluate	15	15	15	15	15	15	15	15
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. B. Srinath, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Dr. E. Chitra, SRMIST*

Course Code	20ECE531T	Course Name	SIGNAL PROCESSING TECHNIQUES FOR VLSI	Course Category	E	*Professional Elective*	L	T	P	C
							3	1	0	4

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes/Standards**		*Nil*	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	**Learning**		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	*To Understand the basic computation item in VLSI Signal Processing*			
CLR-2 :	*Be Familiar with concepts of Iteration Bound, Retiming, Folding*			
CLR-3 :	*To Understand the Design Efficient Pipelining filter design*			
CLR-4 :	*To learn the concept of parallel processing of FIR filter for low power design*			
CLR-5 :	*To understand the concept of Bit –level arithmetic architectures*			
CLR-6 :	*To learn the concepts of low power design aspects in VLSI DSP*			

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	**Learning**			**Program Learning Outcomes (PLO)**													
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Understand VLSI design methodology for signal processing systems.	*2*	*80*	*50*	*M*												*H*		
CLO-2 :	Be familiar with VLSI algorithms and architectures for DSP.	*3*	*99*	*70*		*H*	*H*		*M*				*M*				*H*		
CLO-3 :	Be able to implement basic architectures for DSP using CAD tools.	*2*	*80*	*70*					*M*								*H*		
CLO-4 :	Able to design the pipelined and parallel FIR Filter	*3*	*90*	*70*			*H*	*M*	*M*				***M***				*H*		
CLO-5 :	Be familiar with low power design concepts of ASICs	*2*	*90*	*85*	*L*	*L*			*L*										*M*
CLO-6 :	Understand the High speed Design	*2*	*90*	*70*	*L*	*M*	*H*	*M*	*M*				***M***				*H*		*L*

Duration (hour)		**Introduction to DSP Systems**	**Systolic Architecture and Algorithm Strength Reduction**	**Fast Convolution**	**Bit-Level Arithmetic Architectures**	**High Performance Algorithm for ASIC/Socs**
		12	**12**	**12**	**12**	**12**
S-1	SLO-1	Iteration Bound	Algorithmic strength reduction in filters.	Fast convolution – Cook-Toom algorithm	Scaling and round-off noise	Numerical Strength Reduction
	SLO-2	data flow graph representations,	Transforms.	Problem	scaling operation, round-off noise	sub -expression elimination
S-2	SLO-1	loop bound	2-parallel FIR filter	modified Cook-Took algorithm	state variable description of digital filters	multiple constant multiplications
	SLO-2	Iteration bound.	2-parallel fast FIR filter	problem	scaling and round-off noise computation	iterative matching
S-3	**SLO-1**	Problems on iteration bound techniques	DCT algorithm architecture transformation	Pipelined and parallel recursive and adaptive filters	Round-off noise in pipelined first-order filters.	Linear transformations
	SLO-2					
S-4	SLO-1	Various mechanism for iteration bound computation	parallel architectures for rank-order filters	inefficient/efficient single channel interleaving	Problems on round-off noise computation	Low power Design
	SLO-2	Longest path matrix algorithm	Odd- Even Merge- Sort architecture	Parallel recursive structures	Problems on round-off noise computation	Low power design techniques
S-5	SLO-1	Problems on LPM techniques	parallel rank-order filters	Interleaving mechanism	Bit-Level Arithmetic Architectures- parallel multipliers with sign extension,	Introduction to wave pipelining, asynchronous pipelining bundled data versus dual rail protocol
	SLO-2	Pipelining and parallel processing - Introduction	Parallel rank order filter design	Look-ahead pipelining in first order IIR filters	parallel carry-ripple array multipliers	Wave pipelining in detail
S-6	**SLO-1**	Pipelining of FIR digital filters, parallel processing .	Problems related to ODD-EVEN Merge sort algorithm	Problems on look-ahead techniques	parallel carry-save multiplier tabular form and implementation	Asynchronous pipelining- Introduction
	SLO-2	Parallel processing of FIR Filter.	Problem on rank order filter	Problems on look-ahead techniques	4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation	Detail description on asynchronous pipelining

S-7	SLO-1	Pipelining processing for low power	Problem on ODD-EVEN merge sort	Problems on interleaving	Operation description of parallel carry save	Asynchronous pipelining mechanism
	SLO-2	Parallel processing for low power	Systolic Architecture Design: Introduction,	Problem on parallel recursive structure	Problem on bit-level arithmetic	Data Vs Dual Rail Protocol
S-8	SLO-1	Problems on low power pipelined and parallel systems	Systolic Array Design Methodology introduction	Application of Look-ahead pipelining	Application on carry save multiplication	needs for low power VLSI chips, charging and discharging capacitance
	SLO-2	Introduction to Retiming – Retiming Properties	FIR Systolic Arrays	Clustered Look-Ahead pipelining	Application study on carry save multiplication	needs for low power VLSI chips, charging and discharging capacitance
S-9	SLO-1	Problems on Retiming mechanism	Sample problems on FIR Systolic arrays	parallel processing of IIR filters	design of Lyon's bit-serial multipliers using Horner's rule	CMOS leakage current
	SLO-2	Unfolding – algorithm in detail	Selection of Scheduling Vector	parallel processing of IIR filters	Problems based on HORNER's Rule	Basic principles of low power design.
S-10	SLO-1	Properties of unfolding	Problem related to systolic array design	combined pipelining	bit-serial FIR filter architecture	short-circuit current of an inverter
	SLO-2	Problems on unfolding techniques	Matrix Multiplication	parallel processing of IIR filters	Problem related to bit-serial architecture	DAA and computation of FFT and DCT
S-11	SLO-1	Sample period Reduction techniques	2D Systolic Array Design	pipelined adaptive digital filters	CSD multiplication using Horner"s rule for precision improvement	Problems on power dissipation
	SLO-2	Problems on sample period reduction	Problem	Problem on adaptive digital filters	Problem on CSD multiplication	High performance filters using delta-sigma modulators
S-12	SLO-1	Parallel processing types	HDL Code for 2-parallel FIR Filter	relaxed look-ahead technique	HDL Code for bit-serial FIR filter.	Case Studies: High Speed Data standards
	SLO-2	Parallel processing standards	HDL Code for 2-parallel fast FIR Filter	Sample problem on relaxed look-ahead filter	HDL code for bit serial Fir Filter	High speed data standard application

Learning Resources	1. Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999. 2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998. 3. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.	4. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985. 5. Jose E. France, Yannis Tsividis, "Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Mr. Anuj Kumar, Bombardier* Transportation, Ahmedabad, *kumaranuj.anii@gmail.com*	1. *Dr. Meenakshi, Professor* of ECE, CEG, Anna University, *meena68@annauniv.edu*	*1. Dr. J.Selvakumar, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Mr.S.Prithiviraj, SRMIST*

Course Code	20ECE532T	Course Name	Hardware Design and Scripting Language	Course Category	E	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLR-1 :	Understand the basic features of System C..																		
CLR-2 :	Construct the different types of Digital system in System C																		
CLR-3 :	Utilize the basic constructs of System Verilog.																		
CLR-4 :	Identify different types of System Verilog Advanced features																		
CLR-5 :	.Understand Assertions in System verilog.																		
CLR-6 :	Construct basic programs in TCL.																		
Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:																		
CLO-1 :	Understand the basic concepts of System C	3	80	70	L	L	-	M	L	-	-	-	L	-	-	-	M	-	-
CLO-2 :	Design Combinational and Sequential Circuits in System C	3	85	75	H	L	-	M	L	-	-	-	L	-	-	-	M	-	-
CLO-3 :	Realize the basic conventions in System Verilog	3	75	70	H	L	-	M	L	-	-	-	H	-	-	-	M	-	-
CLO-4 :	Identify the system Verilog Advanced features.	3	85	80	H	H	-	M	M	-	-	-	H	-	-	-	H	-	-
CLO-5 :	Utilize the Assertion feature in System verilog.	3	85	75	H	H	-	H	M	-	-	-	H	-	-	-	H	-	-
CLO-6 :	Understand various concepts in TCL	3	80	70	L	H	-	H	H	-		-	H	-	-	-	H	-	-

Duration (hour)		System C 12	ADVANCED FEATURES 12	SYSTEM VERILOG (SV) 12	ADVANCED FEATURES 12	SCRIPTING LANGUAGE 12
S-1	SLO-1	Introduction, Design Methodology	Modeling Examples	Literal values- Integer and logic literals	Classes -Objects	Introduction
	SLO-2	Data types –Value holders, bit, arbitrary width, logic	A memory model	Real literals, Time literals, String literals, Array literals , Structure literals	Methods	Characteristics of Scripting languages
S-2	SLO-1	Resolved type, User defined type, Integer	Modeling an FSM-Mealy FSM	Data types- String data type	Static methods	The TCL phenomena
	SLO-2	Modeling combinational logic	Moore FSM	User-defined types, Enumerations data type	Casting	Philosophy , Structure
S-3	SLO-1	SC -module	Universal shift register	Arrays –Dynamic Arrays,	Chaining Constructors	Syntax ,Parser
	SLO-2	File structure	Programs -FSM	Associative arrays	Programs on Constructors	Variables
S-4	SLO-1	Reading and writing port signals	Counters- Modulo N counter	Data declarations – constant, variables	Data hiding	Data in TCL
	SLO-2	Logical operators, Arithmetic operators	Johnson counter, Gray code up down counter	nets, registers	Encapsulation	Control flow
S-5	SLO-1	Relational operators	Programs -Counters	Programs using Arrays	Parameterized classes	Data structures
	SLO-2	Programs using Operators	Writing a Test bench	Attributes	Polymorphism	Simple input / output
S-6	SLO-1	Vector Ranges	Simulation control	Operators-Assignment, Real	Types of class	Procedures
	SLO-2	Constant index, Non constant index	Waveforms	Streaming ,conditional	Classes and structures	Programs on control flow
S-7	SLO-1	Delta delay	Monitoring behaviour	Operator overloading.	Programs on Classes	Programs on procedures
	SLO-2	IF statement, Switch statement	Simulation control	Program using Operators	Random constraints	Working with strings, patterns
S-8	SLO-1	Programs using IF, SWITCH Statements	SC-thread process	procedural statements	Random variables	Files
	SLO-2	Loops, methods,	Dynamic sensitivity	Blocking and non blocking assignments	Randomization methods	pipes

S-9	**SLO-1**	*Structures, delta delay*	*Constructor arguments*	*Event control*	*Assertions*	*The eval ,source, commands*
	SLO-2	*Programs on Adder*	*Ports, Interfaces and Channels*	*Process*	*Boolean expressions*	*exec and up level commands*
S-10	**SLO-1**	*Multiplexer , decoder,*	*Shared data members*	*Combinational logic*	*Sequencing operations*	*Libraries*
	SLO-2	*Encoder ,Priority encoder*	*Fixed point types*	*Sequential logic*	*Multiple clock support*	*Packages*
S-11	**SLO-1**	*Modeling flip flops,*	*Module*	*Latched logic*	*Programs -sequencing*	*Namespaces*
	SLO-2	*Programs on Multiplexer, encoder ,decoder*	*Simulation Algorithm*	*Programs using process*	*Case studies -System Verilog assertion API*	*Trapping errors*
S-12	**SLO-1**	*Modeling latches*	*Programs on Shift Registers*	*Tasks*	*System Verilog coverage API*	*Event driven programs*
	SLO-2	*Handling don't cares*	*Run time environment*	*Functions*	*System Verilog Test bench*	*Programs on Packages*

Learning Resources	1. J.Bhaskar , "A System C Primer ", Galaxy publications ,2004. 2. System Verilog for Verification: A Guide to Learning the Test bench Language Features By Chris Spear Edition: 2, Published by Springer, 2008 . 3. A Practical guide for System Verilog Assertions By Srikanth Vijayaraghavan & Meyyappan Ramanathan Edition: illustrated Published by Springer, 2005.	4. System Verilog 3.1 a-Language Reference Manual (Accelera Extensions to Verilog 2001),2004 5. Brent Welch ,"Practical Programming in TCL and TK,"Fourth Edition 2003

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Dr. E. Chitra, SRMIST*

Course Code	20ECE533T	Course Name	Low-Power CMOS Circuit Design	Course Category	E	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLR-1 :	Low Power VLSI concepts and Power Analysis.																		
CLR-2 :	Describe the Low Power very fast Dynamic logic circuits																		
CLR-3 :	Design of low power VLSI Techniques and arithmetic																		
CLR-4 :	Understanding concept of Adiabatic Techniques and Memories																		
CLR-5 :	Low Power VLSI applications.																		
CLR-6 :	Understand, Design and Application of low -Power CMOS Circuits.																		
Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:																		
CLO-1 :	Motivate interest from VLSI designer to the leakage mechanism influencing different leakage currents and its impact on future of CMOS.	3	80	70	H	H	M	M	-	-	-	-	-	-	-	-	-	-	-
CLO-2 :	Design of Dynamic CMOS latches, Flip-flops and power reduction.	3	85	75	H	H	H	L	-	-	-	-	-	-	-	-	-	-	-
CLO-3 :	Optimization of speed and switching activity using special techniques also optimization in arithmetic level.	3	75	70	H	H	H	M	-	-	-	-	-	-	-	-	-	-	-
CLO-4 :	Adiabatic and energy recovery techniques offer new possibilities to trade dynamic power dissipation for delay in switching circuits.	3	85	75	-	H	H	-	-	-	-	-	-	-	-	-	-	-	-
CLO-5 :	Apply low power technique concepts in various Applications.	3	85	75	-	H	H	-	H	-	-	-	-	-	-	-	-	-	-
CLO-6 :	Understanding of Various special Low-Power CMOS circuits and its Applications.	3	85	75	H	H	H	-	H	-	-	-	-	-	-	-	-	-	-

Duration (hour)		Introduction to Low Power VLSI and High level power estimation and analysis (12)	Low Power very fast Dynamic logic circuits (12)	Special Low Power VLSI Design Techniques and Arithmetic Operators (12)	Adiabatic Techniques and Memories (12)	Applications of Low Power VLSI Design (12)
S-1	SLO-1	Introduction - Needs for low power VLSI	Introduction- Single clock latches and Flip-flops	Introduction: Glitch reduction	Introduction: Adiabatic Computation	MTCMOS
	SLO-2	Charging and discharging capacitance	TSPC Latches and Flip-Flops	Gate-level, Block-Level control.	Complementary Adiabatic logic.	High Speed ,Low power using MTCMOS
S-2	SLO-1	Short circuit current of CMOS inverter-CMOS leakage current	Differential Single-clock Latches and Flip-flops-DVSL	Clock gating-Flip flop based design	Adiabatic charging principle:	MTCMOS-DSP
	SLO-2	Static current.	Static RAM latch	Issues in clock gating of DFF-based design.	Implementation Issues:	Mobile Phone application.
S-3	SLO-1	CMOS leakage d current: Reverse biased PN-Junction.	Single transistor clocked differential latch	Latch-Based design	Adiabatic Logic	Conventional circuit and Logic style
	SLO-2	Subthreshold channel leakage.	Power-delay comparison.	Issues in Latch -Based design	Adiabatic Buffering	Power consumption of CMOS Adders and Multipliers
S-4	SLO-1	Basic Principles of Low power design-Reduced switching voltage, reduced capacitance.	High throughput CMOS circuit techniques-TSPC Pipeline	FSM-Gated clock FSM	Latch and energy-recovery driver circuit	Delay Balanced Multipliers for low power/low voltage DSP core
	SLO-2	Reduce switching frequency, Reduce leakage.	TSPC Double pipeline	State encoding, FSM Partitioning	Adiabatic Power supplies	Latches and Flip-flops for Low power systems.
S-5	SLO-1	Network restructuring.	CDPD technique	Bus Invert encoding	Power efficiency of adiabatic logic	Power Analysis Techniques:
	SLO-2	Network reorganization.	CDPD chains	Other Bus encoding Techniques	Adiabatic circuit with full complementary feedback.	A survey of high level power estimation techniques.
S-6	SLO-1	Generic design flow for low power applications.	Fast and efficient CMOS Functional circuits-Divide and Ripple counter.	Data Paths: Precomputation design.	Pass transistor Logic synthesis	Estimation of Average switching activity in combinational circuits

	SLO-2	Generic power estimation and analysis tool flow	Synchronous counter	Control-signal Gating design	Basics of pass transistor logic.	Gate delay effects.
S-7	**SLO-1**	Low power design flow.	Adder and Accumulator	Low power arithmetic operators: Adder	Boolean Decision Diagram	Power Estimation of Sequential logic circuits
	SLO-2	Generic low power design flow	Bit-Serial comparator	Any adder implementation.	Shannon's Decomposition to construct BDD.	STG Characteristics.
S-8	**SLO-1**	System level power analysis	Circuit Parallelization	Low power arithmetic operators Introduction: Adder	Pass transistor Logic synthesis	Survey of High-level Power estimation techniques
	SLO-2	System level architecture.	Memory Parallelization	Any adder implementation.	Pass transistor cell in logic synthesis.	All levels of design flow in power estimation.
S-9	SLO-1	Algorithm-level power estimation and analysis	Serial-Parallel converter	Multiplication	Low power techniques for SRAM cell	Power Optimization Techniques
	SLO-2	Software Power analysis.	Linear Feed-Back shift Registers	Any multiplier implementation.	SRAM Cell, Memory Bank Partitioning	Transformation and synthesis of FSMs for low-Power Gated clock implementation
S-10	SLO-1	Algorithm-level power estimation for Hardware implementation.	Voltage scaling based circuit techniques-Multiple voltage Techniques.	Multiplication	Pulsed wordline and reduced Bitline swing.	Precomputation Based sequential logic optimization for low-power.
	SLO-2	Generic target Architecture.	Low voltage swing.	Any multiplier implementation.	Case study: Design of an FIFO buffer	Precomputation Based sequential logic optimization for low-power
S-11	SLO-1	Resource allocation Binding and sharing	Circuit technology-Independent Power reduction	Square function computation.	Basics of DRAM cell	Glitch Analysis and reduction in RTL power optimization
	SLO-2	Scheduling.	Synthesis of FSMs with Gated clocks.	Division and Square root	Cell refresh circuit-HVG	Glitch generation in the controller and datapath.
S-12	SLO-1	Behavioral-Level Power estimation	Dependent power reduction-Path Balancing	Floating point arithmetic	DRAM -BBG	Glitch reduction techniques
	SLO-2	Interconnect power estimation.	Technology Decomposition, Technology mapping.	Logarithmic number system	DRAM -BVG	Minimizing glitch propagation from data signal.

Learning Resources	1. Yeap, Gary K. Practical low power digital VLSI design. Springer Science & Business Media, 2012. 2. Roy, Kaushik, and Sharat C. Prasad. Low-power CMOS VLSI circuit design. John Wiley & Sons, 2009.	3. Piguet, Christian. Low-power CMOS circuits: technology, logic design and CAD tools. CRC press, 2018. 4. Chandrakasan, Anantha P., and Robert W. Brodersen, eds. Low-power CMOS design. New York: IEEE press, 1998

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Dr.P.Aruna Priya, SRMIST*

Course Code	20ECE534T	Course Name	RECONFIGURABLE COMPUTING SYSTEMS	Course Category	C	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		*Nil*	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	*To familiarize wide range of reconfigurable hardware*			
CLR-2 :	*To introduce architecture that enables high performance computation as well as the supporting application mapping process.*			
CLR-3 :	*Ability to understand the computational architectures for FPGA*			
CLR-4 :	*To explore different Optical reconfigurable architectures.*			
CLR-5 :	*Focuses on specific, important field-programmable gate array (FPGA) applications, presenting case studies of interesting uses of reconfigurable technology.*			
CLR-6 :	*To introduce all facts of reconfigurable system and case studies that show complete applications of reconfigurable logic*			

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	*Understand the fundamentals of the reconfigurable computing and reconfigurable architectures.*	3	80	75	H	H	H	H	M	-	-	-	-	-	-	-	-	-	H
CLO-2 :	*Articulate the design issues involved in reconfigurable computing systems with a specific focus on Field Programmable Gate Arrays (FPGAs) both in theoretical and application levels*	3	85	75	H	H	H	M	M	-	-	-	-	-	-	-	-	-	H
CLO-3 :	*Understand both how to architect reconfigurable systems and how to utilize them for solving challenging computational problems..*	3	80	70	H	H	H	H	H	-	-	-	-	-	-	-	-	-	H
CLO-4 :	*Understand the models, algorithms and techniques for optical reconfigurable architecture*	3	85	80	H	H	H	M	H	-	-	-	-	-	-	-	-	-	H
CLO-5 :	*Explore important field-programmable gate array (FPGA) reconfigurable applications through case studies*	3	85	75	H	H	H	H	H	-	-	-	-	-	-	-	-	-	H
CLO-6 :	*Understand all about reconfigurable system and complete applications of reconfigurable logic by case studies*	3	85	80	H	H	H	H	H	-	-	-	-	-	-	-	-	-	H

Duration (hour)		Reconfigurable Computing Hardware	Mapping Designs Into Reconfigurable Platforms	Computational Architectures for FPGA	Optical Reconfiguration Model	Case Studies Of FPGA Applications
		12	12	12	12	12
S-1	SLO-1	Logic- computational fabric	Mapping designs into reconfigurable platforms	Precision analysis for fixed point computation	Optical reconfigurable models	SPIHT Image Compression
	SLO-2	Logic Elements , Programmability .	Structural mapping algorithm	Fixed-point number system	Models, Models Everywhere	SPIHT algorithm
S-2	SLO-1	Array and interconnect	Area oriented, performance driven mapping	Multiple-wordlength Paradigm	Basic algorithm techniques	SPIHT Coding Engine
	SLO-2	Interconnect Structures ,Programmability	power-aware mapping	Wordlength optimization	Permutation Routing, Binary Prefix Sums	Wavelets and the Discrete Wavelet Transform
S-3	SLO-1	Extending Logic	Integrated mapping algorithms	Analytic Peak Estimation	Algorithms for Optical Models	Design considerations and modifications
	SLO-2	Extended Logic Elements	Simultaneous Logic Synthesis	Distributed arithmetic	Basic Results ,Sorting and Selection	Fixed-point Precision Analysis
S-4	SLO-1	Configuration	Integrated Retiming	DA implementation	Multiple Addition	Hardware implementation-basic
	SLO-2	SRAM , Flash Memory ,Antifuse	Placement-driven Mapping	Mapping process	Matrix Multiplication	Hardware implementation
S-5	SLO-1	Reconfigurable processing fabric architectures	Mapping algorithms for heterogeneous resources-	Mapping DA onto FPGAs	h-Relations	The SPIHT Coding Phase
	SLO-2	Reconfigurable processing fabric architectures	Mapping to Complex Logic Blocks	An application of DA on an FPGA	h-Relations	The SPIHT Coding Phase
S-6	SLO-1	Fine-grained , Coarse-grained	Mapping Logic to Embedded Memory Blocks	CORDIC architectures for FPGA	Complexity of Optical Models	Automatic Target Recognition Systems on Reconfigurable Devices
	SLO-2	RPF integration into traditional computing	Mapping toMacrocells	CORDIC algorithm-Introduction	Simulating PRAMs	Automatic target recognition algorithms

		systems				
S-7	SLO-1	RPF integration into traditional computing systems	The FPGA placement	CORDIC algorithm	Simulating PRAMs example	Dynamically reconfigurable -Introduction
	SLO-2	Independent Reconfigurable Coprocessor Architecture Processor , RPF Architectures	The FPGA placement problem	CORDIC algorithm implementation	Equivalence of One-Dimensional Models	Dynamically reconfigurable designs
S-8	SLO-1	operating system support for reconfigurable computing	Clustering	CORDIC processors	Relating the PR-Mesh and the LR-Mesh	Reconfigurable static design
	SLO-2	Abstracted Hardware Resources, Flexible Binding	simulated annealing	FPGA implementation of CORDIC processors	Relating Two-Dimensional Optical Models	ATR implementations
S-9	SLO-1	Scheduling	VPR Annealing Algorithms	Boolean satisfiability basics	Run time reconfigurability	ATR implementations
	SLO-2	Evolvable FPGA	Related Annealing Algorithms	creating Solvers optimized for specific Problem instances	Run time reconfigurability Design and implementation	The Implications of Floating Point for FPGAs
S-10	SLO-1	Artificial Evolution	Simultaneous Placement and Routing with Annealing	SAT-solving algorithms	Run-Time Reconfiguration Basic Concepts	General Implementation Considerations
	SLO-2	Evolvable Hardware Digital Platforms	analytical placement	Case study: optimized fixed-point arithmetic	Generic Problems	Adder Implémentation
S-11	SLO-1	Case Study: Altera Stratix	partition based placement		Specific Problems	Multiplier-Introduction
	SLO-2		partition based placement example	optimized fixed-point arithmetic circuits in custom hardware		Multiplier Implementation
S-12	SLO-1	Case Study: Xilinx Virtex-II Pro	Case study: proposed algorithms to combine logic synthesis with covering to overcome the limitations of pure structural mapping	Case study: floating point multiplier	Case study : Implémentation of Optical model	Case study : Floating-point application
	SLO-2					

Learning Resources	1. Scott Hauck and Andre` DeHon, "Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation", Morgan Kaufmann, 2008. 2. CliveMaxfield, "The Design Warrior's Guide to FPGAs: Devices, Tools and Flows", Newnes, Elsevier,2006	3. Ramachandran Vaidhyanathan and Jerry. L. Trahan "Dynamic Reconfiguration: Architectures and Algorithms", Kluwer Academic publishers, 2003.

Learning Assessment

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		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2.*

Course Code	20ECE535T	Course Name	Cryptography and Hardware Security in VLSI	Course Category	E	Professional Elective	L	T	P	C
							4	0	0	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR): *The purpose of learning this course is to:*

		Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLR-1 :	*The essential mathematical techniques that apply to cryptography*																		
CLR-2 :	*Describes principles, techniques and algorithms with a strong desire to learn cryptography*																		
CLR-3 :	*Overview of hardware security algorithms in VLSI*																		
CLR-4 :	*Significance of hardware FPGA implementation.*																		
CLR-5 :	*Various attacks and counter measures*																		
CLR-6 :	*Present an overview of mathematics, cryptography algorithm in software and implementation in hardware*																		
CLO-1 :	*Applied the detailed mathematical concepts for cryptography.*	3	75	70	H	M	H	H	-	-	-	-	-	-	-	-	-	-	-
CLO-2 :	*Understand the general structure of Block cipher and steam cipher algorithms.*	3	85	75	H	H	H	H				-	-	-	-	-	-	-	-
CLO-3 :	*Hardware Implementation and performance analysis Hash, RSA*	3	75	70	H	H	M	M				-	-	-	-	-	-	-	-
CLO-4 :	*Detailed study of different PUFs*	3	85	75	H	H	H	M	H			-	-	-	-	-	-	-	-
CLO-5 :	*Learned Different types of Trojan and physical attacks.*	3	85	75	H	H			H			-	-	-	-	-	-	-	-
CLO-6 :	*Able to construct various cryptography algorithms and their hardware implementation.*	3	85	75	H	H	H	H	H			-	-	-	-	-	-	-	-

Course Learning Outcomes (CLO): *At the end of this course, learners will be able to:*

Duration (hour)		Mathematics of Cryptography (12 Hours)	Modern Cryptography (12 Hours)	Hardware Implementation of Hash Function, RSA (12 Hours)	Physical Unclonable Function and FPGA Implementation (12 Hours)	Hardware Trojan and Physical Attacks and its Counter measures (12 Hours)
S-1	SLO-1	Introduction about Hardware Security	Security goals	Introduction to Cryptographic Hash Functions	Introduction	Taxonomy of Hardware Trojans
	SLO-2	Modular arithmetic	Attacks and Services	The Merkle- Damgard model of hash functions	Classification of PUF	Classification
S-2	SLO-1	Groups, Rings and Fields	Block Ciphers	Construction of Hash function	Weak PUF	Phase of Insertion
	SLO-2	Basic Problems	Feistel cipher	Application of Hash function	ICID PUFs	Different phases of Phase insertion steps.
S-3	SLO-1	Greatest common divisors	Cipher block chaining mode	Hardware Implementation of Hash Functions	SRAM Based PUFs	Abstraction level of description
	SLO-2	Multiplication Inverse	Cipher feedback mode	MD5-Pipeling	SRAM based NOR& NAND circuit	Different level of abstraction description.
S-4	SLO-1	Euclidean Algorithm	Algorithm for DES	SHA-2	Strong PUFs	Activation mechanism, effects
	SLO-2	Theorem& corollary	Functional blocks of DES	Performance analysis	Features of strong PUF	Location.
S-5	SLO-1	Extended Euclidean Algorithm	Key generation of DES	SHA-3	Arbiter PUF	Hardware Trojan detection-Introduction
	SLO-2	Examples	DES example	Keccak Algorithms	Variants of arbiter PUF	Different stages of IC design flow.
S-6	SLO-1	Construction of Galois Field	Algorithm for AES	Comparison of MD-5,SHA-2,SHA-3	Analog PUFs	Hardware Trojan detection in IC
	SLO-2	Example	Functional blocks of AES	Performance analysis	Glitch PUF architecture	Hardware Trojan detection approaches
S-7	SLO-1	Efficient Galois Fields	Key generation of AES	RSA: Implementation and security	Controlled PUF and it s Implementation	Trojan Modelling.
	SLO-2	Squaring circuit	AES example	Introduction of RSA	Architecture of controlled PUF.	Combinational modeling

S-8	SLO-1	Mapping between Binary and Composite Fields	RSA algorithm for encryption	Algorithm Description and analysis	FPGA synthesis flow	Sequential modeling.
	SLO-2	Example	RSA algorithm for decryption	RSA Key Generation Algorithm	vulnerabilities	Test generation
S-9	SLO-1	Introduction to cryptography	Elliptic curve	Hardware implementation of RSA	Side channel attack	Case study: Design of MOLES Trojan
	SLO-2	Prime Number Generation	Hash function	3-bit combinational multiplier	Fault injection attack	Case study: Secret-Key Leakage Through RS232 Protocol
S-10	SLO-1	Pseudo random Sequence Generator	SHA-1	Serial Parallel multiplier	FPGA Hardware security primitives	Side Channel Attacks
	SLO-2	Algorithm	MAC	Examples	FPGA Implementation of PUFs	Side Channel: Power consumption.
S-11	SLO-1	Linear Congruential Generators	Steam Ciphers using LFSR	Security Analysis	Arbiter based PUF	Countermeasures: Hiding
	SLO-2	Examples.	Example	Security Analysis	Two implementation of path selecting switches.	Countermeasures:Masking/Blinding
S-12	SLO-2	Linear Feedback shift registers	BM Algorithm	RSA implementation using software	LUT based programmable delay line.	Countermeasures: Design partitioning
	SLO-2	Example	Example	Summary of Hash function and its Implementation	Delay Based PUF	Countermeasures: Physical security

Learning Resources	1. Stallings, W. (2014). Cryptography and network security, 6/E. Pearson Education India. 2. Katz, J., Menezes, A. J., Van Oorschot, P. C., & Vanstone, S. A. (1996). Handbook of applied cryptography. CRC press.	3. Tehranipoor, M., & Wang, C. (Eds.). (2011). Introduction to hardware security and trust. Springer Science & Business Media. 4. Mukhopadhyay, D., & Chakraborty, R. S. (2014). Hardware security: design, threats, and safeguards. Chapman and Hall/CRC.

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	1. Dr.P.Radhika, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	2. Mrs.M.Valarmathi, SRMIST

Course Code	20ECE536T	Course Name	Process and Device Simulation using CAD	Course Category	E	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	20ECC532J	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Determine key indicators of device performance by linking process simulation to device simulation			
CLR-2 :	Provide an insight into the role of device simulation in circuit design			
CLR-3 :	Describe the analytical theory, application of 1D process and device analysis of MOSFET structures			
CLR-4 :	Build a firm foundation in the use of Computer-Assisted techniques for IC device and process Design (CAD			
CLR-5 :	Identify the performance metrics for RF applications			
CLR-6 :	depict the physical processes in the interior of a device and make reliable predictions of the behaviour of next-generation devices			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Design, analyze and optimize semiconductor technologies and devices with fundamental and accurate models.	2	75	70	H	-	-	H	-	-	-	-	-	-	-	-	H	-	H
CLO-2 :	Analyze the basic formulation of decoupling the device equations	2	85	75	H	H	-	H	-	-	-	-	-	-	-	-	-	-	-
CLO-3 :	Compute the threshold voltage for any general structures with process / device simulation programs.	2	75	70	H	-	-	-	H	-	-	-	-	-	-	-	H	-	-
CLO-4 :	Fit the simulation methodology as close as possible to the fabrication technology.	3	85	75	H	-	H	-	H	-	-	-	-	-	-	-	H	-	H
CLO-5 :	Predict the physical and current-voltage properties of 3D semiconductor devices.	3	85	75	H	-	H	-	H	-	-	-	-	-	-	-	H	-	
CLO-6 :	Examine the important properties of a compact model for both analog and RF circuits.	2	85	75	H	-	-	H	-	-	-	-	-	-	-	-	-	-	H

Duration (hour)		IC technology and TCAD tools	Device CAD	MOS Structures	FinFET Structure	Compact models for analog and RF applications
		12	12	12	12	12
S-1	SLO-1	Introduction - *A typical process simulation flow*	Introduction-Semiconductor Device Analysis	Introduction – The MOS capacitor	Introduction of Moore's Law and FinFET	Important role of FinFET in anlog / RF circuits
	SLO-2	*The conventional role of TCAD in IC processing*	Field-Effect Structures	section view to illustrate *pn* junctions and MOS capacitor using CAD tool	ITRS - transistor and circuit performance	Introduction - Important compact model metrics
S-2	SLO-1	*Steps involved in device simulation*	Components of Charge	Energy band diagram of the MOS	Device and circuits scaling key parameters	Analog metrics
	SLO-2	*Coupling of electronic design (ECAD) with technology design (TCAD)*	Bulk Charge - Q_B	Flatband conditions for polysilicon gate MOSFETs	***FinFET structure***	Quiescent operating point
S-3	SLO-1	TCAD for nanoelectronics	Bipolar Junction Structures - Introduction	Basic MOSFET I-V Characteristics	Design Considerations of Threshold Voltage	Importance of moderate region
	SLO-2	Process and Device CAD	Bipolar Device	Terminal conductance G_{DS}	Leakage Current	Role of leakage currents in discrete-time and low-power applications
S-4	SLO-1	Introduction - *A typical process simulation flow*	Equilibrium Equation	the surface inversion	Power Consumption	Geometric scalability
	SLO-2	*The conventional role of TCAD in IC processing*	Non-Equilibrium Equation	MOSFET conduction band surface	High-k Dielectric Materials	Significance of fixed *W* and sweep the number of transistor fingers N_f
S-5	SLO-1	Process simulation techniques	Coupled Equations	band diagrams as functions of *VDS* and *VGS*	***Metal Gate***	Variability model
	SLO-2	Interfaces in process and Device CAD	Minority Carrier Continuity	inversion layer as a nonlinear resistor	***Device Gate***	fully differential circuit
S-6	SLO-1	CMOS technology - Introduction	Analysis of a *PN* Junction Diode using CAD	***Drain current expression***	Process flow of FinFET simulation.	Intrinsic voltage gain
	SLO-2	Ion implantation- Gaussian Profiles	principles of junction operation	Threshold Voltage in Nonuniform Substrate	FinFET 3D Simulation	Device intrinsic gain A_0 as a function of channel length L
S-7	SLO-1	Pearson IV Profiles	Illustrate the electric field plot across the device for various value of V	compute V_{FB} for most nonuniformly doped situations	2D cross-sectional diagram of 3D FinFET structure	Device intrinsic gain A_0 versus device bias .

	SLO-2	Multi-layer Implantation	Illustrate the potential plot across the device for various value of V	transcendental equation for space charge region width	Illustration of "ABA" command	Device transconductance efficiency versus *device bias*.
S-8	**SLO-1**	Boltzmann Transport Analysis	the hole and electron components of current change with position	Threshold voltage computation with a Gaussian channel doping profile	Physical Property Analysis of FinFET	Device transconductance *gm* versus *Vgs* and *Vds*.
	SLO-2	Oxidation -Physical Mechanisms, Intrinsic Oxidation Kinetics,	PN Junctions - Carrier Densities:	MOS Device Design by Simulation	1D energy band diagram	Speed: Unity gain frequency
S-9	**SLO-1**	Substrate Doping Dependence, Thin Oxides	Equilibrium Case	Body-bias Sensitivity of Threshold Voltage	Electron concentration distribution	cascade of common-source amplifiers
	SLO-2	Impurity Diffusion	Non-Equilibrium case	Two-region Model	Electric field distribution	Noise
S-10	**SLO-1**	Point Defect Kinetics	Carrier Transport and Conservation	MOSFET Design by Simulation	Electric potential distribution	Drain noise current spectral density versus frequency for a family of channel lengths *L*
	SLO-2	Concentration Dependent Diffusion	the *pn* Junction - Equilibrium Conditions	Subthreshold characteristics	Energy band diagram Ec and Ev	Linearity and symmetry
S-11	**SLO-1**	Dopant Clustering	the *pn* Junction :Non-equilibrium Conditions	Case Study: Illustrate the analytical theory of the MOSFET	Id–Vd curve of FinFET simulation	RF metrics - Two-port parameters
	SLO-2	Dopant Segregation	Use CAD tool to analyze - Heavy Doping Effects	Case Study: Illustrate the analytical theory of the MOSFET	Speed of CMOS Inverter—Importance of I_{on}	The need for speed
S-12	**SLO-1**	Oxidation Enhanced Diffusion (OED)	Case Study : Analysis of High-Level Injection using TCAD	set of suitable applications of 1D process	Case Study : Design 3D FinFET Inverter with Lg = 15 nm	Non-quasi-static model
	SLO-2	*Implement ion implantation using TCAD tool*	Technology-Dependent Device Effects in PN junction using TCAD	device analysis of MOS structures	***Extract electrical parameter and*** inverter voltage–time curve	***Noise and Linearity***

Learning Resources	1. Yung-Chun Wu • Yi-Ruei Jhan, "3D TCAD Simulation for CMOS Nanoeletronic Devices", Springer Nature Singapore Pte Ltd. 2018. 2. Yogesh Singh Chauhan, Darsen Duane Lu, Vanugopalan Sriramkumar, Sourabh Khandelwal, Juan Pablo Duarte, Navid Payvadosi, Ai Niknejad, Chenming Hu , "FinFET Modeling for IC 'Simulation and Design: Using the BSIM-CMG Standard", Academic Press - Elsevier ,2015.	3. G.A. Armstrong, C.K. Maiti, "TCAD for Si, SiGe and GaAs Integrated Circuits", Published by The Institution of Engineering and Technology, London, United Kingdom, 2007. 4. M S Lundstorm, Fundamentals of Carrier Transport, 2nd Ed., Cambrid University Press,Cambridge UK, 2000. 5. Robert W.Dutton, Zhiping Yu, " Technology CAD Computer Simulation of Processes and Devices", Kluwer Academic Publishers, 1993. 6. Synopsys Sentaurus TCAD Manual.

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1(20%)		CLA-2(25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

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		3. Dr. P. Aruna Priya, SRMIST

Course Code	20ECE537T	Course Name	Diagnosis and Reliable Design of Digital Systems	Course Category	E	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engg	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	To understand the level in the domain of VLSI Design and Test.			
CLR-2 :	To learn the concept of VLSI Testing and analyze the potential of ATPG algorithms			
CLR-3 :	To understand the challenges involved in scan design and test			
CLR-4 :	To introduce Testable memory design and IDDQ Testing			
CLR-5 :	To design for testability and explore the built-in-test concepts			
CLR-6 :	To understand the significance of testing in VLSI, fault models, test generation and fault simulation.			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)															
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Improves the knowledge level in the domain of VLSI Design and Test	3	80	80	H	H	H	L	L	-	-	-	-	-	-	-	-	-	H
CLO-2 :	Enhances the creativity to develop new ATPG Algorithms	3	85	75	H	H	H	H	H	-	-	-	-	-	-	-	-	-	H
CLO-3 :	Analyze the challenges involved in scan design and test	3	75	70	H	H	H	H	H	-	-	-	-	-	-	-	-	-	H
CLO-4 :	summarize Testable memory design and IDDQ Testing method	3	80	75	H	H	H	M	M	-	-	-	-	-	-	-	-	-	H
CLO-5 :	Enables to design for testability	3	85	80	H	H	H	H	H	-	-	-	-	-	-	-	-	-	H
CLO-6 :	Summarize the significance of fault diagnosis and reliable design of VLSI system and understand fault models, fault simulation and about ATPG.	3	80	75	H	H	H	H	H	-	M	-	-	-	-	-	-	-	H

Duration (hour)		Introduction to Testing	Unit-II: Test Generation for Combinational circuit	Unit-III: Test Generation for Sequential circuits	Unit-IV: Memory, IDDQ Testing	Unit-V: Design for Testability
		12	12	12	12	12
S-1	SLO-1	Introduction Testing	Test generation basics	Testing generation of sequential circuits	Testable memory design	Basic principle of of Built-in Self-Test
	SLO-2	Role of testing in VLSI Design flow	Test generation algorithms	Testing of sequential circuits as iterative combinational circuits	Memory organization	Test pattern generation of Built-in Self-Test
S-2	SLO-1	Testing at different Levels of abstraction	path sensitization	state table verification	RAM fault models	Exhaustive Testing
	SLO-2	Types of testing	path sensitization example			Pseudo- Exhaustive pattern Generation
S-3	SLO-1	Fault Error,defect,diagonosis,yield	Boolean difference	Designing Checking Experiments	test algorithms for RAMs	Pseudo-Random Pattern Generation
	SLO-2	Types of tesing,Rule of Ten,Defects in VLSI Chip	Boolean difference example	Test generation based on circuit structure	GALPAT,Walking 0s and 1s,March and Checkerboard Test	Deterministic Testing
S-4	SLO-1	DC parametric tests	Significant Combinational ATPG Algorithm	Example Test generation based on circuit structure	IDDQ testing-Motivation	Output response analysis
	SLO-2	AC parametric tests	D algorithm-basic	Design of testable sequential circuits	Fault Detected by IDDQ test	Transition count
S-5	SLO-1	fault modeling	D algorithm	Controllability and Observability	IDDQ Testing Methods	Syndrome checking ,signature analysis
	SLO-2	Stuck-at fault	D algorithm based example	Ad Hoc design rules for improving Testability	testing methods - limitations of IDDQ testing	Economic case for BIST
S-6	SLO-1	Stuck-at fault example	PODEM algorithm	Ad Hoc design rules for improving Testability	Delay faults	BIST architectures
	SLO-2	Bridging fault	comparing D and PODEM			BILBO
S-7	SLO-1	Bridging fault example	Testable combinational logic circuit design	The scan-path Technique for Testable Sequential circuit design	Delay test Problem	STUMPS

	SLO-2	Stuck on open fault in CMOS	Reed –Muller Expansion Technique	partial scan	Path Delay Test	Memory BIST
S-8	**SLO-1**	Case study: Fault model types in all level of circuit design.	Case study : Advanced ATPG algorithm	Boundary scan-Motivation	Delay Test Methodologies	Case study :TAP controller design using RTL
	SLO-2			System configuration with boundary scan	Practical considerations in Delay Testing	
S-9	**SLO-1**	fault equivalence	Three-Level OR-AND-OR Design	Case Study: State table design for sequential circuit	Case study Testable Memory design	CMOS Testing
	SLO-2	fault equivalence and fault collapsing	Synthesize of Random Pattern Testable Combinational circuits			
s-10	**SLO-1**	fault dominance	Path Delay Fault Testable Combinational Logic design	Testable sequential circuit design example	Cache RAM chip testing	Testing of static CMOS circuit
	SLO-2	fault dominance and fault collapsing				Testing of dynamic CMOS circuit
s-11	**SLO-1**	fault simulation	Testable PLA Design	Case study:ATPG for synchronous circuit	Functional ROM Chip testing	Design for robust testability
	SLO-2	Types of fault simulation				
s-12	**SLO-1**	Case study: Automatic Test Equipment	Case study :Algorithms and Representations – Redundancy Identification	Test Sequence generation using State table	Case study:Analog Testing	Case Study: System testing and test for SOCs.
	SLO-2					

Learning Resources	1. *P. K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.* 2. *M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal* 3. *VLSI Circuits", Kluwar Academic Publishers, 2004.* 4. *I.M.Abramovici,M.A.Breuer and A.D.Friedman,"Digital system and Testable design",Jaico Publishing House*	5. *N.K. Jha and S.G. Gupta, "Testing of Digital Systems", Cambridge University Press,2003.* 6. *Zainalabe Navabi, "Digital System Test and Testable Design: Using HDL Models and* 7. *Architectures", Springer, 2010.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA) (60% weightage)*						*Final Examination(40% weightage)*	
		CLA-1(20%)		*CLA-2(25%)*		*CLA-3#(15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*30*	*-*	*30*	*-*	*30*	*-*	*30*	*-*
	Understand								
Level 2	*Apply*	*40*	*-*	*40*	*-*	*40*	*-*	*40*	*-*
	Analyze								
Level 3	*Evaluate*	*30*	*-*	*30*	*-*	*30*	*-*	*30*	*-*
	Create								
	Total	*100 %*		*100 %*		*100 %*		*100 %*	

 # CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
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Course Code	20ECE538T	Course Name	HIGH PERFORMANCE ASIC DESIGN	Course Category	E	Professional Elective	L	T	P	C
							4	0	0	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Prepare the student to be an entry-level industrial standard ASIC or FPGA designer.			
CLR-2 :	Give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.			
CLR-3 :	Give the student an understanding of basics of System on Chip and Platform based design.			
CLR-4 :	Understand the basic FPGA Architecture			
CLR-5 :	Analyze the partitioning and placement issues			
CLR-6 :	Understand the concept of clock planning in ASIC Design			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)													
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Be familiar with different FPGA Architecture and their interconnect mechanism	2	80	50	M												H		
CLO-2 :	Understand the significance of Partioning and placement in ASIC Design	3	99	70		H	H		M				M				H		
CLO-3 :	Be familiar with optimization algorithms in ASIC	2	80	70					M								H		
CLO-4 :	Strong foundation in various routing algorithm	3	90	70			H	M	M				M				H		
CLO-5 :	Detail analyze of clock planning in ASIC	2	90	85	L	L			L										M
CLO-6 :	Various power strategies in ASIC Design	2	90	70	L	M	H	M	M				M				H		L

Duration (hour)		Introduction To ASIC	Programmable ASIC Logic Cells	Optimization Methods	Optimization Algorithms	Logic Synthesis, Placement And Routing,High Performance Algorithms
		12	12	12	12	12
S-1	SLO-1	Types of ASICs	Actel ACT Architecture	Trade off issues at SystemLevel	Planar subset problem (PSP)	Logic synthesis
	SLO-2	VLSI Design flow.	Actel Interconnect delay analysis	Solutions to the issues at system level	Introduction to Routing	ASIC floor planning,
S-2	SLO-1	Programmable ASICs design types	Xilinx LCA -Architecture	Optimization with regard to speed	single layer global routing	Measurement of Delay in Floorplanning
	SLO-2	Antifuse, SRAM	Xilinx LCA internal architecture	Optimization with regard to area	single layer global routing	Channel Definition, I/O and Power Planning
S-3	**SLO-1**	EPROM based ASICs	Xilinx EPLD Architecture	Optimization with regard to power	single layer detailed routing wire length	Clock Planning: introduction
	SLO-2	ASIC Fusing based on EPROM	Xilinx EPLD Internal Architecture	Optimization trade off factor	single layer detailed routing wire length	Clock planning detailed analysis
S-4	SLO-1	EEPROM based ASICs	Xilinx LCA Interconnect	Asynchronous and low power system design.	Introduction to Left Edge First Algorithm	placement and routing
	SLO-2	FAMOS description	Xilinx EPLD Interconnect		LEF algorithm- Problem	Global routing
S-5	SLO-1	Programmable ASIC logic cells	Altera MAX 5000 - Architecture	ASIC physical design issues	bend minimization technique	Detailed routing, Special routing
	SLO-2	ASIC I/O cells	Altera MAX 7000- Architecture	System Partitioning	over the cell (OTC) Routing	Placement algorithms
S-6	**SLO-1**	Programmable interconnects	Altera Max 9000 : Architecture	System partitioning : Objectives	Problems on LEF algorithm	constructive placement method
	SLO-2	Latest Version – FPGA	Altera Max 9000 : interconnect mechanism	System partitioning Procedure	Problem on LEF algorithm	variations on the min-cut algorithm, Eigen value method
S-7	SLO-1	Types of FPGA	Altera Interconnect features	Objective of System Portioning	Problem on bend minimization	Tutorial on seed placements.
	SLO-2	Programmable FPGA	Altera MAX 5000 : Interconnect Delay	Partitioning methods	OTC applications	min-cut placement

			analysis			
S - 8	SLO-1	Programmable FPGA	Altera MAX 7000 : Interconnect Delay analysis	Partitioning methods	Transistor chaining	Problems on min-cut algorithms
	SLO-2	ASIC I/O Cells : DC Input	Altera MAX 9000: Interconnect Delay analysis	Measuring Connectivity	Transistor chaining	bins, Eigen value placement algorithm
S - 9	SLO-1	ASIC I/O Cells : AC Input	Altera FLEX: Architecture	Problem on Constructive Partitioning	Problem on transistor chaining	Problems
	SLO-2	ASIC I/O Cells : DC/AC output	ASIC Design system: Introduction	Constructive Partitioning	Weinberger Arrays	connectivity matrix (spectral methods) ,
S-10	SLO-1	ASIC I/O Cells : Clock Input	Design Systems: Detailed analysis	Iterative Partitioning Improvement	Gate Matrix Layout	Quadratic placement.
	SLO-2	Introduction to CPLD	Logic Synthesis: Tutorial	Problem on Iterative Partitioning Improvement	Problems on Weinberger array and Gate matrix layout	disconnection matrix, characteristic equation
S-11	SLO-1	CPLD architecture	Half gate ASIC	The Kernighan–Lin Algorithm	Introduction to compaction	power strategies : Tutorial
	SLO-2	Types of CPLD	Low level design language	The Ratio-Cut Algorithm	1D compaction	Types of power strategies
S- 12	**SLO-1**	Soft-core processors-Introduction	PLA tools, EDIF	Power Dissipation: Introduction	2D compaction	Clocking strategies
	SLO-2	Architecture view of soft core processor	CFI design representation	Problem & Derivation on power dissipation	Problem on 1D and 2D compaction	Clocking strategies - tutorial

Learning Resources	1. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996. 2. Jose E. France, YannisTsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994. 3. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003	4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994. 5. Sherwani, N.A., "Algorithm for VLSI Physical Design Automation", 2ndEd., Kluwer. 1999

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1(20%)		CLA-2(25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Mr. Anuj Kumar, Bombardier* Transportation, Ahmedabad, *kumaranuj.anii@gmail.com*	1. *Dr. Meenakshi, Professor* of ECE, CEG, Anna University, *meena68@annauniv.edu*	*1. Dr.J.Selvakumar, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Mr.S.Prithiviraj, SRMIST*

Course Code	20ECE631T	Course Name	MIXED SIGNAL IC DESIGN	Course Category	E	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	20ECC533J	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR): The purpose of learning this course is to:

		Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Understand the basic architectures of Sampling and Quantization process.			
CLR-2 :	Construct the different types of fiters like MOSFET and trans-conductance filters			
CLR-3 :	Utilize the basics of A/D converters			
CLR-4 :	Identify the different types of D/A converters			
CLR-5 :	Understand Various mixed signal SOC design process and issues in analog domain			
CLR-6 :	Implement Bio-medical, IoT, signal conditioning mixed signal design process			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Construct various Sampling Architectures	2	80	70	H	H	H	H	H	H	H	M	L	-	M	-	M	-	L
CLO-2 :	Implement the different types of analog Fiters and SC amplifiers	2	80	70	H	H	H	H	H	H	H	M	L	-	M	-	M	-	L
CLO-3 :	Describe the models of various analog to digital converters	2	80	70	H	H	H	H	H	H	H	M	L	-	M	-	M	-	L
CLO-4 :	Characterize the different types of digital to analog converters	2	80	70	H	H	H	H	H	M	H	M	L	-	M	-	M	-	L
CLO-5 :	Recognize Various mixed mode SOC design process with issues	2	80	70	H	H	H	H	H	M	H	M	L	-	M	-	M	-	L
CLO-6 :	Create Bio-medical, IoT, Energy harvesting and signal conditioning design process	2	80	70	H	H	H	H	H	H	H	M	L	-	M	-	M	-	L

Duration (hour)		Switched Capacitor Circuits 12	High Frequency Analog Filters 12	DAC Architectures 12	ADC Architectures 12	Mixed Signal SOC Design 12
S-1	SLO-1	Introduction to switched capacitor circuits	Introduction	Specifications	Specifications	Introduction
	SLO-2	Sampling theoerem	Low Pass filters	DC, AC, dynamic specifications	Successive approximation converters	Mixed signal mode
S-2	SLO-1	Nyquist criteria	Problem Solving on LPF	Thermometer code converters	Problem Solving on Successive approximation converters	System on chip IC design
	SLO-2	Aliasing	Switched Capacitor filter	Hybrid converters	Flash converters	System on chip IC design
S-3	SLO-1	Problem solving on sampling and aliasing	First and second order section	Input/output characteristics of an ideal D/A converter	Flash converters	Analog design issues for CMOS mixed signal IC
	SLO-2	Quantization Process	Bilinear sections	Problem Solving on basic 4-bit DAC	Problem Solving on flash converters	Modelling
S-4	SLO-1	Quantization noise	Bilinear Transformation	Performance metrics of D/A converter	Two-step A/D converters	Problem Solving on analog issues and modelling
	SLO-2	Applications of quantizers	Biquadratic transformation	Design Issues on DAC : DNL and INL	Interpolating A/D converters	Effects of parasitics on-chip supply voltages
S-5	SLO-1	Multi-bit quantizers	Transfer function analysis of Bilinear and Bi-quad	Problem Solving on design issues	Problem Solving on interpolating converters	Interconnection Parasitics
	SLO-2	Sampling Architectures: Characteristic parameters & Types	Design of Switched Capacitor Cascade filters	D/A converter in terms of voltage division multiplication	Performance metrics of A/D converter	Architectural design
S-6	SLO-1	Unity gain sampler	Design of Switched Capacitor Ladder filters	Current division multiplication	Performance parameters for efficiency enhancement	Physical design
	SLO-2	Open loop architecture	SWITCAP	Charge division multiplication	Floating A/D Converters	Applications & Problem Solving
S-7	SLO-1	Closed loop architecture	Active RC integrators	Problem Solving on voltage division	Pipelined A/D converters	Case Studies Introduction Bio-Medical application

	SLO-2	*Design of* switched capacitor *circuits*	MOSFET-C integrators	*Problem Solving on current division*	*Problem Solving on floating ADC*	*Bio-Medical application*
S-8	**SLO-1**	*Ideal effects of SC circuits*	*Problem solving on Active RC Integrators*	*Implementing R-2R topologies for DACs*	*Problem Solving on pipelined ADC*	IoT for Mixed signal circuit design
	SLO-2	Non-ideal effects in SC circuits	*Problem solving on MOSFET-C Integrators*	Resistor-Ladder architectures	Time-Interleaved converters	IoT for Mixed signal circuit design
S-9	**SLO-1**	*Comparator Design*	Discrete time integrators	*Current mode R-2R DAC*	Time-Interleaved converters	Signal Conditioning circuits
	SLO-2	Basic building blocks	*Analysis an design of Discrete time integrators*	*Voltage mode R-2R DAC*	*Applications & Problem Solving on time interleaved architecture*	Signal Conditioning circuits
S-10	**SLO-1**	*Pre-amplifier design*	*Active LC filters*	*A wide swing current mode R-2R DAC*	*Design issues on time interleaved converters*	*Applications & Problem Solving*
	SLO-2	*Post distortion amplifier design*	*Design with passive and active inductors*	*DNL analysis*	*Applications & Problem Solving*	Energy harvesting for self-powered Wearable devices
S-11	**SLO-1**	*Comparator analysis*	Trans-conductance- C integrator filter	*INL analysis*	*Implementing S/H*	Energy harvesting for self-powered Wearable devices
	SLO-2	*Applications & Problem Solving on comparator*	*Elementary model and Trans-Conductance building block*	*Trimming DAC offset and gain*	*Cyclic ADC*	*Problem Solving*
S-12	**SLO-1**	Switched capacitor amplifier	*Automatic tuning*	*Topologies with and without Op-Amp*	*Problems on Cyclic ADC*	Sensor design
	SLO-2	*Problem Solving on SC amplifier*	*Problem Solving on Trans-conductance C filter*	*Problem solving on R-2R DAC*	*Applications of ADC*	Sensor design

Learning Resources	1. Jacob Baker, "CMOS Mixed-Signal circuit design", IEEE Press, 2009. 2. Razavi, "Principles of data conversion system design", Wiley IEEE Press, 1st Edition, 1994. 3. Razavi, "Design of analog CMOS integrated circuits", McGraw Hill, Edition 2002. 4. Esteban Tlelo-Cuautle," Advances in Analog Circuits", InTech, 1st Edition,February, 2011. 5. Mohammad Alhawari, Baker Mohammad, Hani Saleh, Mohammed Ismail," Energy Harvesting for Self-Powered Wearable Devices", ACSP, Springer, 2018. 6. Gregorian, Temes, "Analog MOS Integrated Circuit for signal processing", John Wiley and Sons, 1986. 5. Baker, Li, Boyce, "CMOS :Circuit Design, layout and Simulation", PHI, 2000. 7. Rolf Schaumann, Haiqiao Xiao, Mac E.Van Valkenburg ,"Analog Filter Design", Oxford University press,Second edition ,Re-print 2013. 8. Jacob Baker, "CMOS circuit design simulation Layout,", IEEE press, 3rd Edition 2010

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

 # CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr.J.Manjula, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Mrs.K.Suganthi, SRMIST*

Course Code	20ECE632T	Course Name	Radio Frequency VLSI	Course Category	E	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	20ECC533J	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR): The purpose of learning this course is to:

		Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Understand the basic architectures of RF systems and its characteristic parameters, Impedance matching techniques.			
CLR-2 :	Construct the different types of filters.			
CLR-3 :	Utilize the basics of High frequency amplifier design, the operation of Mixers, oscillators, PLL and Frequency synthesizers			
CLR-4 :	Identify different types of Power amplifiers			
CLR-5 :	Understand Various multiple access techniques			
CLR-6 :	Construct LNA, Frequency synthesizer and power amplifier			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Construct impedance matching networks	3	80	70	H	H	H	H	M	M	H	M	M	-	L	-	L	-	-
CLO-2 :	Implement the different types of filters.	3	80	70	H	H	H	H	M	M	H	M	M	-	L	-	L	-	-
CLO-3 :	Describe High frequency amplifier design, the operation of Mixers, oscillators, PLL and Frequency synthesizers	3	80	70	H	H	H	H	M	M	H	M	M	-	L	-	L	-	-
CLO-4 :	Characterize the different types of Power amplifiers	3	80	70	H	H	H	H	M	M	H	M	M	-	L	-	L	-	-
CLO-5 :	Recognize Various multiple access techniques	3	80	70	H	H	H	H	M	M	H	M	M	-	L	-	L	-	-
CLO-6 :	Create LNA, Frequency synthesizer and power amplifier	3	80	85	H	H	H	H	M	M	H	M	M	-	L	-	L	-	-

Duration (hour)		RF Systems 12	Filter Design&High Frequency Amplifier Design 12	Mixers& Oscillators 12	RF Power Amplifiers 12	Multiple Access Techniques & Case Studies 12
S-1	SLO-1	Basic architectures	Performance parameters, Types	- Mixer fundamentals	- General considerations and its performance metrics	: Introduction
	SLO-2	Transmission media and reflections Maximum power transfer	Frequency and impedance scaling	Nonlinear systems as Linear mixers	Types of Power amplifiers	Various multiple access Techniques
S-2	SLO-1	Passive RLC Networks, Parallel RLC tank Circuit	Modern filter design	Multiplier based mixers	Class A & Efficiency Derivation	Wireless standards
	SLO-2	Q factor	Derivation of normalized parameters	Subsampling mixers	Problem Solving on Class A	Mobile RF communication
S-3	SLO-1	Series RLC networks	Low Pass Filter Design	OSCILLATORS - Problems with purely linear oscillators	Class B & Efficiency Derivation	FDMA
	SLO-2	Problems solving on RLC networks	Tutorials on Low Pass Filter Design	Resonators	Problem Solving on Class B	TDMA
S-4	SLO-1	Interconnects and skin effect	High Pass filter design	Tuned oscillator- Hartley, Colpitt	Class AB	CDMA
	SLO-2	Impedance Matching networks- Introduction	Tutorials on High Pass Filter Design	Clapp oscillator	Class C & Efficiency Derivation	CDMA
S-5	SLO-1	Conditions for Impedance matching	Band pass filter design	Problem Solving Tuned Oscillator	Class D	Transceiver Architectures:
	SLO-2	Pi matching network	Tutorials on Band Pass Filter Design	Negative Resistance oscillators	Class E	General considerations
S-6	SLO-1	T matching network	Band reject filter design	Voltage controlled oscillators	Class F	Receiver architecture
	SLO-2	Problems solving on Matching network	Tutorials on Band reject Filter Design	Problem Solving	Linearization Techniques	Receiver architecture- contn.
S-7	SLO-1	Gain Parameters	Effects of finite Q	Phase locked loops : Linearized PLL models	Methods of Linearization	Transmitter Architecture
	SLO-2	Problem Solving using gain parameters	HIGH FREQUENCY AMPLIFIER DESIGN - Zeros as Bandwidth enhances	Phase detectors	Envelope feedback	Transceiver performance tests

S-8	SLO-1	Non-linearity parameters	Shunt-series Amplifier	Charge pumps	Feed forward	Transceiver Design examples
	SLO-2	Problem Solving on Non-linearity parameters	Bandwidth enhancement with frequency Doublers	Loop filters	Pre-Post distortion	Transceiver Design examples
S-9	SLO-1	Noise figure	Bandwidth enhancement with frequency Doublers-Contn. Problem Solving	PLL design	Envelope elimination and restoration	CASE STUDIES: LNA Design
	SLO-2	Phase Noise	Tuned amplifiers	Problem Solving on PLL	LINC	LNA Design
S-10	SLO-1	Dynamic range	Neutralization	Frequency synthesizer: Block diagram description	Efficiency Boosting Techniques	Mixer Design
	SLO-2	Problem Solving on noise figure, phase noise and dynamic range	Unilateralization	Frequency division	Methods of Efficiency boosting	Mixer Design
S-11	SLO-1	RF front end performance parameters	cascaded Amplifiers	Integer-N synthesis	Adaptive bias	Frequency Synthesizer
	SLO-2	Performance tradeoffs in an RF circuit.	Problems solving on RF amplifier design	Fractional frequency synthesis	Doherty amplifier	Frequency Synthesizer
S-12	SLO-1	Problem solving on RF front end parameters	LNA Topologies	Applications of Frequency Synthesis	RF Power amplifier design examples.	Power Amplifier
	SLO-2	Review of MOS Device Physics	LNA Topologies	Problem Solving	RF Power amplifier design examples.	Power Amplifier

Learning Resources	1. *Aleksandar Tasic, Wouter.A.Serdijn, John.R.Long, "Adaptive Low Power Circuits for Wireless Communication (Analog Circuits and Signal Processing)", Springer, 1st Edition, 2006.* 2. *Chris Bowick, "RF Circuit design", Newnes (An imprint of Elesvier Science), 1st Edition, 1997. .* 3. *B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1st Edition, 1998.* 4. *Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 1st Edition, 2002.*	5. *Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 2nd Edition,1999* 6. *Jia-sheng Hong, "Microstrip filters for RF/Microwave applications", Wiley, 1st Edition, 2001.* 7. *Thomas.H. Lee, "The design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd Edition, 2004.*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

 # CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr.J.Manjula, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2.*

Course Code	20ECE633T	Course Name	Machine Learning in VLSI	Course Category	E	Professional Elective	L	T	P	C
							3	1	0	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
CLR-1 :	Provide concise introduction to the fundamental concepts of Machine Learning	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-2 :	introduce neural networks and its algorithm			
CLR-3 :	focus on the backend design challenges, including mask synthesis and physical verification			
CLR-4 :	Study how machine learning can help in physical design			
CLR-5 :	Address the energy efficient design of machine learning hardware			
CLR-6 :	Gain the knowledge of machine learning to apply in VLSI design			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Program Learning Outcomes (PLO)														
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
					Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Understand the basic definitions and concepts of Machine Learning	3	80	80	H	H	H	H	L	-	-	-	M	-	-	-	-	-	-
CLO-2 :	Can explore the applications of neural network algorithms	3	80	80	H	H	H	H	L	-	-	-	M	-	-	-	-	-	-
CLO-3 :	Apply the machine learning in physical verification and mask synthesis	3	70	70	M	M	L	M	M	-	-	-	-	-	-	-	-	-	-
CLO-4 :	Predict the machine learning model for physical design such as placement and routing	3	70	70	M	M	M	M	H	-	-	-	-	-	-	-	-	-	-
CLO-5 :	Analyze the energy efficient machine learning hardware structures.	3	65	60	M	M	M	M	H	-	-	-	-	-	-	-	-	-	-
CLO-6 :	Apply the knowledge of machine learning in VLSI field	3	80	80	H	H	M	M	H	-	-	-	-	-	-	-	-	-	-

Duration (hour)		Unit I- Introduction to Machine Learning	Unit II - Neural Network, Computational Learning Theory and Clustering	Unit III - Machine Learning in Physical Verification and Mask Synthesis	Unit IV - Machine Learning Applications in IC Physical Design	Unit V – Energy Efficient Design of Advanced Machine Learning Hardware
		12	12	12	12	12
S-1	SLO-1	Introduction	Neural Network Introduction	Machine Learning Taxonomy	Machine Learning for Physical Design: Modern VLSI Layouts	Software and Co-design Optimizations
	SLO-2	Basic Definitions	Perceptrons	VLSI CAD Abstraction Levels	IC Design Flow –Silicon Compiler	Pruning in Optimization
S-2	SLO-1	Types of Learning	Limitations of Perceptrons	ML in Physical Verification	Placement and Routing Example	Weight Sharing
	SLO-2	Supervised learning: Classification and Regression	Multilayer Neural Network	Layout Feature Extraction and Hotspot Detection	Correlation between Placement and Routing	Compact Network Architectures
S-3	SLO-1	Unsupervised Learning: Clustering	Back Propagation Algorithm	ML in Mask Synthesis	Challenges for VLSI Design	Hardware–Software Co-design in neural networks
	SLO-2	Density Estimation	Back Propagation Algorithm : Learning in epochs stopping	Mask Synthesis Flow	Datapath Placement	Hardware-Level Techniques
S-4	SLO-1	Reinforcement learning	Deep Neural Networks	Sub-resolution Assist Features	Machine Learning for Placement, Routing, Mask Synthesis and Verification	Dataflows for Accelerators
	SLO-2	Reinforcement learning	Training of neural networks	Optical Proximity Correction (OPC)	VLSI Placement and Algorithm	Architectures for Accelerators
S-5	SLO-1	Hypothesis Space	Introduction to computational learning theory	Machine Learning guided OPC	Advances in Deep Learning Hardware/Software	Deep CNN Accelerators
	SLO-2	Inductive Bias	Sample Complexity	Mask Synthesis and Verification	Analogy between NN Training and Placement	Hardware Friendly Strategies for Deep CNN Accelerators
S-6	SLO-1	Evaluation	Finite hypothesis space	Machine Learning for Clock Optimization	DREAM Place Architecture	Memory-Efficient Architectures
	SLO-2	Cross-Validation	Infinite hypothesis space	Decision tree induction algorithm	DREAM Place Architecture flow	Hardware Architectural Techniques for Leveraging Sparsity in Neural Networks
S-7	SLO-1	Linear Regression	Ensemble Learning : Classification	Importance of Lithographic Patterning Process	MAGICAL Overview	Error Resilience Analysis
	SLO-2	Types of Regression Models	Ensemble Creation and combining Approaches	Representation of Lithographic Patterning Process	Routing Guidance: Genius Route	Energy-Efficient Hardware Accelerator Design Methodology for Neural Networks
S-8	SLO-1	Tutorial on supervised vs unsupervised learning	Bootstrap Method	Machine Learning for Lithography Friendly Routing	Routability-Driven Placement	Deep Neural Networks (DNN): Training and model compression
	SLO-2	Tutorial on regression	Bagging: Bootstrap Aggregation	Image Translation for Lithography Modeling	SRAF Insertion	Efficient Machine Learning Architectures: Challenges and the Way Forward
S-9	SLO-1	Decision Tree	Boosting: Adaptive Boosting (AdaBoost) Algorithms	Mask Verification: Bottleneck in Semiconductor	SRAF Image Translation	Optimizing Memory vs. Computations
	SLO-2	Example for Decision Tree	Gradient Boosting Algorithms	Mask Verification: Bottleneck in IC Manufacturing	Challenges for SRAF Insertion	Neuromorphic Computing
S-10	SLO-1	Overfitting	Clustering	Challenges in Lithography Modeling	Multi-Channel Heat map Encoding	Effective Fixed-Point Quantization
	SLO-2	Pruning	Hierarchical, Model Based and Density Based Clustering	Transfer learning for Lithography Modeling	Multi-Channel Heat map Decoding	H/W and Architectural Optimizations
S-11	SLO-1	Feature Extraction	K-means Clustering	Learning from Limited Data in VLSI CAD: Iterative feature search	Prediction of Routing Congestion	Accuracy vs. Energy Trade-off
	SLO-2	Feature Extraction : Principle components	Example for K-means Clustering	Machine Learning Assumption to enable learning	Challenges of Routing Congestion	Adaptability, (Re-) configurability, and Scalability
S-12	SLO-1	Bayesian Learning	Agglomerative hierarchical clustering	Traditional Machine Learning	Application Specific ML	Run-Time Evolutionary Algorithms for Designing
	SLO-2	Bayesian Network	Divisive hierarchical clustering	An Adjusted machine learning view	Future Directions of ML in physical design	Correct Benchmarking with Fairness and High Fidelity

Learning Resources	1. Lorenzo Rosasco, (2017), Introductory Machine Learning Notes. 2. Ethem Alpaydin, Introduction to Machine Learning, Second Edition.	3. Ibrahim (Abe) M. Elfadel, Duane S. Boning and Xin Li (2019), Machine Learning in VLSI Computer Aided Design.

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	30	-	30	-	30	-	30	-
Level 2	Apply Analyze	40	-	40	-	40	-	40	-
Level 3	Evaluate Create	30	-	30	-	30	-	30	-
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. E. Chitra, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	

Course Code	20ECE634T	Course Name	FUNDAMENTALS OF SOLAR CELL	Course Category	B	Engineering and Technology	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Identify and understands the basics of light and solar irradiance			
CLR-2 :	Uunderstands the basics of PN junction			
CLR-3 :	Analyze and apply PN Jucnction in Solar Cell			
CLR-4 :	Create insights to design of solar cell			
CLR-5 :	Analyze the working principle of high efficiency solar cell			
CLR-6 :	Utilize the concepts in physics to design advance solar cells			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	Identify the principle of light	2	80	70	H	H	-	-	-	-	-	-	-	-	-	-	-	-	-
CLO-2 :	Analyze the concept of PN junction	2	85	75	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CLO-3 :	Apply PN junction theory to design solar cell	2	75	70	H	H	-	H	-	-	-	-	-	-	-	-	-	-	-
CLO-4 :	Apply physical phenomenon to design high efficiency solar cell	2	85	80	H	H	-	-	-	-	-	-	-	-	-	-	-	-	-
CLO-5 :	Identify the basic concepts of Next generation solar cell	2	85	75	H	-	H	-	-	-	-	-	-	-	-	-	-	-	-
CLO-6 :	Technology for analyzing the engineering problems with futuristic approach	2	80	70	-	H	-	H	-	-	H	-	-	-	-	-	-	-	-

Duration (hour)		Unit-I: Solar Irradiance (9 Hours)	Unit-II: PN Junction (9 Hours)	Unit-III: Introduction to Solar Cells (9 Hours)	Unit-IV: High Efficiency Solar Devices (9 Hours)	Unit-V: Next Generation Solar Cells (9 Hours)
S-1	SLO-1	Energy and Climate Change	Semiconductor materials,	Photon In, Electron Out: Photovoltaic effect	Need for high efficiency	Quantum Well (QW) solar cells
	SLO-2	Properties of light, Energy of photon	semiconductor structure	Definition of solar cell	Way to improve efficiency	
	SLO-3	Photon flux, spectral irradiance	conduction in semiconductor, band gap			QWs in tandem cells, QWSCs with light trapping
S-2	SLO-1	Radiant power density	Intrinsic carrier concentration	Electrical characteristics, optical properties	Multijunction solar cell	QWSCs for thermophotovoltaics
	SLO-2	Black body radiation				
	SLO-3	Sun radiation	doping, and equilibrium carrier concentration		Basic concept	Quantum Dot (QD) solar cells
S-3	SLO-1	The Sun, solar radiation in space	Absorption of light, absorption coefficient	Typical solar cell structures, ideal efficiencies.	Dual junction Solar cell	Silicon-QD solar cell
	SLO-2	solar radiation outside the earth's atmosphere	absorption depth, generation rate	Quantum Efficiency, Short Circuit Current, Open Circuit voltage, Fill factor		III-V multi-junction QD solar cells
	SLO-3	terrestrial solar radiation	Types of recombination, life time		Triple and four junction solar cell	
S 4-5	SLO-1	solar radiation at the earth's surface	diffusion length, surface recombination	Manufacturing and properties of Crystalline silicon	Prospects of multijunction solar cell	Intermediate-Band Solar Cells (IBSC)
	SLO-2	atmospheric effects				
S-7	SLO-1	air mass	movement of carriers in semiconductor,	High efficiency laboratory cells	High concentration PV technology	Preliminary concepts and definitions, IBSC

	SLO-2		*diffusion, drift*			*model*
S-8	***SLO-1***	*motion of the sun, solar time*	*Formation of a PN junction*	*screen-printed cells, laser-processed cells*	*Classification of CPV*	*Nanowire (NW) solar cells, Silicon NW solar cells*
	SLO-2					
S-9	***SLO-1***	*declination angle, elevation angle, azimuth angle*	*PN junction diode, bias of PN junctions, diode equations, diode equation for PV*	*HIT cell, rear-contacted cells*	*merits and status of CPV*	*compound semiconductor NW solar cells*
	SLO-2					
S-8	*SLO-1*	*the sun's position, solar radiation on a tilted surface arbitrary orientation*	*ideal diode equation derivation, basic equations for PN Junction*	*thin silicon solar cells – light trapping, voltage enhancements*	*Overview of HCPV modules*	*Hydrogenated amorphous silicon thin film solar cell*
	SLO-2					
S-9	*SLO-1*	*calculation of solar insulation, measurement of solar radiation*	*Solving for depletion region and quasi-neutral regions, finding total current.*	*silicon deposition and crystal growth*	*Disadvantages of multijunction solar cell*	*CdTe, CIGS and CZTS Solar Cell*
	SLO-2					

Learning Resources	1. **Pallab Bhattacharya**, *Semiconductor Opto electronics Devices, 2nd ed, PHI, 2017* 2. *Peter Wurfel, Physics of Solar cells,* Wiley-VCH; 2nd ed, 2009	3. *A. Martí, A. Luque, "Next Generation Photovoltaics: High Efficiency through Full Spectrum Utilization", Illustrated edition, CRC Press, 2010* 4. *Arvind Shah, "Thin-Film Silicon Solar Cells", Illustrated edition, EPFL Press, 2010*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)				Final Examination (50% weightage)
		CLA – 1 (10%)	CLA – 2 (15%)	CLA – 3 (15%)	CLA – 4 (10%)#	
		Theory	Theory	Theory	Theory	Theory
Level 1	Remember	*40%*	*40%*	*40%*	*40%*	*30%*
	Understand					
Level 2	Apply	*40%*	*40%*	*40%*	*40%*	*40%*
	Analyze					
Level 3	Evaluate	*20%*	*20%*	*20%*	*20%*	*30%*
	Create					
	Total	100 %	100 %	100 %	100 %	100 %

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
	Dr. G. P. Mishra, National Institute of Technology Raipur	*Dr. Soumyaranjan Routray, SRMIST*
	Dr. K. P. Pradhan, IIITDM, Kancheepuram, Chennai	

Course Code	20GNS501J	Course Name	RESEARCH PUBLISHING AND PRESENTING SKILLS	Course Category	S	Skill Enhancement	L	T	P	C
							1	0	2	2

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	English and Foreign Languages	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	*Practice different oral presentation material preparations*
CLR-2 :	*Practice presenting techniques suitable for different audiences*
CLR-3 :	*Prepare and typeset scientific documents for disseminating research findings*
CLR-4 :	*Analyze different disseminating techniques available*
CLR-5 :	*Utilize different intellectual property sharing mechanisms*
CLR-6 :	*Evaluate amongst different options available to present, publish research findings*

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	*Identify different oral presentation elements, materials and technologies*	3	85	80	L	H	H	M	M	-	L	H	M	-	H	-	L	-	M
CLO-2 :	*Practice high impact presentation skills*	3	85	80	L	H	H	M	M	-	L	H	M	-	H	-	L	-	M
CLO-3 :	*Identify ways to present technical / scientific content structure and elements*	3	85	80	L	H	H	M	M	-	L	H	M	-	H	-	L	-	M
CLO-4 :	*Practice the different disseminating techniques used in scientific research findings*	3	85	80	L	H	H	M	M	-	L	H	M	-	H	-	L	-	M
CLO-5 :	*Identify intellectual property and its components, ways to protect, share intellectual information*	3	85	80	L	H	H	M	M	-	L	H	M	-	H	-	L	-	M
CLO-6 :	*Analyze the different oral and written publishing techniques to disseminate research findings*	3	85	80	L	H	H	M	M	-	L	H	M	-	H	-	L	-	M

Duration (hour)		Oral Content Preparation	Presenting Methods	Written Content Preparation	Publishing Methods	Intellectual Property & Plagiarism
		9	9	9	9	9
S-1	SLO-1	*Oral Presentation Structure: Manuscript, Impromptu, Memory, Extempore*	*Describe Audience; knowledge, Experience, Needs, Goals*	*Writing Preface, Prelude, Prologue, foreword, Introduction, Abstract,*	*Typesetting: LaTex, Word, XML etc.,*	*Public License, Creative Commons, Share-alike, Reciprocal License,*
	SLO-2	*context, need, agenda ,task, and object of the presentation document*	*Plan, Prepare, Practice, Present Creating a Positive First Impression,*	*Writing Dedication, Acknowledgement, Forward, Background*	*Indexing: ISI, SCI, SCIE, SCOPUS, SCIMAGO, ESCI, WoS,*	*Copyleft, Patentleft, Open patent, Public Domain*
S 2-3	SLO-1	*Practice-1: Create Structure of a Presentation*	*Practice-4: Building rapport with Audience*	*Practice-7: Writing Preface, Prelude, Prologue, foreword, Introduction, Abstract*	*Practice-12: LaTex Editor, Word Editor*	*Practice-13: GNU-GPL, Public License Creative Commons License, Unlicense*
	SLO-2					
S-4	SLO-1	*Gather data, evidence to present, visual-auditory balance, engagement techniques*	*Increasing Credibility, Presenting Complex Material, Communicating with Impact*	*Literature Review: Narrative, Systematic, Argumentative, Integrative, Theoretical*	*Disseminating Research Findings: Public Domain, Open Information, Wikipedia*	*Intellectual Property Rights, Copyrights, Patents, Trademarks, and Trade secrets*
	SLO-2	*Introduction, body, closure, question-answer*	*Motivating Others, Responding to Pressure Situations, Inspiring People*	*Writing Problem Statement, Limitations, Method Adapted, Tools & Technology used*	*Media, Press Release, Flyers, Brochure, Research Summary, Posters, Websites*	*Industrial design rights, Plant variety rights, trade dress, geographical indications*
S 5-6	SLO-1	*Practice-2: Create a structured oral presentation module*	*Practice-5: Communicating with Greater Impact, Rehersals and Retrials*	*Practice-8: Writing Literature Review*	*Practice-11: Study of Various Open Publishing Methods*	*Practice-14: IPR Law, Private Domain*
	SLO-2					
S-7	SLO-1	*Tools: Presentation Slides, Whiteboard Animators, Immersive Technologies*	*Delivery Styles: Visual, Freeform, Lessig Instructor, Coach, Storytelling, Connector*	*Main Body: Analysis, Design, Development Steps, Implementation Steps, Evaluations*	*Patents, Journals, Conferences, Reports, RFCs etc.,*	*Infringements: Copylefts, Copyrights, Patentlefts, Patentrights,*
	SLO-2	*Handouts, Visual Aids, Demonstrative Aids, Thought Provoking Questions*	*Persuasive, Interactive, Decision Making, Educational, Takahasi Arousing*	*Referencing: Documentary, Parenthetical, Numbered, Vancouver, IEEE, Harvard etc.,*	*Journal Index, Impact Factor, Quality Standards*	*Plagiarism: Paraphrasing, Verbatim, Mosaic, Global, Self, Accidental etc.,*
S 8-9	SLO-1	*Practice-3: Demonstrating a multi technology oral presentation*	*Practice-6: Presenting same content using different delivery styles*	*Practice-9: Writing Main Body*	*Practice-12:Study of h-index, i10-index, g-index, r-index, π - index*	*Practice-15: Plagiarism checking and correcting techniques*
	SLO-2					

Learning Resources	
1. Dale Carnegie, "Develop Self-Confidence, Improve Public Speaking", Amazing Reads, 2018 *2. Dale Carnegie, "The Art of Public Speaking", Amazing Reads, 2018* *3. Joseph Mugah, "Essentials of Scientific Writing: How to Write Effective Titles and Abstracts for Research Papers and Proposals", Authorhouse, 2016*	*4. Rajesh Singh, Sanjeev Kumar Sinha, Samir Kumar, "Unfolding Intellectual Property Rights : A Practical Patent Guide for Researchers, Academicians and start-ups", Notion Press, 2019* *5. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016*

Learning Assessment									
	Bloom's Level of Thinking	Continuous Learning Assessment (60% weightage)						Final Examination (40% weightage)	
		CLA – 1 (20%)		CLA – 2 (25%)		CLA – 3 (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Understand								
Level 2	Apply	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
	Analyze								
Level 3	Evaluate	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Dr. Sainarayanan Gopalakrishnan, HCL Technologies, sai.jgk@gmail.com	*1. Dr. Venkat Adhikari, Technology Licensing Manager, IISC, venkatadhikari@iisc.ac.in*	*1. Dr. Rajeev Sukumaran SRMIST*
2. Dr. Sricharan Srinivasan, Wipro Technologies, sricharanms@gmail.com	*2. Mr. Ateet Palmurkar, Senior Manager IP Licensing, IITM, ipmarketing@iitm.ac.in*	*2. Dr. V. Nithyananthan SRMIST*

Course Code	20ECS500T	Course Name	RESEARCH METHODOLOGY FOR ELECTRONICS AND COMMUNICATION ENGINEERS	Course Category	S	Skill Enhancement	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	NIL
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	NIL		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Learn to plan and prepare for research			
CLR-2 :	Know about various Research Resources			
CLR-3 :	Know ways of academic writing and presentation			
CLR-4 :	Learn ideas on data collection, analysis and inference			
CLR-5 :	Perform case studies pertaining to various domain of study			
CLR-6 :	Study the concepts of research and its methodology			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)															
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning	
CLO-1 :	Cover an overview of Research Preparation and Planning	2	80	70	H	H	-	H	-	-	-	-	-	-	-	-	-	-	-	
CLO-2 :	Analyse the different Research Resources	2	80	70	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	
CLO-3 :	Update knowledge onAcademic Writing & Presentation	2	80	70	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	
CLO-4 :	Gain complete knowledge on Data Collection, Analysis and Inference	2	80	70	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	
CLO-5 :	Perform Case Studies and Applications in various domain of study	2	80	70	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	
CLO-6 :	Gain thorough knowledge about research and its methodology	2	80	70	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	

Duration (hour)		Research Preparation and Planning	Research Resources	Academic Writing & Presentation	Data Collection, Analysis and Inference	Case Studies and Applications
		12	12	12	12	12
S-1	SLO-1	. Objectives of research	Sources of information.	Proposal submission for funding agencies, Elements of Style	Basic Statistical Distributions and their applications: Binomial Distribution.	Case study :Research Basics in IOT/Physical Design Automation/Cryptography and coding.
	SLO-2			Organization of proposals	Poisson, Normal Distribution	
S-2	SLO-1	Understanding research and its goals	Literature search	Organization of proposals	Exponential Distribution	Case study: Survey in IOT/Physical Design Automation/Cryptography and coding
	SLO-2			Basic knowledge of funding agencies	Weibull and Geometric Distributions	
S-3	SLO-1	Critical thinking	World Wide Web, Online data bases – search tools	Research report writing	Sample size determination & sampling techniques: Random sampling	Case study: Presentation in IOT/Physical Design Automation/Cryptography and coding
	SLO-2				Stratified sampling	
S-4	SLO-1	Techniques for generating research topics.	Citation indices	Communication skills	Systematic sampling	Case study :Research Basics in System Architecture/RF VLSI/Optical Wireless Communication
	SLO-2	Techniques for generating research topics	Citation indices	Tailoring the presentation to the target audience	Cluster sampling	
S-5	SLO-1	Techniques for generating research topics	Principles underlying impact factor	Oral presentations	Large Sample Tests and Small Sample Tests	Case study: Survey in System Architecture/RF VLSI/Optical Wireless Communication
	SLO-2	Topic selection and justification	Principles underlying impact factor	Oral presentations	Student–t-test and its application in research studies	
S-6	SLO-1	Topic selection and justification	Literature review	Poster preparations	F-test and its application in research studies	Case study:Presentation in System Architecture/RF VLSI/Optical Wireless Communication
	SLO-2	Techniques involved in designing a questionnaire	Literature review	Poster preparations	$\chi 2$ test and its application in research studies	
S-7	SLO-1	Techniques involved in designing a	Case studies, review	Submission of research articles for	Correlation and Regression Analysis-Time	Case study :Research Basics in

		questionnaire	articles and Meta analysis	Publication to Reputed journals	series analysis	RTOS/Hardware Securuty/Signal Processing
	SLO-2	Techniques involved in designing a questionnaire	Case studies, review articles and Meta analysis	Submission of research articles for Publication to Reputed journals,	Forecasting methods	
S-8	SLO-1	Methods of scientific enquiry	record of research review	Thesis writing,	Factor analysis,	Case study: Survey in RTOS/Hardware Securuty/Signal Processing
	SLO-2	Methods of scientific enquiry	Role of the librarian.	Thesis writing	Cluster Analysis and Discriminant Analysis (Basic ideas only).	
S-9	SLO-1	Formulation of hypotheses	Ethical Issues in Research,	Research report writing.	Principles of Experimentation, Basic Experimental Designs:	Case study:Presentation in RTOS/Hardware Securuty/Signal Processing
	SLO-2	Formulation of hypotheses	Moral Issues in Research	Research report writing	Completely Randomized Design	
S-10	SLO-1	Testing of the hypotheses	Plagiarism	Elements of excellent presentation:	Randomized Block Design	Case study: Research Basics in Robotics/Low power design techniques /Wireless Communication
	SLO-2	Testing of the hypotheses	Tools to avoid plagiarism	Elements of excellent presentation	Latin Square Design	
S-11	SLO-1	Development of a research proposal	Intellectual Property Rights	Preparation, Visual and Delivery	Factorial Designs: 2^2	Case study: Survey in Robotics/Low power design techniques /Wireless Communication
	SLO-2	Development of a research proposal	Intellectual Property Rights	Oral Communication skills	Factorial Designs: 2^3	
S-12	SLO-1	Theoretical and Experimental Processes	Copy right laws	Oral Communication skills	Factorial Designs: 2^4	Case study:Presentation in Robotics/Low power design techniques /Wireless Communication
	SLO-2	Theoretical and Experimental Processes	Patent rights	Oral defence	Accuracy, Precision and error analysis	

Learning Resources

1. Ganesan R, Research Methodology for Engineers, MJP Publishers, Chennai. 2011
2. Walpole R.A., Myers R.H., Myers S.L. and Ye, King: Probability & Statistics for Engineers and Scientists, Pearson Prentice Hall, Pearson Education, Inc. 2007.
3. Anderson B.H., Dursaton, and Poole M.: Thesis and assignment writing, Wiley Eastern 1997.
4. Bijorn Gustavii: How to write and illustrate scientific papers? Cambridge University Press.
5. Bordens K.S. and Abbott, B.b.: Research Design and Methods, Mc Graw Hill, 2008.
6. Graves N, Varma V: Working for a doctorate Toutledge 1997.
7. Graziano, A., M., and Raulin, M.,L.: Research Methods – A Process of Inquiry, Sixth Edition, Pearson, 2007.
8. Leedy., P., D.: Practical Research – Planning and Design, Eighth Edition, Pearson., 2005.
9. Kothari C.K., Research Methodology - Methods and Techniques (New International, New Delhi), 2004.
10. Stamatios V. Kartalopoulos, DWDM Networks devices and technology, IEEE Press,Wiley, 2003

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination (40% weightage)	
		CLA-1 (20%)		CLA-2 (25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	*1. Dr. J. Subhashini, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	

Course Code	20MAC507T	Course Name	APPLIED MATHEMATICS FOR VLSI	Course Category	C	Professional Core	L	T	P	C
							4	0	0	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Mathematics	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Idea of Basics of Graph Theory			
CLR-2 :	Understand and apply shortest path algorithms			
CLR-3 :	Solving PDE using finite difference method			
CLR-4 :	To get ability to solve linear programming problems and its uses			
CLR-5 :	Use discrete time finite state Markov chain			
CLR-6 :	Solve problems of shortest path, optimization, differential equation and Markovian model and implement in engg problems			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Students will get idea of different types of graphs and their representation with basic theorems	1	85	80	L		L					M	M						H
CLO-2 :	Students will be introduced planarity and coloring of graphs, matrix representation and finding shortest path and distance	2	85	80	L		L	M	M		M	M							H
CLO-3 :	Students will be able to find numerical solution of different types of PDE	2	85	80	L	M	M		L			M	M						H
CLO-4 :	Students will be able to find optimal solution of linear programming problem	2	85	80	L	M	M	M	L		M	M	M						H
CLO-5 :	Students will be able to specify a given discrete and Markov chain in terms of a transition matrix & transition diagram	3	85	80	L	M	L		M			M	M						H
CLO-6 :	To solve the problems of shortest path, optimization, differential equation and Markovian model in science and engineering	3	85	80	L	M	L		M			M	M						H

Duration (hour)		Module 1/ Basics of Graph Theory	Module2 / Matrix representation and Traversal Algorithm	Module 3/ Numerical solutions of PDE	Module 4/ Optimization Technique	Module 5/ Stochastic Processes
		12	12	12	12	12
S-1	SLO-1	Introduction to graphs	Cut-sets and Cut-vertices	Introduction to Partial differential equations	Introduction to operations research	Classification of stochastic processes
	SLO-2	Different types of graphs	Properties of a Cut-set	Classification of PDE	Linear programming problem	Methods and Description
S-2	SLO-1	Basic theorems related to graphs	Fundamental Circuits and cut-sets	Classification of PDE	Basic definitions on LPP	Random process - Characteristics
	SLO-2	Basic theorems related to graphs	Fundamental Circuits and cut-sets	Numerical solutions for PDE	Basic definitions on LPP	Special cases of Random process and its average values
S-3	SLO-1	Basic theorems related to graphs	Networks flow	Elliptic equations	Solving L.P.P by graphical method	Introduction to Markov process
	SLO-2	Basic theorems related to graphs	Maximum flow and minimum cut theorems	Solution of elliptic equations	Solving L.P.P by graphical method	Definition of a Markov chain
S-4	SLO-1	Subgraphs	Matrix representation of graphs	Solution of Laplace equation by Leibmann's iterative process	Simplex method	Markov chain one step
	SLO-2	Different types of Subgraphs	Matrix representation of graphs	Solution of Laplace equation by Leibmann's iterative process	Simplex method	Markov chain n-step transition probability
S-5	SLO-1	Operations on graphs	Matrix representation of directed graphs	Problems on Laplace equation	Solving problems using simplex method	Transition Probability Matrix (TPM)
	SLO-2	Union and intersection of graphs	Matrix representation of directed graphs	Problems on Laplace equation	Solving problems using simplex method	Characteristics of TPM
S-6	SLO-1	Decomposition and deletion of graphs	Traversal Algorithm	Solution of Poisson equations	More Problems using simplex method	Constructing TPM

	SLO-2	Fusion of graphs	DFS algorithm	Problems on Poisson equations	More Problems using simplex method	Chapman Kolmogorov theorem (statement only)
S-7	SLO-1	Euler Graphs	BFS algorithm	Solution of Parabolic equations	Introduction to transportation problems	Applications on Chapman Kolmogorov Theorem
	SLO-2	Standard theorems on Euler Graphs	Prim's algorithm	Bendre-Schmidt method for Parabolic equations	Applications of transportation problems	Applications on Chapman Kolmogorov Theorem
S-8	SLO-1	Standard theorems on Euler Graphs	Problems on Prim's algorithm	Problems on Parabolic equations using Bendre-Smidth formula	Problems solving by least cost method and north west corner rule.	Problems on TPM using Chapman Kolmogorov Theorem
	SLO-2	Hamilton Graphs	Problems on Prim's algorithm			
S-9	SLO-1	Standard theorems on Hamilton Graphs	Kruskal algorithms	Crank-Nicolson difference method for Parabolic equations	Problems using vogel's approximation	Transition probability -Applications
	SLO-2	Standard theorems on Hamilton Graphs	Problems on Kruskal algorithms	Crank-Nicolson difference method for Parabolic equations	Problems using vogel's approximation	Transition probability -Applications
S-10	SLO-1	Trees and Rooted trees	Problems on Kruskal algorithms	Problems on Parabolic equations using Crank-Nicolson formula	MODI Method	Limiting distributions -Applications
	SLO-2	Basic theorems	Shortest path algorithms	Problems on Parabolic equations using Crank-Nicolson formula	MODI Method	Limiting distributions - Applications
S-11	SLO-1	Spanning trees	Dijskra's algorithms	Solution of Hyberbolic equations	Introduction to assignment problems	Classifications of states of a Markov chain
	SLO-2	Properties of Spanning trees	Dijskra's algorithms	Explict formula for Hyberbolic equations	Assignment problems	Problems on Classification of states of a Markov chain
S-12	SLO-1	Steiner tree	Problems on Dijskra's algorithms	Problems on Hyberbolic equations using Explict formula	Hungarian method for Assignment problems	Problems on Classification of states of a Markov chain
	SLO-2	Steiner tree problem	Problems on Dijskra's algorithms	Problems on Hyberbolic equations using Explict formula	Assignment problems using Hungarian method	Applications on Classification of states of a Markov chain

Learning Resources	1. Narsingh Deo, Graph Theory With Applications to Engineering and Computer Science, Prentice Hall India Learning Private Limited,New Delhi, 2003. 2. B.S. Grewal, Numerical Methods in engineering and science, Khanna Publishers, 42nd edition, 2012.	3. Rao S.S.,Engineering Optimization: Theory and Practice, New Age International Pvt. Ltd.,3rd Edition 1998. 4. Ross Sheldon M., Stochastic Processes, 2nd Wiley India Pvt. Ltd,New Delhi, 2008.

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1(20%)		CLA-2(25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	30	-	30	-	30	-	30	-
Level 2	Apply Analyze	40	-	40	-	40	-	40	-
Level 3	Evaluate Create	30	-	30	-	30	-	30	-
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr.V.Maheshwaran, CTS, Chennai, maheshwaranv@yahoo.com	1. Dr. Y.V.S.S. Sanyasi Raju, IIT Madras, sryedida@iitm.ac.in	1. .Dr. A. Govindarajan, SRMIST
2.	2. Dr.K.C.Sivakumar, IIT Madras, kcskumar@iitm.ac.in	2. Dr. V. Srinivasan, SRMIST

Course Code	20PDM501T	Course Name	Career Advancement Course for Engineers-I	Course Category	M	Mandatory	L	T	P	C
							1	0	1	0

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Career Development Centre	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1 :	Become an expert in communication and problem solving skills
CLR-2 :	Recapitulate fundamental mathematical concepts and skills
CLR-3 :	Strengthen writing skills professionally and understand commercial mathematical applications
CLR-4 :	Identification of relationships between words based on their function, usage and characteristics
CLR-5 :	Sharpen logical and critical reasoning through skillful conceptualization
CLR-6 :	Acquire the right knowledge, skill and aptitude to face any competitive examination

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	Acquire communication and problem solving skills	2	80	75	-	H	-	H	-	-	-	-	H	H	-	H	-	-	-
CLO-2 :	Build a strong base in the fundamental mathematical concepts	2	75	70	-	H	-	H	-	-	-	-	H	H	-	H	-	-	-
CLO-3 :	Acquire writing skill to communicate with clarity	2	80	75	-	H	-	H	-	-	-	-	H	H	-	H	-	-	-
CLO-4 :	Use apt vocabulary to embellish language	3	75	70	-	H	-	H	-	-	-	-	H	H	-	H	-	-	-
CLO-5 :	Gain appropriate skills to succeed in preliminary selection process for recruitment	3	85	80	-	H	-	H	-	-	-	-	H	H	-	H	-	-	-
CLO-6 :	Enhance aptitude skills though systematic application of knowledge	2	85	80	-	H	-	H	-	-	-	-	H	H	-	H	-	-	-

Duration (hour)		6	6	6	6	6
S-1	SLO-1	Types of numbers, Divisibility tests	Fractions and Decimals, Surds	Percentage - Introduction	Sentence Correction	Number and Alphabet Series
	SLO-2	Solving Problems	Solving Problems	Solving Problems	Practice	Direction Test
S-2	SLO-1	LCM and GCD	Square roots, Cube roots, Remainder	Percentage Problems	Reading Comprehension	Blood Relations
	SLO-2	Solving Problems	Solving Problems	Solving Problems	Practice	Arrangements Linear, Circular
S-3	SLO-1	Unit digit, Number of zeroes, Factorial notation	Identities	Profit and Loss	Reading Comprehension	Ranking
	SLO-2	Solving Problems	Solving Problems	Solving Problems	Practice	Practice
S-4	SLO-1	Verbal Reasoning-Vocabulary	Spotting Errors	Discount	Reading Comprehension	Critical Reasoning-Strengthening
	SLO-2	Practice	Practice	Solving Problems	Practice	Practice
S-5	SLO-1	Verbal Reasoning-Vocabulary	Spotting Errors	Sentence Correction	Linear Equations	Critical Reasoning-Weakening
	SLO-2	Practice	Practice	Practice	Solving Problems	Practice
S-6	SLO-1	Verbal Reasoning-Vocabulary	Spotting Errors	Sentence Correction	Logical Reasoning-Intro	Critical Reasoning-Assumption
	SLO-2	Practice	Practice	Practice	Coding and Decoding	Practice

Learning Resources

1. Khattar D. "Quantitative Aptitude", Pearson's Publications, Third Edition (2015).
2. Praveen R.V. "Quantitative Aptitude and Reasoning", EEE Publications, Third Edition (2016)
3. Guha A. "Quantitative Aptitude", TATA McGraw Hill Publications, Sixth Edition (2017).
4. P.A. Anand, "Quantitative Aptitude for Competitive Examination", WILEY Publications (2019)
5. Arihant. "IBPS PO - CWE Success Master", Arihant Publications(I) Pvt.Ltd – Meerut, First Edition (2018)
6. Nishit Sinha. "Verbal Ability for CAT", Pearson India, First Edition (2018).
7. Archana Ram, "Placementor", Oxford University Press, (2018)
8. Bharadwaj A.P. " General English for Competitive Examination", Pearson Education, First Edition (2013)
9. Thorpe S. "English for Competitive Examination", Pearson Education, Sixth Edition (2012).

Learning Assessment							
	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)				Final Examination (40% weightage)	
		CLA-1 (30%)		CLA-2 (30%)		Fully Internal	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	40 %	-	30 %	-	30 %	-
	Understand						
Level 2	Apply	40 %	-	40 %	-	40 %	-
	Analyze						
Level 3	Evaluate	20 %	-	30 %	-	30 %	-
	Create						
	Total	100 %		100 %		100 %	

Note: CLA-2 (Surprise Test, Assignment-1, Assignment-2)

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Ajay Zener, Career Launcher, ajay.z@careerlauncher.com		1. Dr. P. Madhusoodhanan, SRMIST 2. Dr. M. Snehalatha,, SRMIST
		3. Mr. J.Jayapragash, SRMIST 4. Dr. A. Clement, SRMIST

Course Code	20PDM502T	Course Name	Career Advancement Course For Engineers - II	Course Category	M	Mandatory	L	T	P	C
							1	0	1	0

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Career Development Centre	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Recapitulate fundamental mathematical concepts and building the resume			
CLR-2 :	Become an expert in communication and problem solving skills			
CLR-3 :	Sharpen interpretational skills through skillful conceptualization,			
CLR-4 :	Sharpen analytical reasoning skills and professional skills			
CLR-5 :	Utilize professionalism with idealistic, practical and moral values that govern the behavior			
CLR-6 :	Acquire the right knowledge, skill and aptitude to face any competitive examination			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	Build a strong base in the fundamental mathematical concepts and resume	2	80	75	-	H	-	M	-	-	-	-	H	H	-	H	-	-	-
CLO-2 :	Acquire communication and problem solving skills.	2	75	70	-	H	-	M	-	-	-	-	H	H	-	H	-	-	-
CLO-3 :	Gain appropriate skills to succeed in preliminary selection process for recruitment	2	80	75	-	H	-	M	-	-	-	-	H	H	-	H	-	-	-
CLO-4 :	Acquire interpretational skills and professional skills	3	75	70	-	H	-	M	-	-	-	-	H	H	-	H	-	-	-
CLO-5 :	Develop professionalism with idealistic, practical and moral values	3	85	80	-	H	-	M	-	-	-	-	H	H	-	H	-	-	-
CLO-6 :	Enhance lexical skills through systematic application of concepts and careful analysis of style, syntax, semantics and logic	2	85	80	-	H	-	M	-	-	-	-	H	H	-	H	-	-	-

Duration (hour)		6	6	6	6	6
S-1	SLO-1	Ratio and Proportion-Intro	Sets-Rules	Group Discussion-3	Data Sufficiency-Intro	Personal Interview
	SLO-2	Solving Problems	Solving Problems	Practice	Solving Problems	Practice
S-2	SLO-1	Ratio and Proportion	Sets-Identities, Venn Diagram	Group Discussion-4	Data Sufficiency	Personal Interview
	SLO-2	Solving Problems	Solving Problems	Practice	Solving Problems	Practice
S-3	SLO-1	Mixture and Solutions-Intro	Functions-Intro	Group Discussion-5	Analytical Reasoning-Intro	Mock Interview
	SLO-2	Solving Problems	Solving Problems	Practice	Solving Problems	Mock Interview
S-4	SLO-1	Mixture and Solutions	Group Discussion- Do's and Don'ts	Data Interpretation-Intro	Analytical Reasoning	Mock Interview
	SLO-2	Solving Problems	Practice	Solving Problems	Solving Problems	Mock Interview
S-5	SLO-1	Profile Building	Group Discussion-1	Data Interpretation-Tables, Pie Chart	Personal Interview-Do's and Don'ts	Mock Interview
	SLO-2	Profile Building	Practice	Solving Problems	Practice	Mock Interview
S-6	SLO-1	Resume Building	Group Discussion-2	Data Interpretation-Lines, Bar Graphs	Personal Interview	Quantitative Reasoning Revision
	SLO-2	Resume Building	Practice	Solving Problems	Practice	Solving Problems

Learning Resources	*1. Khattar D. "Quantitative Aptitude", Pearson's Publications, Third Edition (2015).* *2. Guha A. "Quantitative Aptitude", TATA McGraw Hill Publications, Sixth Edition (2017).* *3. Butterfield J. "Soft Skills for Everyone", Cengage Learning India Private Ltd, First Edition, (2011).*	*4. Bono E.D. "Six Thinking Hats is a book" , Little Brown and Company, First Edition (1981)* *5. P.A. Anand, "Quantitative Aptitude for Competitive Examination", WILEY Publications (2019)* *6. Archana Ram, "Placementor", Oxford University Press, (2018)*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)				Final Examination (40% weightage)	
		CLA-1 (30%)		CLA-2 (30%)		Fully Internal	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	40 %	-	30 %	-	30 %	-
	Understand						
Level 2	Apply	40 %	-	40 %	-	40 %	-
	Analyze						
Level 3	Evaluate	20 %	-	30 %	-	30 %	-
	Create						
	Total	100 %		100 %		100 %	

Note: CLA-2 (Surprise Test, Assignment-1, Assignment-2)

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Ajay Zener, Career Launcher, ajay.z@careerlauncher.com		1. Dr. P. Madhusoodhanan, SRMIST 2. Dr. M. Snehalatha,, SRMIST
		3. Mr.P.Priyanand, SRMIST 4. Mrs.Kaviatha Srisarann, SRMIST

Course Code	20PDM601T	Course Name	Career Advancement Course For Engineers - III	Course Category	M	Mandatory	L	T	P	C
							1	0	1	0

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Career Development Centre	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	acquire knowledge on planning, preparing and designing a learning program			
CLR-2 :	prepare effective learning resources for active practice sessions			
CLR-3 :	facilitate active learning with new methodologies and approaches			
CLR-4 :	create balanced assessment tools			
CLR-5 :	hone teaching skills for further enrichment			
CLR-6 :	define standards, goals and objectives			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	Build a strong foundation in designing a lesson plan	2	80	75	-	H	H	H	M	-	-	-	H	H	-	H	-	-	-
CLO-2 :	Acquire knowledge of learning resources for effective delivery	2	75	70	-	H	H	H	M	-	-	-	H	H	-	H	-	-	-
CLO-3 :	Sharpen teaching skills with the latest methodologies and techniques	2	80	75	-	H	H	H	M	-	-	-	H	H	-	H	-	-	-
CLO-4 :	Develop practical assessment tools to ensure validity and flexibility	3	75	70	-	H	H	H	M	-	-	-	H	H	-	H	-	-	-
CLO-5 :	Enhance effective presentation and teaching methods	3	85	80	-	H	H	H	M	-	-	-	H	H	-	H	-	-	-
CLO-6 :	Reinforce Bloom's Taxonomy of educational goals and objectives	2	85	80	-	H	H	H	M	-	-	-	H	H	-	H	-	-	-

Duration (hour)		6	6	6	6	6
S-1	SLO-1	Lower and Higher order learning	Definition and purpose of assessment	Peer Teaching practice	Live Teaching Sessions	Live Teaching Sessions
	SLO-2	Outcomes from lower order learning	Practice	Discussion and feedback	Live Teaching Sessions	Live Teaching Sessions
S-2	SLO-1	Planning and preparing a learning programme and session	Distinction between formative and summative assessment	Peer Teaching practice	Live Teaching Sessions	Live Teaching Sessions
	SLO-2	Practice	Examples and discussions	Discussion and feedback	Live Teaching Sessions	Live Teaching Sessions
S-3	SLO-1	Teacher and Student-Centered class room	Instructional materials	Cooperative learning procedure	Live Teaching Sessions	Live Teaching Sessions
	SLO-2	Discussion	Examples and discussion	Different models of cooperative learning	Live Teaching Sessions	Live Teaching Sessions
S-4	SLO-1	Roles of teachers and students	Instructional design	Limitations of cooperative learning	Live Teaching Sessions	Live Teaching Sessions
	SLO-2	Discussion	Practice	Discussion	Live Teaching Sessions	Live Teaching Sessions
S-5	SLO-1	Discussion Strategies	Presentation of lesson plans	Structure of a lecture	Live Teaching Sessions	Live Teaching Sessions
	SLO-2	Practice	Discussion	Practice	Live Teaching Sessions	Live Teaching Sessions
S-6	SLO-1	Bloom's Taxonomy of educational goal	Group Work in learning	Live Teaching Sessions	Live Teaching Sessions	Live Teaching Sessions
	SLO-2	Practice	Discussion	Live Teaching Sessions	Live Teaching Sessions	Live Teaching Sessions

Learning Resources	1. *Barker I. "Cambridge International Diploma for Teachers and Trainers", Cambridge University Press, 2006.* 2. *Whitehead Jack, Creating a Living Educational Theory from Questions of the kind: How do I improve my Practice? Cambridge Journal of Education, 2006.*	3. *Vicki Phillips and Lynn Olson, "Ensuring Effective Instruction: How do I improve teaching using multiple measures?"Bill & Melinda Gates Foundation, 2013.* 4. *Dr G M Chaudhary, "Teaching Methodology: Effective Teaching Strategies", Independently Published, 2019.*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)				Final Examination (40% weightage)	
		CLA-1 (30%)		CLA-2 (30%)		Fully Internal	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	40 %	-	30 %	-	30 %	-
	Understand						
Level 2	Apply	40 %	-	40 %	-	40 %	-
	Analyze						
Level 3	Evaluate	20 %	-	30 %	-	30 %	-
	Create						
	Total	100 %		100 %		100 %	

Note: CLA-2 (Surprise Test, Assignment-1, Assignment-2)

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Ajay Zener, Career Launcher, ajay.z@careerlauncher.com		1. Dr. P. Madhusoodhanan, SRMIST 2. Dr. M. Snehalatha,, SRMIST
		3. Mr. J.Jayapragash, SRMIST 4. Dr. A. Clement, SRMIST

Course Code	20ECP601L	Course Name	INTERNSHIP	Course Category	P	Project Work, Internship In Industry / Higher Technical Institutions	L	T	P	C
							0	0	8	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
CLR-1 :	Provide an exposure to an industrial environment or research laboratory / institution	1	2	3
CLR-2 :	Acquire practical knowledge of theoretical concepts	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-3 :	Understand the organization structure, functions and protocols			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning		
CLO-1 :	Appreciate the functioning of an organization	1	70	65
CLO-2 :	Apply the theoretical concepts to solve engineering problems	2	80	75
CLO-3 :	Take up different roles in a career with confidence	3	65	60

Program Learning Outcomes (PLO)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	H	H	H	H	M	H	H	H	M	H	M	M	M	L	M
CLO-2 :	H	H	H	H	H	H	H	H	H	M	H	M	H	H	H
CLO-3 :	H	M	L	L	M	M	M	M	L	L	L	L	L	M	M

1. It is mandatory for every student to undergo this course.
2. Every student is expected to spend a minimum of 4 to 6 weeks in an Industry/ Company/ Organization, during the summer vacation between II and III semester
3. The type of industry must be NOT below the Medium Scale category in his / her domain of the degree programme.
4. The student must submit the "Training Completion Certificate" issued by the industry / company / Organization as well as a technical report not exceeding 15 pages, within the stipulated time to be eligible for making a presentation before the committee constituted by the department.
5. The committee will then assess the student based on the report submitted and the presentation made.
6. Marks will be awarded out of maximum 100.
7. Appropriate grades will be assigned as per the regulations.
8. Only if a student gets a minimum of pass grade, appropriate credit will be transferred towards the degree requirements, as per the regulations.
9. It is solely the responsibility of the individual student to fulfill the above conditions to earn the credits.
10. The attendance for this course, for the purpose of awarding attendance grade, will be considered 100%, if the credits are transferred, after satisfying the above (1) to (8) norms; else if the credits are not transferred or transferable, the attendance will be considered as ZERO.
11. The committee must recommend redoing the course, if it collectively concludes, based on the assessment made from the report and presentations submitted by the student, that either the level of training received or the skill and / or knowledge gained is NOT satisfactory.

Assessment for Semester Internship		
	Final Evaluation (100% weightage)	
	Report along with completion certificate from company	Viva-Voce
Semester Internship	50 %	50 %

Course Code	20ECP602L	Course Name	MINOR PROJECT	Course Category	P	Project Work, Internship In Industry / Higher Technical Institutions	L	T	P	C
							0	0	8	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Department of Electronics and Communication	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	Conceptualize a novel idea / technique			
CLR-2 :	Think in terms of social or commercial applications			
CLR-3 :	Understand the management techniques of implementing a project			
CLR-4 :	Prepare a technical report and present in a professional manner			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLO-1 :	Identify and solve simple engineering / biological problems	1	70	65
CLO-2 :	Assess the feasibility of project commercialization	2	80	75
CLO-3 :	Manage the implementation of a project	3	65	60
CLO-4 :	Document a project report	3	75	70

Program Learning Outcomes (PLO)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	H	H	H	H	M	H	H	H	M	H	M	M	M	L	M
CLO-2 :	H	H	H	H	H	H	H	H	H	M	H	M	H	H	H
CLO-3 :	H	M	L	L	M	M	M	M	L	L	L	L	L	M	M
CLO-4 :	H	H	H	H	L	M	H	M	H	M	M	M	H	M	H

1. An in-house project to be taken up by the individual student and complete the minor project before the end of III semester
2. The project can be a development of an experimental kit/ method, an innovative concept or idea or methodology or algorithm / technique, a 3D model, simulation, prototype product, blueprint for a larger project or any other similar developmental work that the respective department approved by the department, are permitted.
3. The student must be attached to a faculty supervisor / mentor
4. A comprehensive report is to be submitted.
5. A presentation is to be made on the work done by the student to committee of reviewers

Learning Assessment weightage	Continuous Learning Assessment (70% weightage)		Final Evaluation (30% weightage)	
	Review I	Review II	Report	Viva-Voce
Minor Project	20 %	50 %	15 %	15 %

Course Code	20ECP603L	Course Name	PROJECT WORK PHASE - I	Course Category	P	Project Work, Internship In Industry / Higher Technical Institutions	L	T	P	C
							0	0	12	6

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1 :	Prepare the student to gain major design and or research experience as applicable to the profession
CLR-2 :	Apply knowledge and skills acquired through earlier course work in the chosen project
CLR-3 :	Make conversant with the codes, standards, application software and equipment
CLR-4 :	Carry out the projects within multiple design constraints
CLR-5 :	Incorporate multidisciplinary components
CLR-6 :	Acquire the skills of comprehensive report writing

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning 1 (Level of Thinking (Bloom))	Learning 2 (Expected Proficiency (%))	Learning 3 (Expected Attainment (%))
CLO-1 :	Design a system / process or gain research insight into a defined problem as would be encountered in engineering practice taking into consideration its impact on global, economic, environmental and social context.	3	85	75

Program Learning Outcomes (PLO)	1 Disciplinary Knowledge	2 Critical Thinking	3 Problem Solving	4 Analytical Reasoning	5 Research Skills	6 Team Work	7 Scientific Reasoning	8 Reflective Thinking	9 Self-Directed Learning	10 Multicultural Competence	11 Ethical Reasoning	12 Community Engagement	13 ICT Skills	14 Leadership Skills	15 Life Long Learning
	H	H	H	M	H	H	M	L	H	L	M	L	H	L	H

- The Major project is a major component of our engineering curriculum: it is the culmination of the program of study enabling the learners to showcase the knowledge and the skills they have acquired, design a product/service of significance, and solve an open-ended problem in engineering.
- The Major Project is to be taken up during the final semester of the program
- The project work (Phase – I) is the preparatory phase for the major project and is to be taken up during the pre-final semester of the program.
- Each student is expected to identify an engineering problem in his / her specialization of study.
- Each student must study in-depth the issues / causes & effects underlying the problem and define the objective of the subsequent work.
- The project shall be driven by realistic constraints like that related to economic, environmental, social, political, ethical, health & safety, manufacturability and sustainability.
- A faculty supervisor / mentor will be assigned to each project.
- Each student team is expected to maintain a log book that would normally be used to serve as a record of the way in which the project progressed during the course of the session.
- Salient points discussed at meetings with the supervisor (i.e., suggestions for further meetings, changes to experimental procedures) should be recorded by the student in order to provide a basis for subsequent work.
- The logbook may be formally assessed;
- A report of the work done during Phase – I must be submitted at the end of the semester, for evaluation.
- Assessment components will be as spelt out in the regulations.
- The department will announce a marking scheme for awarding marks for the different sections of the report.
- The project report must possess substantial technical depth and require the learners to exercise analytical, evaluation and design skills at the appropriate level.

S. No.	Description of project work progress
1.	Review – 1: Major design project identification, the objective, methodology and expected outcome.
2.	Review – 2: Presentation of the proposed work design, implementation and partial result
3.	Review – 3: Presentation of complete project work with results and discussion, Demonstration of project work
4.	Project report/ Thesis submission

Learning Resources	
1.	IEEE Journals, Elsevier Journals, Springer Journals, Any open Access Journal, Reference / user manuals, etc.

Learning Assessment	Continuous Learning Assessment (70% weightage)			Final Evaluation (30% weightage)	
	Review - 1	Review - 2	Review - 3	Project Report	Viva-Voce
Project Work(Phase I)	15 %	25 %	30 %	15 %	15 %

Course Code	20ECP604L	Course Name	PROJECT WORK PHASE - II	Course Category	P	Project Work, Internship In Industry / Higher Technical Institutions	L	T	P	C
							0	0	32	16

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes/Standards**	*Nil*		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	**Learning**		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	*Prepare the student to gain major design and or research experience as applicable to the profession*			
CLR-2 :	*Apply knowledge and skills acquired through earlier course work in the chosen project*			
CLR-3 :	*Make conversant with the codes, standards, application software and equipment*			
CLR-4 :	*Carry out the projects within multiple design constraints*			
CLR-5 :	*Incorporate multidisciplinary components*			
CLR-6 :	*Acquire the skills of comprehensive report writing*			
Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*			
CLO-1 :	*Design a system / process or gain research insight into a defined problem as would be encountered in engineering practice taking into consideration its impact on global, economic, environmental and social context.*	*3*	*85*	*75*

Program Learning Outcomes (PLO)														
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
H	*H*	*H*	*M*	*H*	*H*	*M*	*L*	*H*	*L*	*M*	*L*	*H*	*L*	*H*

- The Major project (Phase-II) is a major component of our engineering curriculum: it is the culmination of the program of study enabling the learners to showcase the knowledge and the skills they have acquired, design a product/service of significance, and solve an open-ended problem in engineering.
- The Major Project is to be taken up during the final semester of the program, and it can be an extension of the Project Work (Phase-I)
- Each student is expected to identify an engineering problem in his / her specialization of study.
- Each student must study in-depth the issues / causes & effects underlying the problem and define the objective of the subsequent work.
- The project shall be driven by realistic constraints like that related to economic, environmental, social, political, ethical, health & safety, manufacturability and sustainability.
- A faculty supervisor / mentor will be assigned to each project.
- Each student team is expected to maintain a log book that would normally be used to serve as a record of the way in which the project progressed during the course of the session.
- Salient points discussed at meetings with the supervisor (i.e., suggestions for further meetings, changes to experimental procedures) should be recorded by the student in order to provide a basis for subsequent work.
- The logbook may be formally assessed;
- A report of the work done during Phase – II must be submitted at the end of the semester, for evaluation.
- Assessment components will be as spelt out in the regulations.
- The department will announce a marking scheme for awarding marks for the different sections of the report.
- The project report must possess substantial technical depth and require the learners to exercise analytical, evaluation and design skills at the appropriate level.

S. No.	Description of project work progress
1.	Review – 1: Major design project identification, the objective, methodology and expected outcome.
2.	Review – 2: Presentation of the proposed work design, implementation and partial result
3.	Review – 3: Presentation of complete project work with results and discussion, Demonstration of project work
4.	Project report/ Thesis submission

Learning Resources	
1.	IEEE Journals, Elsevier Journals, Springer Journals, Any open Access Journal, Reference / user manuals, etc.

Learning Assessment					
	Continuous Learning Assessment (70% weightage)			Final Evaluation (30% weightage)	
	Review - 1	Review - 2	Review - 3	Project Report	Viva-Voce
Project Work (Phase-II)	15 %	25 %	30 %	15 %	15 %

Course Code	20MAO501T	Course Name	OPERATIONS RESEARCH	Course Category	O	Open Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Mathematics	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
CLR-1 :	To provide the knowledge about linear programming problems and simplex method.	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-2 :	To understand and apply the transportation model and assignment models in engineering applications.			
CLR-3 :	To provide the knowledge about networking, scheduling and crashing of networks.			
CLR-4 :	To understand and apply the inventory models and game theory in industrial and engineering problems.			
CLR-5 :	To gain the knowledge about the Markovian model and different kind of Queueing models.			
CLR-6 :	To apply the optimization techniques and Queueing Theory in the industrial and Engineering applications.			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Students will be able to solve the problems of LPP by simplex and graphical method.	1	85	80	L		L						M						M
CLO-2 :	Students will be able to solve transportation and assignment problems.	1	85	80	L		L	M	L		M	M							H
CLO-3 :	Students will be able to solve the networking and scheduling problems.	2	85	80	L	L	M					L	M						L
CLO-4 :	Students will be able to apply the inventory and game theory techniques in the engineering problems.	2	85	80	L	M	M	M	L		M	L	M						H
CLO-5 :	Students will be able to formulate concrete problems using Queueing theoretical approaches.	3	85	80	L	M	L		M			L	M						M
CLO-6:	Students will be able to apply optimization techniques in industrial and engineering problems.	2	85	80	L		L		L		L		L						M

Duration (hour)		Module 1/ Linear Programming Problem	Module 2/ Transportation and Assignment Problems	Module 3/ Networks and Scheduling	Module 4/ Inventory models and Graph theory	Module 5/ Queueing Theory
		9	9	9	9	9
S-1	SLO-1	Introduction to Operations Research	Transportation model	Network models	Introduction to Inventory models	Introduction to Queueing models
	SLO-2	Applications	Applications	Applications	Applications	Characteristics
S-2	SLO-1	Linear Programming-Mathematical Formulation	Northwest Corner method	Construction of Networks	Various Costs and Concepts	Poisson arrivals and Exponential service times
	SLO-2	Simple Examples	Simple Examples	Simple Problems	Simple examples	Symbolic representation
S-3	SLO-1	Graphical Method	Vogel's Approximation method	Shortest Route problem	EOQ Deterministic inventory models	Single server model with infinite system capacity
	SLO-2	Simple Examples	Simple Examples	Examples	Applications	Characteristics of the model(M/M/1):(∞/FIFO)
S-4	SLO-1	Simplex Method	MODI method	Maximal Flow model	Problems on EOQ models	Relation between waiting time in the queue and in the system
	SLO-2	Examples	Simple Examples	Examples	Problems on EOQ models	Selected Problems
S-5	SLO-1	Big M Method	Stepping stone method	CPM Network	Dynamic EOQ models	Multiple server model with infinite system capacity
	SLO-2	Examples	Simple Examples	Problems of CPM	Applications	Characteristics of the model (M/M/s):(∞/FIFO)

S-6	SLO-1	Two phase Simplex method	Assignment problems	PERT Network	No set up EOQ model	Selected Problems
	SLO-2	Examples	Examples and problems	Problems of PERT	Problems	Selected Problems
S-7	SLO-1	Duality	The Hungarian method	Problems on CPM & PERT to Engineering	Set up EOQ model	(M/M/s):(∞/FIFO) -applications
	SLO-2	Examples	Examples and problems	Problems on CPM & PERT to Engineering	Problems	More Problems
S-8	SLO-1	Dual Simplex method	Travelling salesman problem	Scheduling of Network	Elementary Game Theory	Non-Markovian model
	SLO-2	Examples	Methodology	Problems	Game theory applications	M/G/1 Queueing system characteristics
S-9	SLO-1	Sensitivity analysis	Applications	Crashing of Network	Game Theory Simulation	Pollaczek Khinchine Formula
	SLO-2	Application of Simplex method	Applications to Engineering problems	Problems	Problems	Applications

Learning Resources	1. H.A. Taha, Operations Research, An Introduction, 10th Edition, Pearson, 2017 2. J.C. Pant, Introduction to Optimization: Operations Research, 7th reprinted edition, Jain Brothers, Delhi, 2015 3. Frederick S. Hillier, Gerald J. Lieberman, Bodhibrata Nag, Preetam Basu, Introduction to Operations Research, McGraw Hill Pub., 2017	4. R. Panneerselvam, Operations Research, 2nd Edition, Prentice Hall of India 2012 5. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) (60% weightage)						Final Examination(40% weightage)	
		CLA-1(20%)		CLA-2(25%)		CLA-3# (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30	-	30	-	30	-	30	-
	Understand								
Level 2	Apply	40	-	40	-	40	-	40	-
	Analyze								
Level 3	Evaluate	30	-	30	-	30	-	30	-
	Create								
	Total	100 %		100 %		100 %		100 %	

CLA – 3 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers:		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
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		3. Dr. D. Prakash, SRMIST

Course Code	20GNP620T	Course Name	MASSIVE OPEN OLINE COURSES	Course Category	O	OPEN ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1 :	Provide opportunity to study with the top universities through online platform in his / her areas of interest beyond the curriculum
CLR-2 :	Provide full credit transfer, as per university regulations

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Disciplinary Knowledge	Critical Thinking	Problem Solving	Analytical Reasoning	Research Skills	Team Work	Scientific Reasoning	Reflective Thinking	Self-Directed Learning	Multicultural Competence	Ethical Reasoning	Community Engagement	ICT Skills	Leadership Skills	Life Long Learning
CLO-1 :	Acquire additional knowledge in his / her areas of interest	1	70	65	H	H	H	H	M	H	H	H	M	H	M	M	M	L	M
CLO-2 :	Take advantage of the flexibility in learning	2	80	75	H	H	H	H	H	H	H	H	H	M	H	M	H	H	H

Registration process, Assessment and Credit Transfer

1. Students can register for courses offered by approved global MOOCs platforms like Swayam, NPTEL, edX, Coursera or Universities with which SRM partners specifically for MOOCs.
2. Annually, each department must officially announce, to the students as well as to the Controller of Examinations, the list of courses that will be recognized and accepted for credit transfer.
3. The student has to choose online courses listed by the department and should undergo for the minimum period of 8-12 weeks.
4. The department must also officially announce / appoint one or more faculty coordinator(s) for advising the students attached to them, monitoring their progress and assist the department in proctoring the tests, uploading the marks / grades, and collecting and submitting the graded certificate(s) to the CoE, within the stipulated timeframe.
5. Student who desires to pursue a course, from the above department-approved list, through MOOCs must register for that course during the course registration process of the Faculty of Engineering and Technology, SRM University.
6. The maximum credit limits for course registration at SRM will include the MOOCs course registered.
7. The student must periodically submit the marks / grades obtained in various quizzes, assignments, tests etc immediately to the Faculty Advisor or the Course Coordinator for uploading in the university's academic module.
8. The student must take the final test as a Proctored / Supervised test through a secure, physical testing center.
9. The student must submit the "Certificate of Completion" as well as the final overall Marks and / or Grade within the stipulated time for effecting the grade conversion and credit transfer, as per the regulations. It is solely the responsibility of the individual student to fulfil the above conditions to earn the credits.
10. The attendance for this course, for the purpose of awarding attendance grade, will be considered 100%, if the credits are transferred, after satisfying the above (1) to (7) norms; else if the credits are not transferred or transferable, the attendance will be considered as ZERO.

Learning Resources

1. https://swayam.gov.in/
2. www.cousera.org
3. www.edx.org
4. www.it.iitb.ac.in
5. Any other online courses offered by reputed entity