A PROJECT REPORT

on

MISSILE LAUNCHER SYSTEM CONTROL UNIT

Submitted in partial fulfilment for the award of the degree

of

BACHELOR OF TECHNOLOGY

in

ELECTRICAL & ELECTRONICS

by

ANUPAM GOPE (Reg. No.: RA1511005010221)

Under the guidance of

Dr. K. VIJAYAKUMAR, M.E., Ph.D

Professor & Head, EEE

SRM
INSTITUTE OF SCIENCE & TECHNOLOGY
(Deemed to be University u/s 3 of UGC Act, 1956)

FACULTY OF ENGINEERING AND TECHNOLOGY

SRM Nagar, Kattankulathur- 603 203

Kancheepuram Dist

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BONAFIDE CERTIFICATE

Certified that this project report titled "**MISSILE LAUNCHER SYSTEM CONTROL UNIT**" is the bonafide work of **ANUPAM GOPE** (Reg. No.: **RA1511005010221**) who carried out the project work under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project report or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

Signature of the Guide

Dr. K.VIJAYAKUMAR, M.E., Ph.D

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Signature of the HOD

Dr. K.VIJAYAKUMAR, M.E., Ph.D

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Internal Examiner

External Examiner

Date:

TATA

19th Mar' 2019

TRAINING COMPLETION CERTIFICATE

This is to certify that **Mr. Anupam Gope** studying B.E. in Electronics & Electrical Engineering, in **SRM Institute of Science & Technology** has successfully completed his Project at **Tata Power - SED** from **03-Jan-2019** to **19-Mar-2019** under guidance of **Mr. A K Swamy**.

He had worked on a project - **"MISSILE LAUNCHER SYSTEM CONTROL UNIT".**

During his stay with us, he was found to be sincere and hardworking.

We wish him all the best for his future endeavors.

For Tata Power – SED

Prema N
Manager - HR

TATA POWER SED

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I owe my deep sense of gratitude to my **Project Coordinator, Dr. A. RATHINAM,** Professor having extended their fullest support in completing the project work.

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Last but not the least; I would like to thank my **Parents and Friends** for the supports, concerns and prayers, which were a major factor in the completion of this project.

As everything begins and ends with God, I conclude this acknowledgement by thanking God for everything.

(ANUPAM GOPE)

ABSTRACT

In the modern day scenario, national security is of utmost importance and the best way to achieve this is by advancing in the field of defence technology. Use of modern weapon systems has revolutionised the concept of warfare. Technology as a force multiplier provides a competitive and cutting edge. The technology of missile systems encompasses the multiple streams of engineering, technology and applied sciences. A number of factors are responsible for the successful launch of missiles. Missile control systems typically employ a missile interface unit capable of relaying guidance information to the missile and monitoring the operation of the missile and its launcher prior to launch. The missile interface unit provides target position information and control signals for test and launch of the missile, and power for activating it as well as determining the status of the missile. It employs a plurality of cards, each card having a specific function and being interconnected by a backplane bus system which also couples the cards to other components of the launcher control system. A system control unit is developed which controls various cards that have specific functions and work together for the system to work efficiently. The new system that has been developed under the guidance of experienced personnel in R&D labs of Tata Power SED and has proven to be more cost effective and have a better control capability. The ruggedness of the system has been tested under various environmental conditions as given under JS 55555 guidelines for environmental testing. It has also proven to be successful when subjected to tests of electromagnetic interference according to the international American military

standard MIL-STD-461-E. Complying with conductivity and susceptibility tests, the control unit has cleared all the testing procedures for electromagnetic compatibility and is ready to be deployed for warfare where electronic compatibility is of utmost importance. A launcher control system must be flexible and efficient to accomplish its mission. While prior missile interface units relied on hardware components which were less efficient and limited in the number of tasks they could perform, a modern approach will ensure high operational mobility, flexibility and accuracy which give the missile launcher system an edge in modern artillery warfare.

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COMPANY PROFILE

1.1 GENERAL

For close to four decades, The Tata Power Company Limited through its Strategic Engineering Division (Tata Power SED) has been a leading private-sector player in the indigenous Design, Development, Production, Integration, Supply and Life-cycle Support of mission-critical Defence Systems of Strategic importance. During this period, the Division has partnered the Ministry of Defence (MoD), the Armed Forces, DPSUs and DRDO in the development & supply of state-of-the-art Systems and emerged as a Prime Contractor to MoD for Indigenous Defence Production when it secured Orders for Pinaka Multi Barrel Rocket Launcher, Akash Army Launcher and Integrated EW System for the Indian Army and for the Akash Air Force Launcher, COTS-based Automatic Data Handling System for Air Defence and Modernisation of Airfield Infrastructure (MAFI) for the Indian Air Force.

Tata Power SED has the unique distinction of participating in Defence Programs through a dedicated R&D Centre at Mumbai and a Production facility along with an R&D Facility at Bengaluru. As a leading domestic player in Strategic Engineering, the Division is now globally recognised for harnessing its "Systems and Engineering" capabilities and has been appraised at Maturity Level 5 of CMMI for Development v1.3.

Success in modern war depends on Integrated operations over distributed geographies using Sensors and Weapons of varying vintage. Tata Power SED's team has the right blend of technological and operational experience in integrating these heterogeneous systems, using both industry standard and system specific interfaces and protocols.

In recognition of its pioneering capabilities in Design, Development, Manufacturing and System Integration, Tata Power SED was nominated by MoD

as a Major Work Centre for the Samyukta Electronic Warfare Program under the aegis of DRDO. Tata Power SED has also received several national awards from industry associations such as the Federation of the Indian Chamber of Commerce and Industry (FICCI), the Confederation of Indian Industry (CII) and the Ministry of Science and Technology.

CHAPTER 2

INTRODUCTION

2.1 GENERAL

Use of modern weapon systems has revolutionised the concept of warfare. Technology as a force multiplier provides a competitive and cutting edge. The technology of missile systems encompasses the multiple streams of engineering, technology and applied sciences. A number of factors are responsible for the successful launch of missiles.

Missile control systems typically employ a missile interface unit capable of relaying guidance information to the missile and monitoring the operation of the missile and its launcher prior to launch. The missile interface unit provides target position information and control signals for test and launch of the missile, and power for activating it as well as determining the status of the missile. It employs a plurality of cards, each card having a specific function and being interconnected by a backplane bus system which also couples the cards to other components of the launcher control system. A system control unit is developed which controls various cards that have specific functions and work together for the system to work efficiently.

The new system that has been developed under the guidance of experienced personnel in R&D labs of Tata Power SED and has proven to be more cost effective and have a better control capability. The ruggedness of the system has been tested under various environmental conditions as given under JS 55555 guidelines for environmental testing. It has also proven to be successful when subjected to tests of electromagnetic interference according to the international American military standard MIL-STD-461-E. Complying with conductivity and susceptibility tests, the control unit has cleared all the testing procedures for electromagnetic compatibility and is ready to be deployed for warfare where electronic compatibility is of utmost importance.

A launcher control system must be flexible and efficient to accomplish its mission. While prior missile interface units relied on hardware components which were less efficient and limited in the number of tasks they could perform, a modern approach will ensure high operational mobility, flexibility and accuracy which give the missile launcher system an edge in modern artillery warfare.

. **2.2 OBJECTIVES**

    (a) To explain the design of a system controller module for missile launcher.

    (b) Conduct CE & RE tests to check the EMC compliance of the module.

CHAPTER 3

SYSTEM CONTROLLER MODULE

3.1 GENERAL

The System controller module is based on VITA-46 (VPX) specifications with 3U form factor defined by the standards body VITA. The SC consists of a rugged conduction-cooled chassis comprising of the following modules:

1) CPU module (VPX SBC)
2) Discrete Input Board (72 channels)
3) Discrete Output Board (32 channels)
4) Isolated Analog Input Board (32 channels)
5) Isolated Analog Output Board (8 channels)
6) SATA & COMM board(32 GB SATA flash)
7) SSI Encoder(12 channels)
8) Octal-based RS422 (16 Channels)
9) Power Supply Board
10) EMI/Filter Module
11) SC I/O panel(USB and display port)

These modules are Open VPX based 3U conduction cooled modules with insertion/ extraction feature. The SC consists of 10-slot flex-rigid backplane which complies with open VPX based 3U backplane.

3.2 SPECIFICATIONS

Table 3.1 Electrical Specifications of SC Module

Processor	COMe-mBT10, CPU:Intel Atom E3845 series embedded or equivalent
Input supply	24-28V DC
No of slots	10 slots Slot 1: Power card 1 Slot 2: Power card 2(spare for future) Slot 3: SBC – single board computer Slot 4: SATA & COMM card Slot 5: RS422 card 1 Slot 6: RS422 card 2 Slot 7: DIO card 1 Slot 8: DIO card2 Slot 9: SSI card Slot 10: Analog card
Memory	32 GB Onboard SATA Flash 32GB CFast SSD 16GB eMMC Flash
I/O resources	Gigabit Ethernet: Two ports on the communication connector, and one port on the RJ45 connector RS-422: 16 serial channels 72 Digital inputs 32 Digital outputs 32 Analog input channels with 16-bit resolution and ±10 V range each 8 Analog output channels USB: 4 ports 1 DVI-D

Table 3.2 Mechanical Specifications of SC Module

Card Area	Conduction cooled cards and sealed enclosure
Thermal Management	Conduction cooled
Back Plane	VPX –VITA46 (Military Rugged)
Connectors	Front End Series-III MIL-38999 Connectors
Chassis Dimensions	3U form factor
Operating Temperature	-20°C to +55°C
Storage Temperature	-30°C to +70°C
Colour	Aluminium/Matte Black
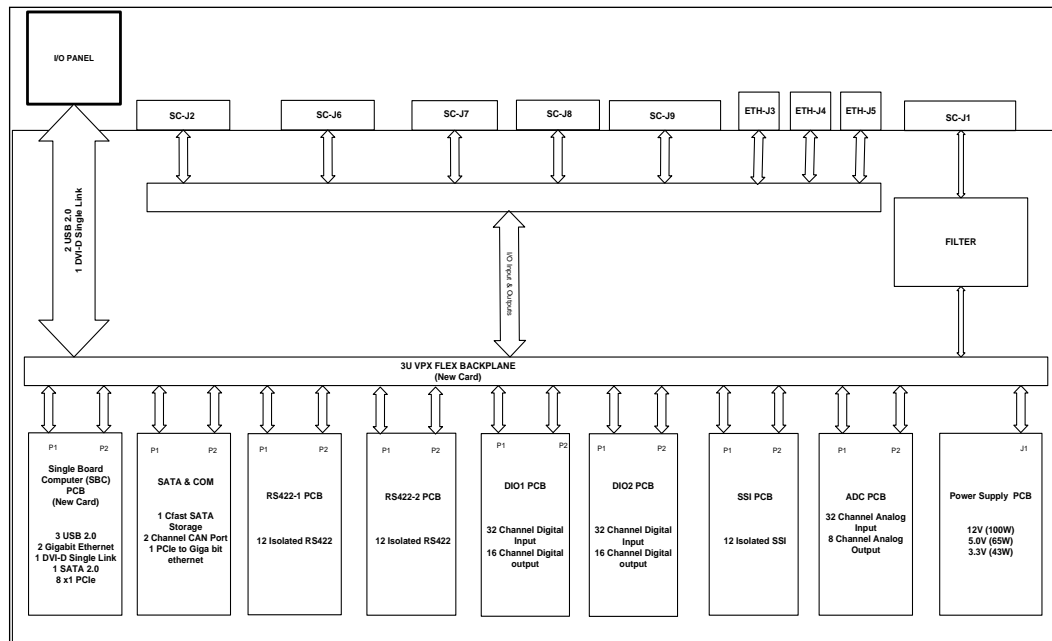
Figure 3.1 Functional block diagram of SC Module

3.3 MODULE/CARD DETAILS

3.3.1 VPX BASED SBC Module (CPU CARD)

The SC SBC card is a conduction-cooled 3U VPX card based on COMe-mBT10, CPU: Intel Atom E3845 series embedded or equivalent processor and operates at 12V power. The 3U based SBC card complies with VPX VITA 46 specification. The SBC communicates with other interfaces through the PCIe interface. The SBC is having 32GB onboard flash is used to store source code and application code. 2 PCIe x1 lane interface from the processor is converted into eight single lane PCIe interfaces using 2 PCIe bridges. These eight single lanes are utilized for DIO (2), ADC, RS422 (2), SATA & COMM, SSI interfaces. Two 1Gbps Ethernet interfaces are designed using one PCIe to Ethernet (I210) converter and using MDI lines from the processor. 2 USB ports are provided for user application and 1 DVI-D display port is provided for user application.
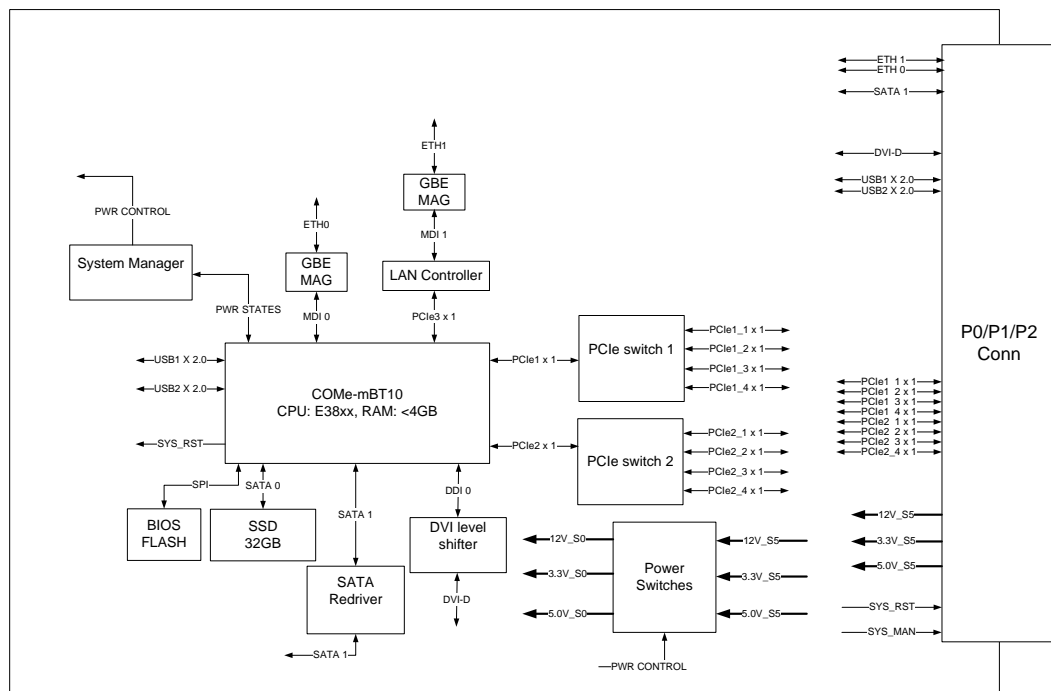

Figure 3.3 Functional block diagram of SBC Module (CPU Card)

Table 3.3 Functional Specifications of SBC Module (CPU Card)

Processor	BayTrail-I IntelR Atom E3845
Memory	16 GB Onboard SATA Flash 16 GB eMMC Flash
Display Port	1 x DVI-D
Ethernet	2 Ethernet ports
SATA	1 x SATA 2.0 External to VPX 1 x For internal SATA FLASH
USB	2 x USB 2.0 External
Battery	1 x RTC battery

Table 3.4 Electrical Specifications of SBC Module (CPU Card)

Power Input	12.0V,3.3V, 5.0V
Voltages generated onboard	2.5V, 1.2V, 1.0V

Table 3.5 Environmental Specifications of SBC Module (CPU Card)

Operating Temperature:	-20°C to +55°C
Relative Humidity:	>95% RH (Non-condensing)

3.3.2 DISCRETE INPUT/OUTPUT BOARD (36 CHANNEL DIP & 8 CHANNEL DOP)

The SC 3U VPX DIO PCB ASSEMBLY is designed as per VITA 46 standard. The key functionality of this board is receiving 36 Isolated Discrete inputs, processing and providing to FPGA using GPIO pins. The FPGA has an internal logic to provide the data to SBC card using the PCIe interface. The other

key functionality of this board is providing 16 discrete outputs using Relay drivers.

36 Isolated digital inputs are achieved through TCMT4100 optical isolator. Each TCMT device can support up to 4 inputs.

There are 16 isolated digital outputs made available through ASSR-1410 device which is driven by GPIO pins of the FPGA. Each output of ASSR-1410 can drive 600mA current. A latch logic is provided for the output to avoid any toggling on output line during FPGA configuration and power up.

There FPGA function as a PCIe based controller with digital input and output connections. During power up the configuration flash loads logic cell configuration to FPGA through a serial link synchronous with a clock generated from configuration flash. Once the FPGA is configured it take control from configuration flash and start function as a hardware ASIC. The fully configured FPGA will function as PCIe based discrete digital input and output device.
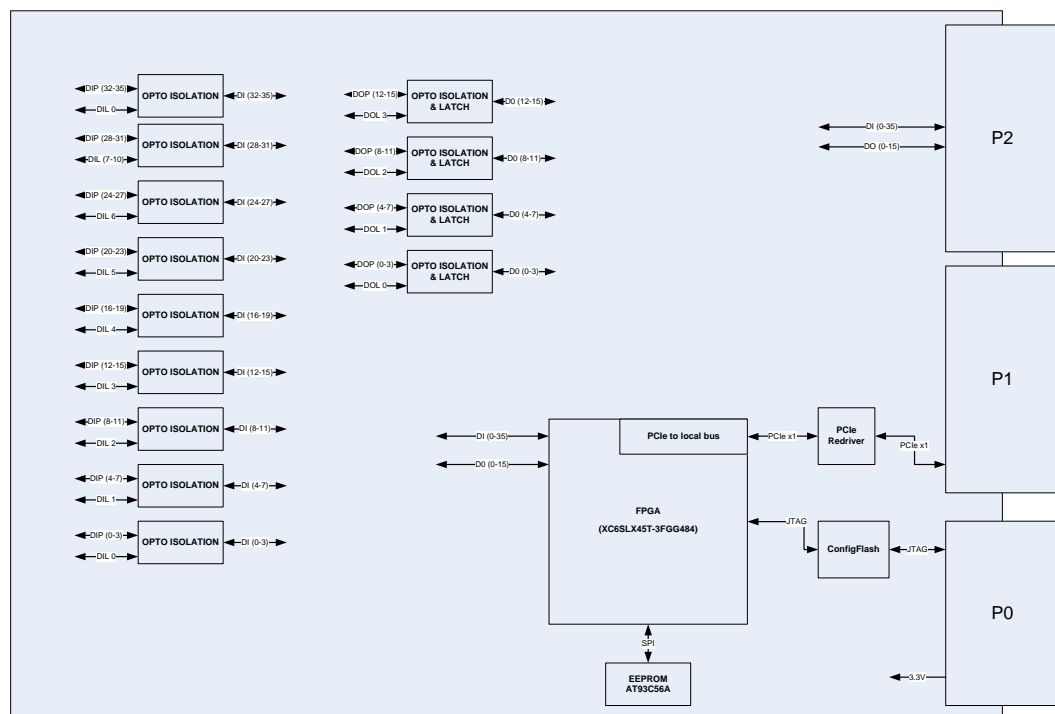

Figure 3.3 Functional block diagram of DIP Board

The PCB will get 3.3V and 5.0V power from P0 connector as per the VPX standard. From the 5.0V core voltages required for FPGA will be converted using LTM4622, TPS77518D, DC-DC converter and LDO. The LTM4622 is capable of driving 2.5A current on two output channel of this device. There is an LDO provided on the PCB for 1.8V required for configuration flash for FPGA.

Table 3.6 Functional Specifications of DIP Board

FPGA	1 X Spartan6 FPGA with 32Mb of Platform Flash
PCIe Interface	1 x PCIe 2.0 lane 1 interfaced between FPGA and SBC Board
Power Input	+5V,+3.3V input from Backplane and the other required voltages like +1.8V, +1.2V are generated on this board using Switching/Linear Regulators/Isolated DC-DC Converters
PCB Dimensions	100mm X 160mm X 1.6mm
Terminations	VPX Connectors as per VITA46.0 Standard
Operating Temperature	-20°C to +55°C

3.3.3 ISOLATED ANALOG INPUT & OUTPUT BOARD (32 AI CHANNELS, 8 AO CHANNELS)

P0, P1 and P2 are the VPX connectors, P0 Connector is provided with the board power requirement of 3.3V, 5V and 12V power from the backplane and P1 Connector are used to connect the PCIe lane from SBC through the backplane. P2 is used to connect 32 Channel of Analog inputs and 8 Channels of Analog outputs connection to and from the backplane.

The AD76061/AD7606-6/AD7606-4 is 16-bit, simultaneous sampling, analog-to-digital data acquisition systems (DAS) with eight, six, and four channels, respectively. Each part contains analog input clamp protection, a second-order antialiasing filter, a track-and-hold amplifier, a 16-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces

The AD5360/AD5361 contains sixteen, 16-/14-bit DACs in a single 52-lead LQFP or 56-lead LFCSP package. They provide buffered voltage outputs with a span four times the reference voltage. The gain and offset of each DAC can be independently trimmed to remove errors. For even greater flexibility, the device is divided into two groups of eight DACs, and the output range of each group can be independently adjusted by an offset DAC. The Outputs of DAC is Buffered using OP-AMP voltage follower Circuit.

The SC VPX BASED ADC PCB ASSEMBLY comprises of one Spartan6 FPGA with one PCIe interface and four SPI Master Interfaces. A total of 32 analog inputs are interfaced to four ADCs with each ADC interfaced to 8 analog input channels and 8 analog outputs to DAC. The output of ADC which is SPI interface is isolated using SPI-isolator and then isolated SPI signals are provided to FPGA. Now the FPGA reads the data from four SPI interfaces and transmits the data to SBC board using PCIe interface.

12V, 5V and 3.3V are input supplies from external Power Supply card through VPX connector P0 (Power). The 5V and 3.3V Supplies Used for Internal Circuits and there are two 1.2V internal generated supply voltages from 5V, 5V and 3.3V Isolated Supply generated from 5V, 1.8V is generated from 5V, Isolated +15V and -15V generated from 12V, and 3.3V isolated supply generated from +15V. These are the internally generated supplies.

Table 3.7 Functional Specifications of Isolated Analog I/O Board

FPGA	1 X Spartan6 FPGA with 32Mb of Platform Flash
ADC,DAC	4 X 8-Channel,16Bit ADC @ 200ksps with SPI interface, 16-/14-bit,16- channel DACs(using only 8)
SPI-isolator	4 X SPI-isolators
PCIe Interface	1 x PCIe 2.0 lane 1 interfaced between FPGA and SBC Board
Power Input	12V,3.3V,5V input from Backplane and the other required voltages like 1.8V, 1.2V are generated on this board using Switching/Linear Regulators
Power supply Isolated μModule	+15V,-15V, +5V, +3.3V isolated voltages are generated using Linear Technologies μModule for each ADC
PCB Dimensions	100mm X160mm X 1.6mm
Cooling	Conduction cooled
Operating Temperature	-20°C to +55°C

3.3.4 OCTAL BASED RS422 CARD

The Octal RS422 card is a serial communication board having provisions for 8 channel isolated RS422 transceivers based on EXAR (XR17V358IB176-F) PCIe to 8 Port UART Converter, RS422 Level Translator is used to convert the UART TTL output to RS442 Level, the PCB outline and placement of the connectors are as per the VITA 46.0 specifications.

The Octal RS422 card will be interfaced to the SBC over PCIe interface board supports 8 channels of UART RS422 serial communication lines, EXAR (XR17V358IB176-F) PCIe to 8 Port UART Converter is used to convert PCIe to 8 Channels of TTL level UART communication lines. The TTL level UART ports further level translated to RS422 Level using (LTM2881IV-5#PBF) Isolated RS422 Level Translator with internal isolated 5V power generation. The

data or command from the SBC through backplane with PCIe interface sends the required communication data to selected UART channels. The received serial UART communication data will be sent back to SBC through PCIe.

P0, P1 and P2 are the VPX connectors, P0 Connector is provided with the board power requirement of 3.3V and 5V from the backplane and P1 Connector is used to connect the PCIe lane from SBC through the backplane. P2 is used to connect 8 Channels RS442 Serial communication Lines connection to and from the backplane.

5V and 3.3V are input supplies from external Power Supply card through VPX connector P0 (Power), No internal Regulators Used.
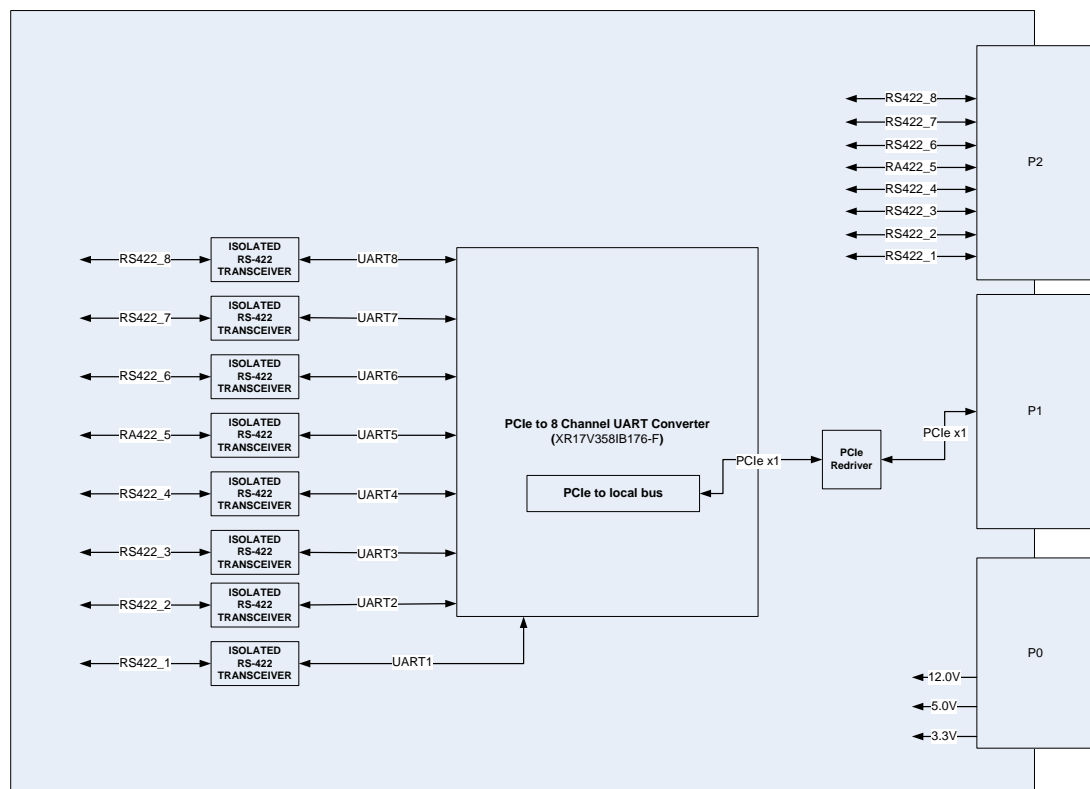

Figure 3.4 Functional block diagram of Octal Based RS422 Card

Table 3.8 Functional Specifications of Octal Based RS422 Card

PCIe to UART	8 channels
PCIe Interface	1 x PCIe 2.0 lane 1 interfaced for converting to UART channels
Power Input	3.3V,5V input from Backplane
PCB Dimensions	100mm X160mm X 1.6mm
Cooling	Conduction cooled
Operating Temperature	-20°C to +55°C
PCIe to UART	8 channels
PCIe Interface	1 x PCIe 2.0 lane 1 interfaced for converting to UART channels
Power Input	3.3V,5V input from Backplane

3.3.5 SSI ENCODER CARD

P0, P1 and P2 are the VPX connectors, P0 Connector is provided with the board power requirement of 3.3V and 5V from the backplane and P1 Connector is used to connect the PCIe lane from SBC through the backplane. P2 is used to connect 12 encoder Channels.

The PCB will get 3.3V and 5.0V power from P0 connector as per the VPX standard. From the 5.0V core voltages required for FPGA will be converted using LTM4622, TPS77518D, DC-DC convertor and LDO. The LTM4622 is capable of driving 2.5A current on two output channel of this device. There is an LDO provided on the PCB for 1.8V required for configuration flash for FPGA.

The 3U VPX based SSI PCB Assembly comprises of one spartan6 FPGA with one PCIe interface, from FPGA through GPIO lines providing to the SSI level translated using (LTM2881IV-5#PBF) Isolated SSI Level Translator with internal isolated 5V power generation. The data or command from the SBC through backplane with PCIe interface sends the required communication data to

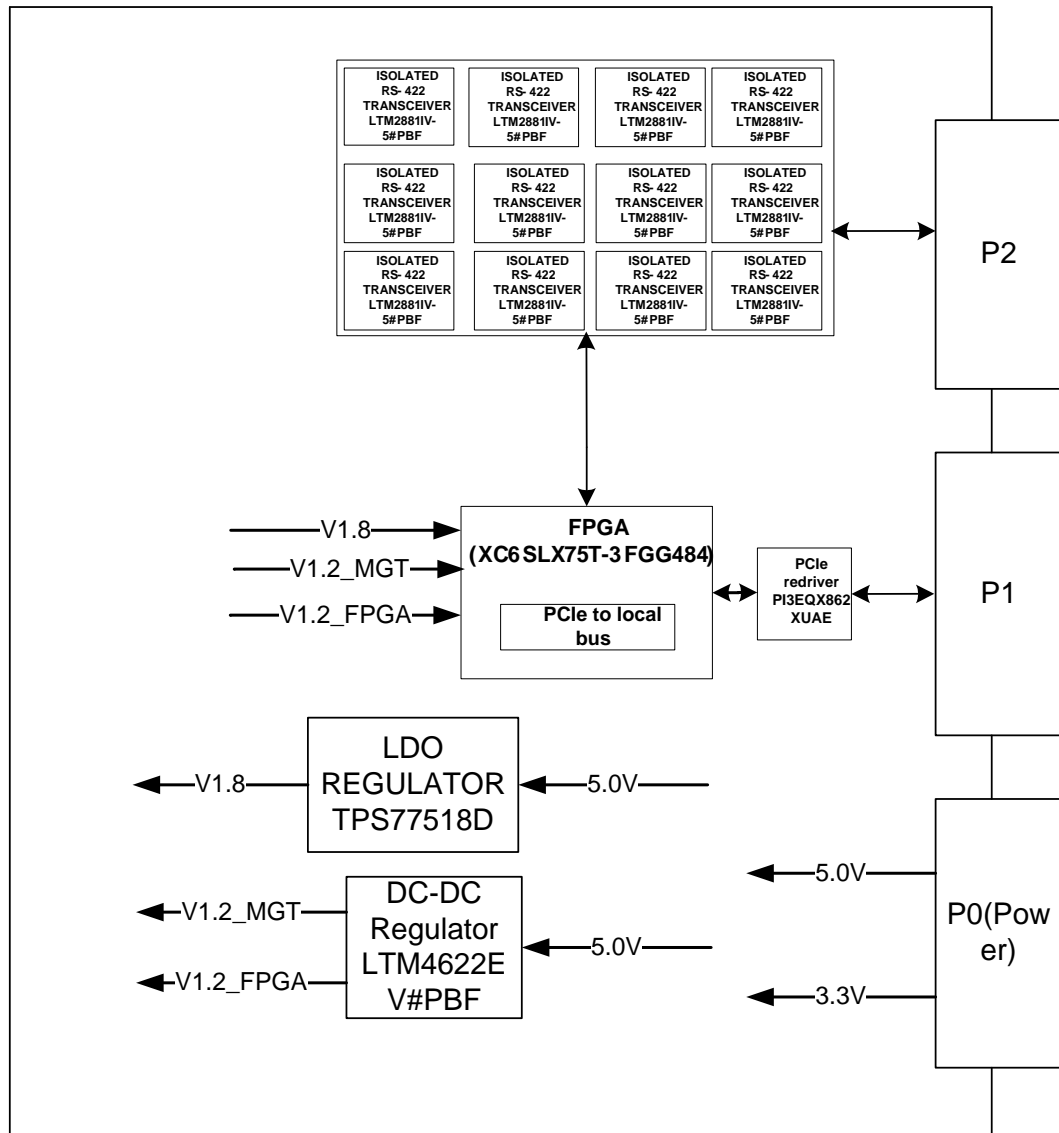selected SSI channels. The received encoders communication data will be sent back to SBC through PCIe.

Figure 3.5 Functional block diagram of SSI Encoder Card

Table 3.9 Functional Specifications of SSI Encoder Card

FPGA	1 X Spartan6 FPGA with 32Mb of Platform Flash
ADC,DAC	4 X 8-Channel,16Bit ADC @ 200ksps with SPI interface, 16-/14-bit,16- channel DACs(using only 8)
SPI-isolator	4 X SPI-isolators
PCIe Interface	1 x PCIe 2.0 lane 1 interfaced between FPGA and SBC Board
Power Input	12V,3.3V,5V input from Backplane and the other required voltages like 1.8V, 1.2V are generated on this board using Switching/Linear Regulators
Power supply Isolated µModule	+15V,-15V, +5V, +3.3V isolated voltages are generated using Linear Technologies µModule for each ADC
PCB Dimensions	100mm X160mm X 1.6mm
Cooling	Conduction cooled
Operating Temperature	-20°C to +55°C

3.3.6 SATA & COM CARD

P0, P1 and P2 are the VPX connectors, P0 Connector is provided with the board power requirement of 3.3V and 5V from the backplane and P1 Connector is used to connect the PCIe lanes and SATA lane from SBC through the backplane. P2 is used to connect one channel Gigabit Ethernet lines and 2 Channels of CAN Serial communication Lines connection to and from the backplane.

The SATA AND COM card will be interfaced to the SBC over PCIe and SATA interface. The Board supports 32 GB of SATA CFAST Memory, one Gigabit Ethernet interface and 2 channels of CAN Serial communication lines (for future purposes).

The SATA & COM card has the provision of 32 GB of SATA CFAST Memory with Write protect option, the SATA lines are interfaced to SBC card through SATA Redriver. 1 channel of PCIe to Gigabit Ethernet Converter (I210) with Isolation Transformer and 2 channels CAN interface with isolated CAN transceiver which is converted from PCIe to parallel data using FPGA and SJA1000 is used as Parallel to CAN Converter.

One Gigabit Ethernet interface shall be provided on this card. This is interfaced using PCIe. I210 controller shall be used for PCIe to Gigabit Ethernet conversion. The Ethernet line shall be connected to Ethernet magnetic and the output magnetic lines are given to connector.

12V, 5V and 3.3V are input supplies from external Power Supply card through VPX connector P0 (Power). The 5V and 3.3V Supplies Used for Internal Circuits and there are two 1.2V internal generated supply voltages from 5V and 1.8V is also generated from 5V.
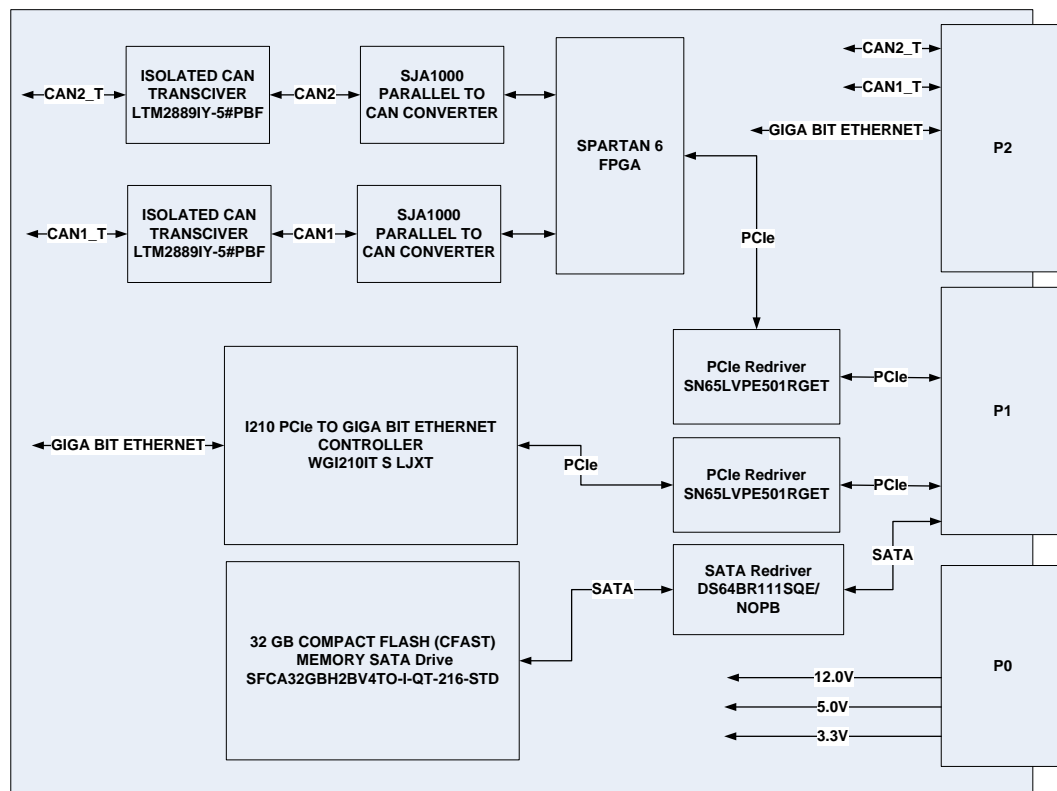

Figure 3.6 Functional block diagram of SATA & COM Card

Table 3.10 Functional Specifications of SATA & COM Card

FPGA	1 X Spartan6 FPGA with 32Mb of Platform Flash
PCIe Interface	2 x PCIe 2.0 lane 1 interfaced between FPGA and SBC Board and 1 for gigabit ethernet
CFast Storage	32 GB
Ethernet	1 ethernet port using I210 PCIe to Gigabit Ethernet
Power Input	+12V,+5V,+3.3V input from Backplane and the other required voltages like +1.8V, +1.2V are generated on this board using Switching/Linear Regulators/Isolated DC-DC Converters
PCB Dimensions	100mm X 160mm X 1.6mm
Terminations	VPX Connectors as per VITA46.0 Standard
Operating Temperature	-20°C to +55°C

3.3.7 POWER SUPPLY BOARD

The input to this PCB comes from a filter card, the variable DC voltage (18-36V) is connected to the power card through Euro Connector.

The Euro connector provides the main 28-36VDC power supply, which is routed to a dc-dc converter (V28C12T100B2). The DC-DC converter comprises constant DC 12V from (V28C12T100B2).

And one more DC-DC converter (LTM4628) is used to generate 3.3V and 5V from 12V.

Outputs of both these dc-dc converters would be routed from this power card to the Flex backplane and hence would be routed to all the card slots for the internal usage of the module.

The PCB outline and placement of the connectors would be as per the VITA 46 specifications.
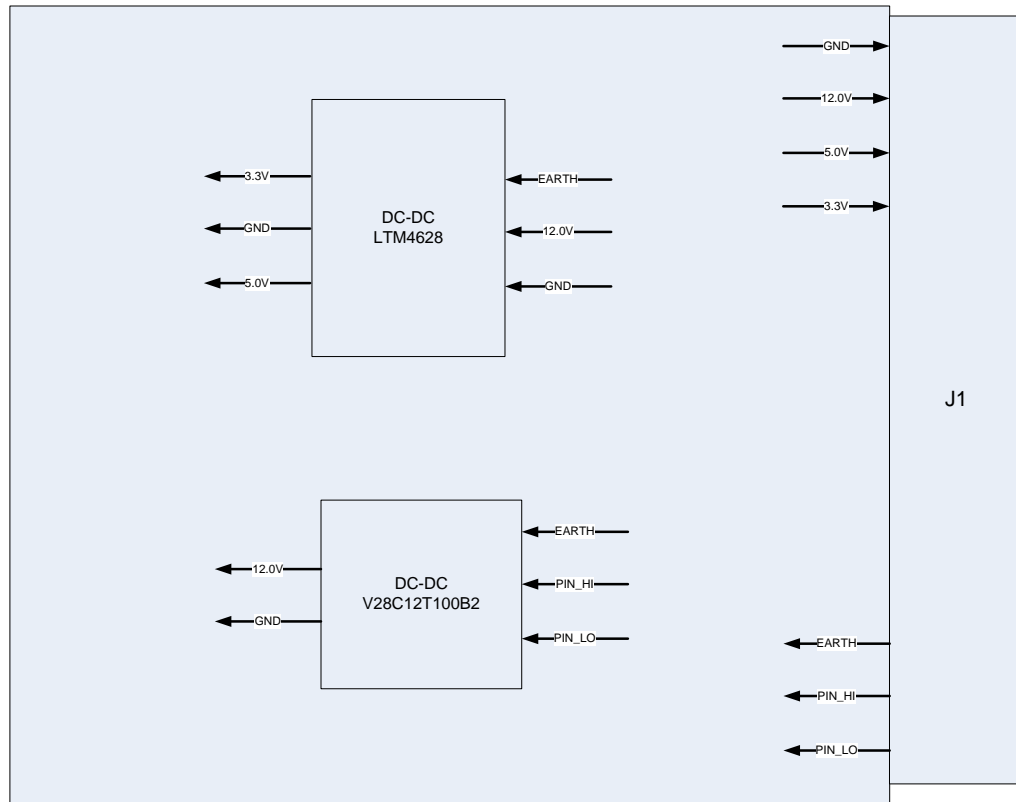

Figure 3.7 Functional block diagram of Power Supply Board

3.3.8 FILTER MODULE

This board is a Filter card used to filter the input (Input power 28 ± 4V) coming inside the module from the external world. The filtered is routed to the VPX backplane through a connector (VPX6W6M400A1 from positronic J2 mentioned in block diagram)

The input is routed from the circular connector to the feed-throughs and then to Molex connector(J1, 43045-0602).

The M-FIAM9 is a DC front-end module that provides EMI filtering and transient protection. The M-FIAM9 enables designers using Vicor's Maxi,

Mini, Micro Series 24 V & Maxi Series 28 V DC-DC converters to meet conducted emission / conducted susceptibility per MIL-STD-461E; and input transients per MIL-STD-704A/E/F and MILSTD-1275A/B/D. The M-FIAM9 accepts an input voltage of 10 – 36 Vdc

The output is routed to panel mount LED (Power LED) on the module. The switch when turned on will result in the LED to be turned ON and simultaneously allow the input power to be routed to the SC Module.
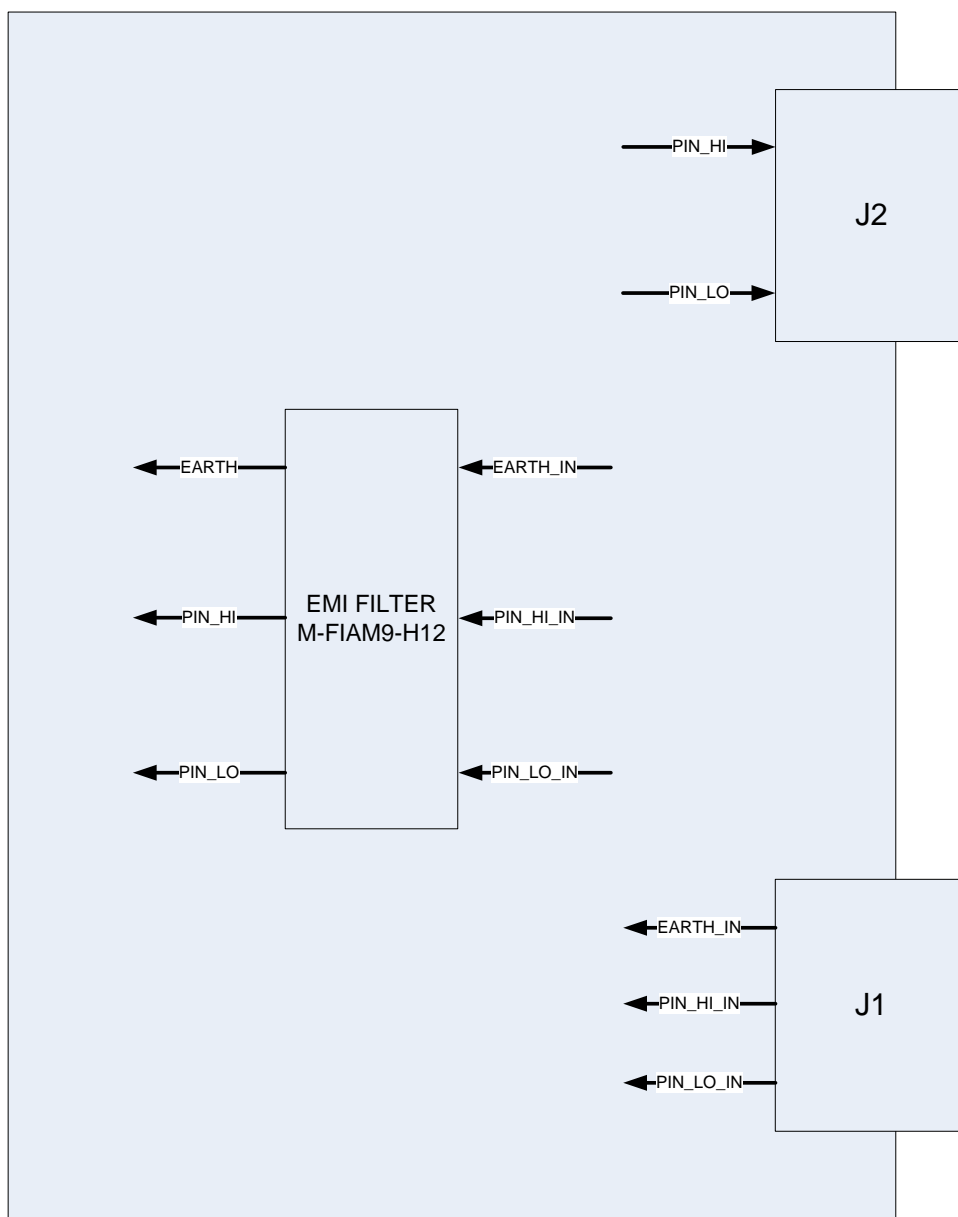

Figure 3.8 Functional block diagram of Filter Module

3.3.9 FLEX BACKPLANE INTERFACE
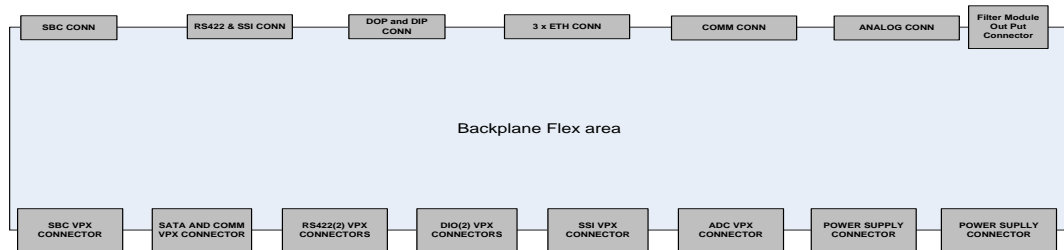
Figure 3.9 Functional block diagram of Flex Backplane Interface

This board would act as a 3U VPX backplane for the SC VPX boards such that the signals can be routed from individual 3U VPX P2 connectors of each of the PCB's to the circular connectors that are to be mounted on the SC rear plate. The filter power is routed to the power supply cards via. "Power connector" on this flex backplane PCB.

The PCB is a Flex-rigid PCB that has a routing from the individual PCB P2 connectors to the circular connector area of the PCB. The circular connector section of the PCB connects the rear panel of the SC module.

3.3.10 CONNECTOR DETAILS:

Table 3.11 Connector Specifications

Sl. No.	Connector Legend	Connector Description	Reference Designation	Connector Part No.	Source
1.	POWER	28V power input	J1	D38999/20 WB05PN	SOURIA U
2.	Circular connector	I/O Interface Connectors	SC-J2	8D0L23W 35PN	SOURIA U
3.	ETH-1,ETH-2,ETH-3	10/100/100 0 Mbps Ethernet	SC-J3,SC-J4,SC-J5	CFX20J11 08FAN	Tyco
4.	Circular connector	I/O Interface Connectors	SC-J6	8D0L21W 35SN	Souriau
5.	Circular connector	I/O Interface Connectors	SC-J7	8D0L23W 35SN	Souriau
6.	Circular connector	I/O Interface Connectors	SC-J8	8D0L25W 35SN	Souriau
7.	Circular connector	I/O Interface Connectors	SC-J9	8D0L25W 35PN	Souriau

3.3.11 KEY REQUIREMENTS IN TESTING

- PINAKA SJU test jig with cable

3.3.12 SOFTWARE DESIGN DETAILS

- Updated Linux kernel and driver files
- Updated GUI.

CHAPTER 4

ELECTROMAGNETIC COMPATIBILITY

4.1 ELECTROMAGNETIC INTERFERENCE

Any undesired signal in the form of radiated field or in the form of conducted current that can cause malfunction or degradation in the performance/normal functioning of any electrical or electronic product, system or device is known as electromagnetic interference. It could be due to the generation of any intentional or unintentional signals primarily from any electrical /electronic systems/devices/components etc.
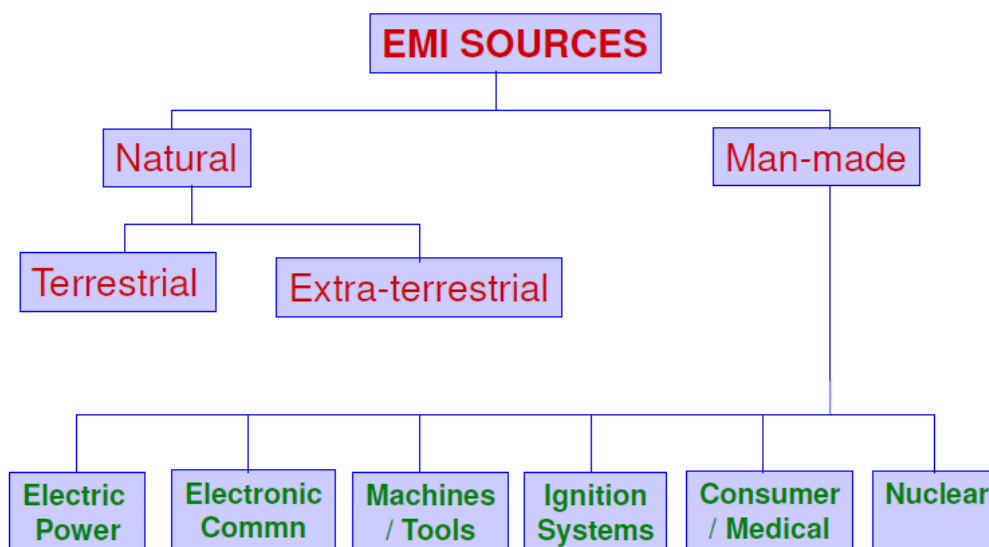
Figure 4.1 Electromagnetic Interference Sources

4.1.1 TYPES OF INTERFERENCE

- Conducted Interference
- Radiated Interference

- Conducted followed by radiated interference
- Radiated followed by conducted interference
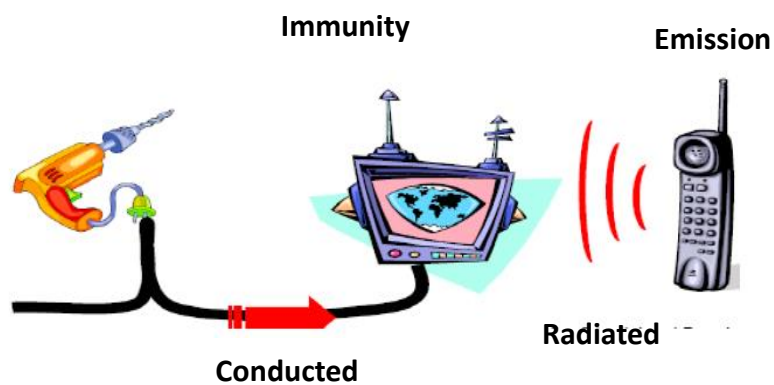
Figure 4.2 Electromagnetic Interference Types

4.1.2 EFFECTS OF EMI

EMI causes a malfunction in equipment where it gets coupled to it either in conducted form or in radiated form. Sometimes the effects are catastrophic. Therefore the level of EMI is to be controlled or reduced to prevent malfunctions in electrical /electronic systems or subsystems in a broad sense.
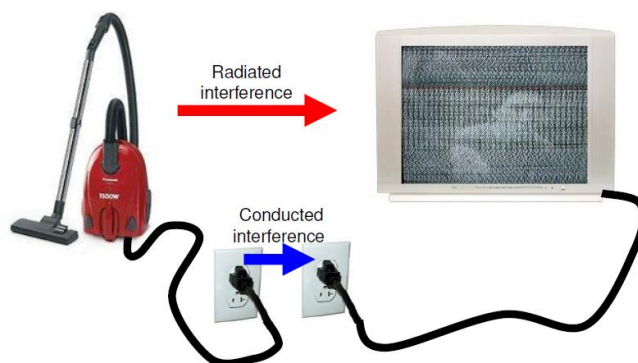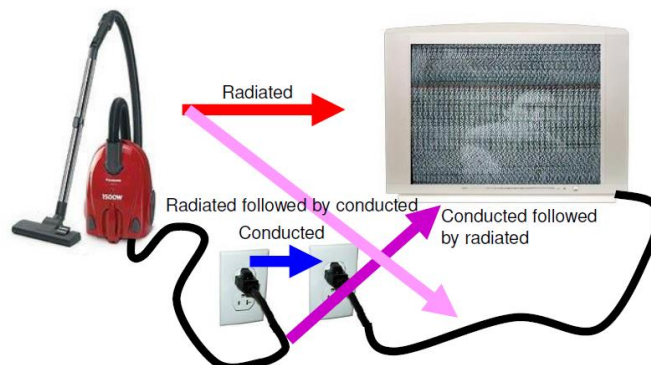

Figure 4.3 Conducted Interference

Figure 4.4 Radiated & Conducted Interference

4.2 ELECTROMAGNETIC COMPATIBILITY

It is the ability of electronic, electrical, and electromechanical systems to operate together efficiently and reliably, without being degraded due to electromagnetic interference (EMI) is called electromagnetic compatibility. Hence, it is achieved by addressing both emission and susceptibility issues, i.e., quieting the sources of interference and hardening the potential victims.

4.2.1 TYPES OF EMC

A pair of emitter and receptor/susceptor is said to work compatibly when the above conditions are achieved. There are three important stages of EMC namely:-

- Intrasystem EMC
- Intersystem EMC
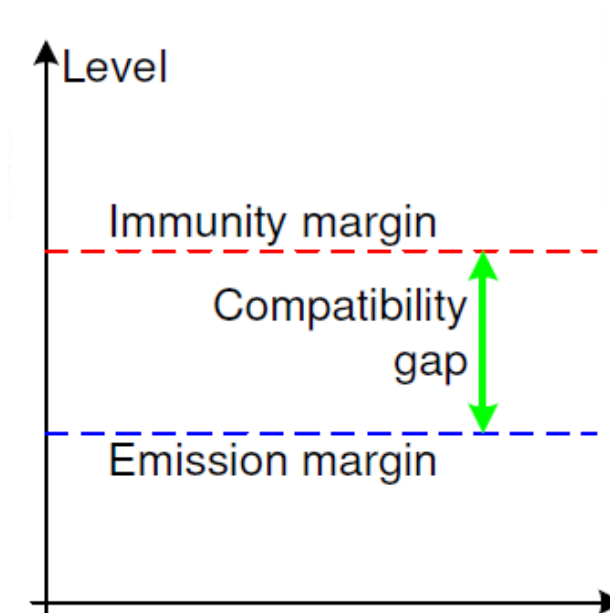- Operational Compatibility

Figure 4.5 Compatibility Gap

4.2.2 DANGER OF NON COMPLIANCE OF EMC

There can be a wide range of implications due to EMI and their effects can have various effects on a device or system. This includes the failure of a product or the accidents caused due to electromagnetic interference. It can also lead to loss of investment and time which could have been utilized judiciously. It can get the parent body involved in a legal suit and can cause its reputation to be at stake which could even lead to legal proceedings. Bans can be imposed on organisations if it jeopardizes the safety of people and equipment.

4.2.3 BENEFITS OF ADDRESSING EMC EARLY

Addressing the electromagnetic compatibility of a device or system can save a lot of precious time which can be utilized for other purposes. It will increase the cost-effectiveness of a machine and also become more reliable in terms of functioning and accuracy. A quality product will be obtained if EMC is addressed properly and in time and will also make it a better choice than other products in the market.

4.3 BASIC TERMINOLOGY

These are some terms and definitions which must be understood in order to understand EMI & EMC testing and compatibility. Being thorough in the understanding of these will ensure an in-depth understanding of EMC testing.

4.3.1 SHIELDED ENCLOSURES

To prevent interaction between the EUT and the outside environment, shielded enclosures will usually be required for testing. These enclosures prevent external environment signals from contaminating emission measurements and susceptibility test signals from interfering with electrical and electronic items in the vicinity of the test facility. Shielded enclosures must have adequate attenuation such that the ambient requirements are satisfied. The enclosures must be sufficiently large such that the EUT arrangement requirements and antenna positioning requirements described in the individual test procedures are satisfied.
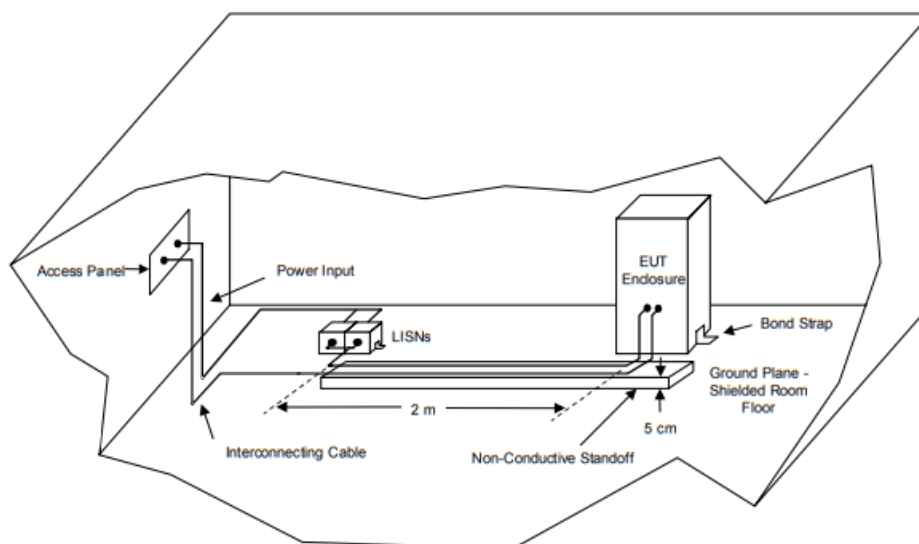
Figure 4.6 Test setup for freestanding EUT in a shielded enclosure

4.3.2 RADIO FREQUENCY (RF) ABSORBER MATERIAL

RF absorber material (carbon impregnated foam pyramids, ferrite tiles, and so forth) shall be used when performing electric field radiated emissions or radiated susceptibility testing inside a shielded enclosure to reduce reflections of electromagnetic energy and to improve accuracy and repeatability. The RF absorber shall be placed above, behind, and on both sides of the EUT (Equipment Under Testing), and behind the radiating or receiving antenna as shown in Figure 1. Minimum performance of the material shall be as specified in Table 4.1.

Table 4.1 Absorption at normal incidence

FREQUENCY	MINIMUM ABSORPTION
80 MHz-250 MHz	6 dB
Above 250 MHz	10 dB
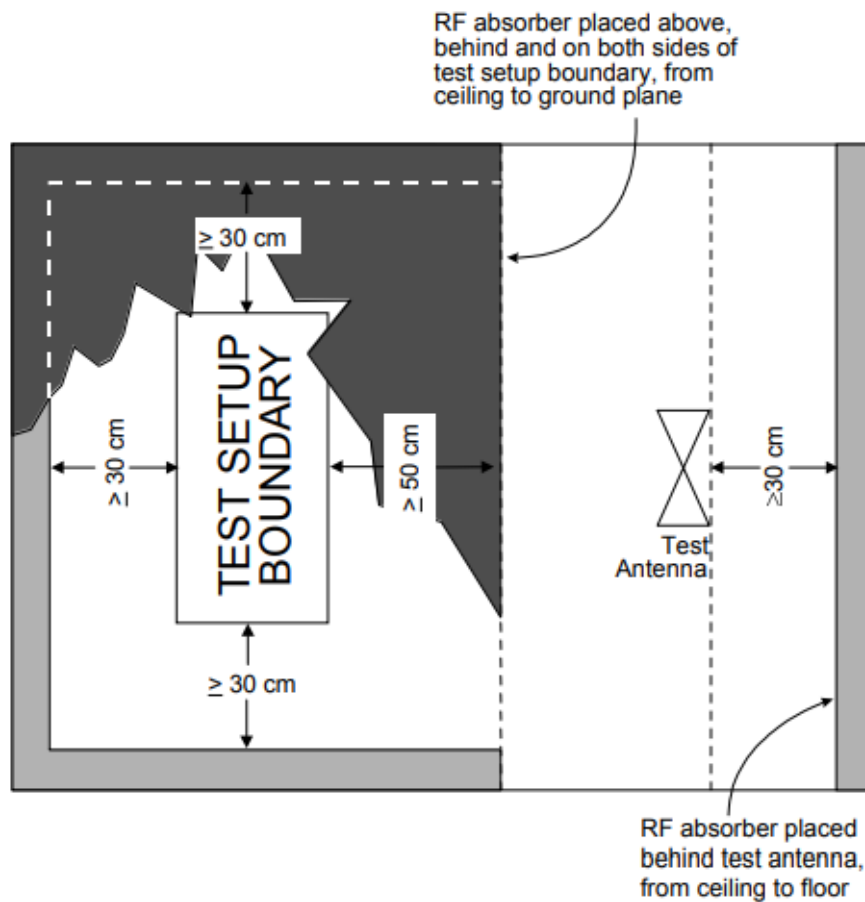
Figure 4.7 RF Absorber Loading Diagram

4.3.3 AMBIENT ELECTROMAGNETIC LEVEL

During testing, the ambient electromagnetic level measured with the EUT de-energized and all auxiliary equipment turned on shall be at least 6 dB below the allowable specified limits when the tests are performed in a shielded enclosure. Ambient conducted levels on power leads shall be measured with the

leads disconnected from the EUT and connected to a resistive load which draws the same rated current as the EUT. When tests are performed in a shielded enclosure and the EUT is in compliance with required limits, the ambient profile need not be recorded in the EMITR (Electromagnetic Interference Test Report). When measurements are made outside a shielded enclosure, the tests shall be performed during times and conditions when the ambient is at its lowest level. The ambient shall be recorded in the EMITR and shall not compromise the test results.
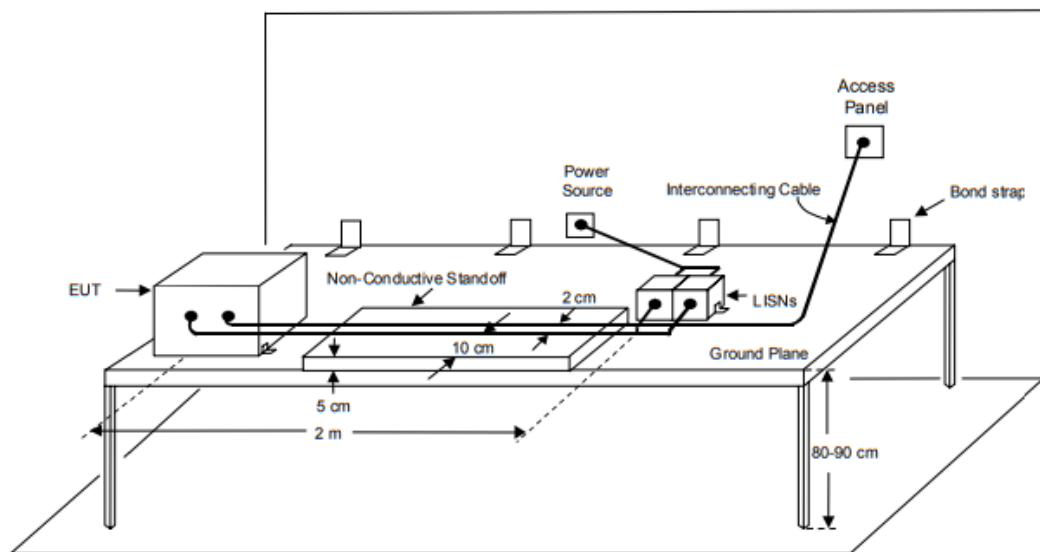
Figure 4.8 General Test Setup

4.3.4 GROUND PLANE

The EUT shall be installed on a ground plane that simulates the actual installation. If the actual installation is unknown or multiple installations are expected, then a metallic ground plane shall be used. Unless otherwise specified below, ground planes shall be 2.25 square meters or larger in area with the smaller side no less than 76 centimetres. When a ground plane is not present in the EUT installation, the EUT shall be placed on a non-conductive table.

4.3.5 POWER SOURCE IMPEDANCE

The impedance of power sources providing input power to the EUT shall be controlled by Line Impedance Stabilization Networks (LISNs) for all measurement procedures of this document unless otherwise stated in a particular test procedure. LISNs shall not be used on output power leads. The LISNs shall be located at the power source end of the exposed length of power leads. The LISN circuit shall be in accordance with the schematic shown in Figure 6. The LISN impedance characteristics shall be in accordance with Figure 7. The LISN impedance shall be measured at least annually.
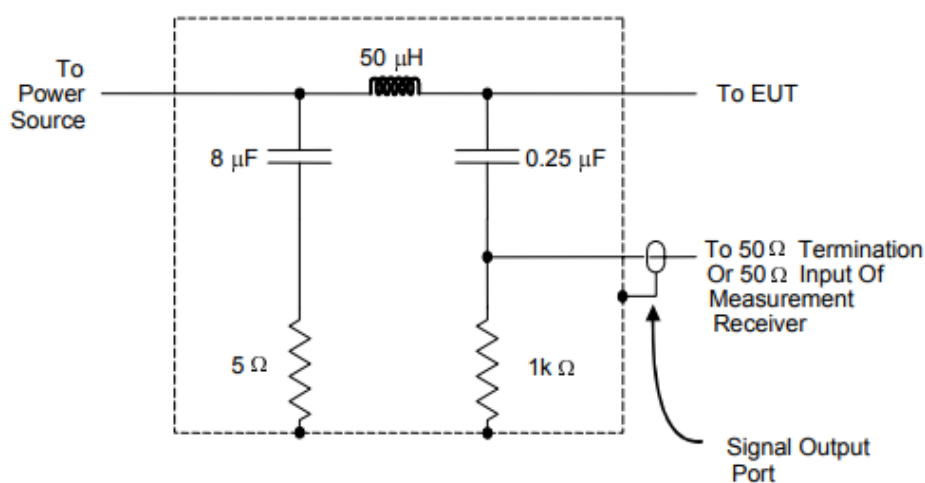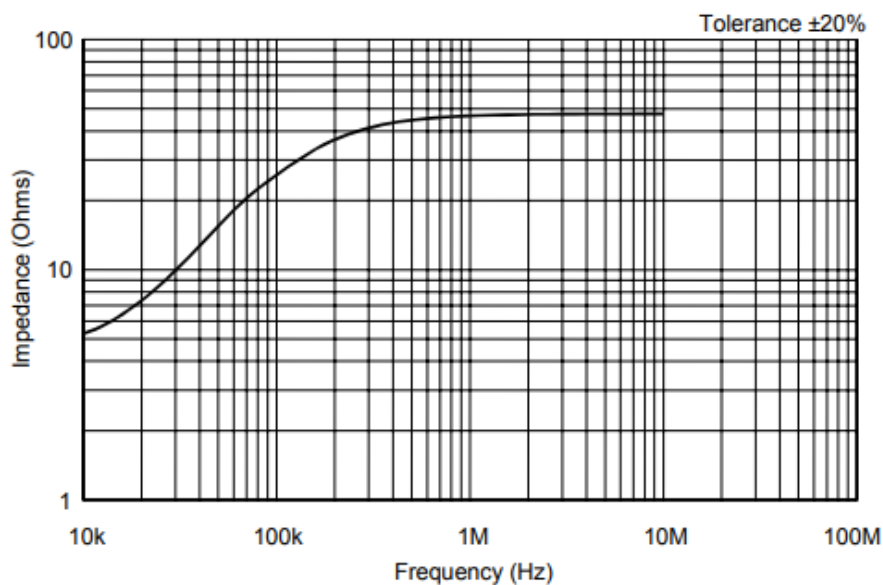
Figure 4.9 LISN Schematic

Figure 4.10 LISN Impedance

4.3.6 RF HAZARDS

Some tests in this standard will result in electromagnetic fields which are potentially dangerous to personnel. The permissible exposure levels shall not be exceeded beyond limits in areas where personnel are present. Safety procedures and devices shall be used to prevent accidental exposure of personnel to RF hazards.

4.3.7 DETECTOR

A peak detector shall be used for all frequency domain emission and susceptibility measurements. This device detects the peak value of the modulation envelope in the receiver bandpass. Measurement receivers are calibrated in terms of an equivalent Root Mean Square (RMS) value of a sine wave that produces the same peak value. When other measurement devices such as oscilloscopes, non-selective voltmeters, or broadband field strength sensors are used for susceptibility testing, correction factors shall be applied for test signals

to adjust the reading to equivalent RMS values under the peak of the modulation envelope.

4.4 TESTING

Individual emission or susceptibility requirements and their associated limits and test procedures are grouped together. The applicable frequency range and limit of many emission and susceptibility requirements vary depending on the particular platform or installation. The test procedures included in this section are valid for the entire frequency range specified in the procedure; however, testing only needs to be performed over the frequency range specified for the particular platform or installation.

Table 4.2 Emission & Susceptibility Tests

REQUIREMENT	DESCRIPTION
CE101	Conducted Emissions, Power Leads, 30 Hz to 10 kHz
CE102	Conducted Emissions, Power Leads, 10 kHz to 10 MHz
CE106	Conducted Emissions, Antenna Terminal, 10 kHz to 40 GHz
CS101	Conducted Susceptibility, Power Leads, 30 Hz to 150 kHz

CS103	Conducted Susceptibility, Antenna Port, Intermodulation, 15 kHz to 10 GHz
CS104	Conducted Susceptibility, Antenna Port, Rejection of Undesired Signals, 30 Hz to 20 GHz
CS105	Conducted Susceptibility, Antenna Port, Cross-Modulation, 30 Hz to 20 GHz
CS109	Conducted Susceptibility, Structure Current, 60 Hz to 100 kHz
CS114	Conducted Susceptibility, Bulk Cable Injection, 10 kHz to 200 MHz
CS115	Conducted Susceptibility, Bulk Cable Injection, Impulse Excitation
CS116	Conducted Susceptibility, Damped Sinusoidal Transients, Cables and Power Leads, 10 kHz to 100 MHz
RE101	Radiated Emissions, Magnetic Field, 30 Hz to 100 kHz
RE102	Radiated Emissions, Electric Field, 10 kHz to 18 GHz
RE103	Radiated Emissions, Antenna Spurious and Harmonic Outputs, 10 kHz to 40 GHz

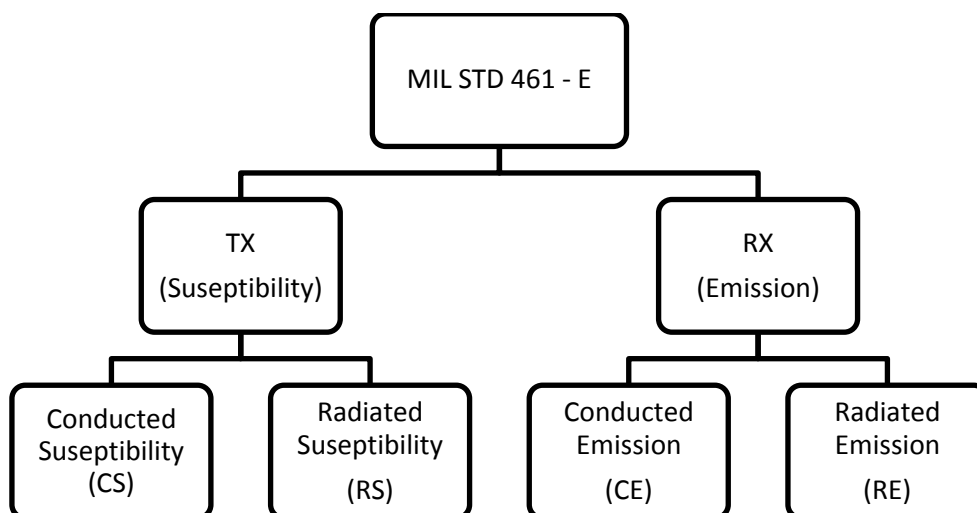|	
RS101	Radiated Susceptibility, Magnetic Field, 30 Hz to 100 kHz
RS103	Radiated Susceptibility, Electric Field, 2 MHz to 40 GHz
RS105	Radiated Susceptibility, Transient Electromagnetic Field

Figure 4.11 Categories of Testing

4.4.1 TEST RESULTS

Various tests had been conducted to test the ruggedness and susceptibility of the system controller module. These tests are aimed at reducing the electromagnetic interference caused by the device to other installations in contact or in the vicinity, and also to increase the immunity of the device and compatibility with other devices or installations nearby.
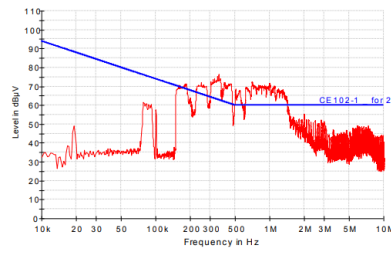
Figure 4.12 CE 102-24V DC Positive
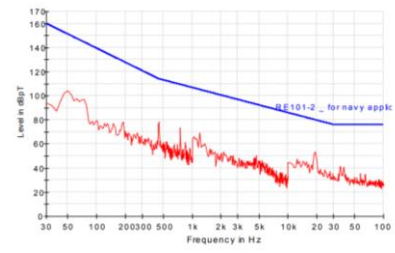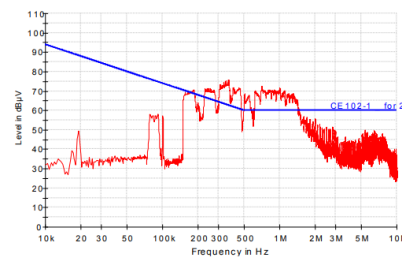

Figure 4.16 RE101-24V DC Front Centre position
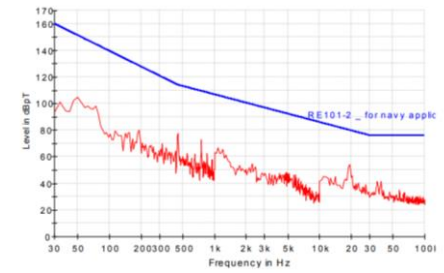

Figure 4.13 CE 102-24V DC Negative

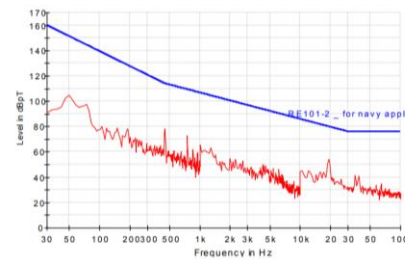**Figure 4.17 RE 101-24V DC Right Side**

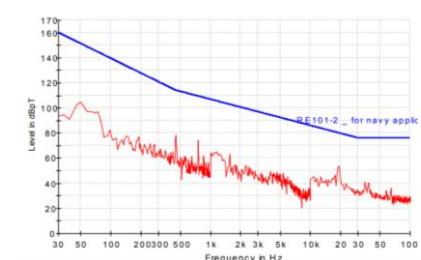
Figure 4.14 RE101- 24V DC Front Top side

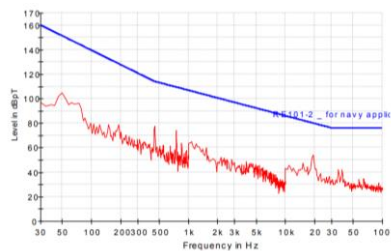**Figure 4.18 RE101-110V DC Front Top**
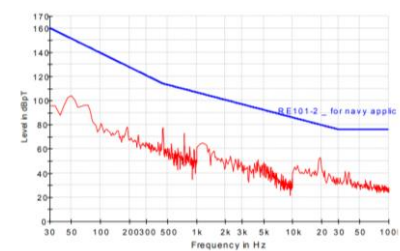

Figure 4.15 RE101- 24V DC Left side

Figure 4.19 RE101-110V DC Front Down

4.4.2 INFERENCE

From the test results it is inferred that the conducted emission levels as per the CE 102 test is not in compliance with the standards. Various steps such as proper grounding, using better shielded enclosures and RF absorber materials are used to make the module to comply with the standards. It is also inferred that the radiated emission levels as per the RE 101 test is in compliance with the standards. The radiated emission levels are 6 dB lower than the limit line and it meets the standard requirements.

Figure 4.20 Missile Launcher in Action

CHAPTER 6

CONCLUSION

A flexible and efficient launcher control system has been developed to accomplish the mission it is assigned. It is efficient in the number of tasks it performs and ensures high operational mobility, flexibility and accuracy which gives the system an edge in modern artillery warfare. It has been developed under the guidance of experienced personnel at Tata Power SED and has proven to be more cost effective and have a better control capability. It employs a plurality of cards, each card having a specific function and being interconnected by a backplane bus system which also couples the cards to other components of the launcher control system. A number of factors are responsible for the successful launch of missiles and it involves multiple streams of engineering and technology. Since the use of modern weapons systems has revolutionised the concept of warfare, this particular module will be an important contribution to the ever evolving technology in the field of modern military warfare.

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[5]. Allan E. Gamble and Philip N. Jenkins, US Army Aviation and Missile Command; "Low Cost Guidance the Multiple Launch Rocket System (MLRS) Artillery Rocket".

[6]. MIL-STD-461E (20 August 1999), Department of Defence Interface Standard - Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment.

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