## **ACADEMIC CURRICULA**

**Professional Core Courses** 

**ELECTRONICS AND COMMUNICATION ENGINEERING** 

Regulations - 2018



SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Kancheepuram, Tamil Nadu, India

Cou		18ECC102J Course Name	ELECTRONIC DEVICES		Cours Catego		С					Profe.	ssion	al Cor	е				1	_ T	P 2	C 4
Co	requisite ourses Offering	18EES101J  Department Electronics and Com	Co-requisite Courses  Mil  Mulication Engineering  Data Bo	ook / Codes/Standards		rogre: Cour		18ECC	201J													
Course	Learning	g Rationale (CLR): The purpose of learning	ng <mark>this course i</mark> s to:	CHEC	L	earniı	ng					Pr	ograr	n Lea	rning (	Outco	mes (	PLO)	)			
CLR-1	: Provi	de a basis for understanding semiconductor	<mark>material, ho</mark> w a pn junction is formed and	its principle of operation	1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CLR-2		in the importance of diode in electronic ci <mark>rcu</mark>																			±	_
CLR-3		iss the basic characteristics of several <mark>other t</mark>							ж.		5			<u>i</u>							ner	Research
CLR-4		ribe the basic structure, operation an <mark>d charac</mark>			Ē	(%	(%	a:	g Pr		arc			labi		بح					ıgeı	ese
CLR-5	: Desci	ribe the basic structure, operation a <mark>nd charac</mark> fier.	cteristics of MOSFET, and discuss its use	e as a switch and an	) (Bloo	ency (	nent (º	wledg	S	pmen	, Rese	age	(I)	Sustainability		Team Work		Finance	و ق	onal	t Mana	∞ ठ
CLR-6		modern engineering tools such as <mark>PSPICE t</mark> o nethods used by technicians an <mark>d electroni</mark> c e		experience with instruments	Thinking (Bloom)	d Profici	d Attainr	ring Kno	Analysi	& Development	, Design, Research	Tool Usage	& Culture	nent & S		ıl & Tea	ication	<u>۲</u> ∞	g Learning	–1: Professional evement	<ol> <li>Project Management ques</li> </ol>	3: Analyze
		, , ,	rse, learners will be able to:		Level of	Expected Proficiency (%)	Expected Attainment (%)	Fnaineering Knowledge	Problem Analysis	Design &	Analysis,	Modern	Society 8	Environment &	Ethics	Individual &	Communication	Project Mgt.	Life Long I	PSO-1: Profe Achievement	PSO – 2: Pr Techniques	PSO – 3
CLO-1		iin the operation, characteristi <mark>cs, param</mark> eters		les and special diodes	1	60	70	Н	-	-	-	-	-	-	-	-	-	-	М	-	-	-
CLO-2		ate important applications of s <mark>emicond</mark> uctor (		CONTROL OF THE	2	60	70	-	-	-	-	-	-	-	-	-	-	-	М	-	-	-
CLO-3		ew bipolar transistor constructi <mark>on, opera</mark> tion, o witching.	characteristics and parameters, as well a	s its application in amplification	1	60	70	Н	-	-	-	-	-	-	-	-	-	-	М	-	-	-
CLO-4		ew field-effect transistor constr <mark>uction, o</mark> peration fields and switching.	on, characteristics and parameters, as we	ell as its application in	1	60	70	Н		0.5	7	-	-	-	1	-	-	-	М	-	L	•
CLO-5		truct a circuit, then make funct <mark>ional mea</mark> sure	ments to understand the operating charac	cteristics of the device / circuit.	3	70	75	-	TIP.			Н	-	-	-	-	-	-	-	L	L	-
CLO-6	: Solve	e specific design problem, which <mark>after co</mark> mple	tion will be verified using modern enginee	ering tools such as PSPICE.	2	70	75	-	-	-	-	Н	-	-	L	Н	М	-	М	-	-	-
,		0	D: 1.0: "	018:	1				D:								100 5			_		
Duration	n (hour)	Semiconductor Diodes 15	Diode Circuits	Special Dioc	ies				Ribola	r Juno	15	ransı	stors			IV	105 F	ieia-E		ırans	sistors	
S-1	SLO-1	Basic semiconductor theory: Intrinsic & extrinsic semiconductors	15  HWR operation, Efficiency and ripple fac	15 ctor Backward diode				Physi <mark>c</mark> a	l struc	ture	10	Ť	Ť		Phy	sical	struct	ure	15			
3-1	SLO-2	Current flow in semiconductors	Problem solving	Varactor diode				Device	opera	tion of	BJT					rice o		on of	f E-M	OSFE	T & D-	-
SLO-1 PN junction theory: Equilibrium PN junction Center-Tapped Transformer FWR operation, Efficiency and ripple factor Step recovery diod								Current configui		ge cha	aracte	ristics	of C	E BJ1	I-V	chara	acteris	tics c	s of E-MOSFET			
3-2	01.0.0	B						Current	-Volta	ae cha	aracte	ristics	of C	F BJ1	- T_							

Point-contact diode

Energy band diagram

Schottky Diode

Lab 4: Diode clipping and clamping circuits Lab 7: Series and Shunt Regulators

Metal-semiconductor junction: Structure,

Forward & Reverse Characteristics of

SLO-2 Forward biased PN junction

Reverse biased PN junction

SLO-2 Relation between Current and Voltage

Lab 1: PN Junction Diode Characteristics

SLO-1

SLO-1 SLO-2

S-3

Problem solving

Problem solving

ripple factor

Bridge FWR operation, Efficiency and

Current-Voltage characteristics of CE BJT

Current-Voltage characteristics of CB BJT

Current-Voltage characteristics of CB BJT

Lab 10: BJT and MOSFET Switching

configuration

configuration

configuration

Circuits

Problem solving

Problem solving

Derive drain current

Lab 13: Repeat Experiments

S-6	SLO-1	Calculate depletion width	Filters: Inductor & Capacitor Filters	Tunnel Diode	Current-Voltage characteristics of CC BJT configuration	Derive transconductance
5-0	SLO-2	Calculate barrier potential	Problem solving	Tunnel Diode	Current-Voltage characteristics of CC BJT configuration	Problem solving
S-7	SLO-1	Derive diode current equation	Filters: LC & CLC Filters	Gunn Diode	BJT as an amplifier	CMOS FET
5-7	SLO-2	Derive diode current equation	Problem solving	Gunn Diode	BJT as a switch	MOSFET as an amplifier
S-8	SLO-1	Effect of Capacitance in PN junction: Transition Capacitance	Diode Clippers	IMPATT Diode	BJT circuit models - h-parameter	MOSFET as a switch
	SLO-2	Diffusion Capacitance	Problem solving	IMPATT Diode	BJT circuit models - hybrid-π parameter	Problem solving
S 9-10	SLO-1 SLO-2	Lab 2: Zener diode characteristics	Lab 5: BJT Characteristics	Lab 8: MOSFET Characteristics	Lab 11: Photoconductive Cell, LED, and Solar Cell Characteristics	Lab-14: Model Examination
S-11	SLO-1	Energy band structure of PN Junction Diode	Diode Clampers	PIN Diode	BJT biasing circuits and stability analysis: Base bias and emitter bias	Biasing Circuits for MOSFET: Gate Bias
5-11	SLO-2	Ideal diode and its current-voltage characteristics	Problem solving	PIN Photodiode	Problem solving	Problem Solving
	SLO-1	Terminal characteristics & parameters	Voltage Multipliers	Avalanche photodiode	Voltage-divider bias	Self-bias
S-12	SLO-2	Diode modeling	Zener diode: Characteristics, breakdown mechanisms	Laser diode	Problem solving	Problem Solving
S-13	SLO-1	DC load line and analysis	Zener resistances and temperature effects Zener diode as voltage regulator	Problem solving	Collector-feedback bias	Voltage-divider bias
	SLO-2	Problem solving	Problem solving	Problem solving	Problem solving	Problem Solving
S 14-15	SLO-1 SLO-2	Lab 3: Diode rectifier circuits	Lab 6: BJT Biasing Circuits	Lab 9: MOSFET Biasing Circuits	Lab 12: Simulation experiments using PSPICE	Lab 15: End-Semester Practical Examination

	1.	David A. Bell, Electronic Devices and Circuits, 5th ed., Oxford University Press, 2015	5.	Robert L. Boylestad, Louis Nashelsky, Electronic Devices and Circuit Theory, 11th ed., Pearson Education, 2013
Learning	2.	Donald Neamen, Electronic Circuits: Analysis and Design, 3rd ed., McGraw-Hill Education, 2011	6.	Muhammad Rashid, Microelectronic Circuits: Analysis & Design, 2nd ed., Cengage Learning, 2010
Resources	3.	Adel S. Sedra, Kenneth C. Smith, Microelectronic Circuits: Theory and Applications, OUP, 2014	7.	Muhammed H Rashid, Introduction to PSpice using OrCAD for circuits and electronics, 3rd ed., Pearson, 2004
	4.	Thomas L. Floyd, Electronic Devices", 9th ed., Pearson Education, 2013	8.	Laboratory Manual, Department of ECE, SRM University

Learning Assess	sment		100								
	Bloom's			Conti	inuous Learning Ass	essment (50% weig	htage)			Final Evamination	n (50% weightage)
	Level of Thinking	CLA –	1 (10%)	CLA –	2 (15%)	CLA –	3 (15%)	CLA -	4 (10%)#	Filiai Examination	n (50% weightage)
	Level of Thirtking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%
Level 2	Apply Analyze	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
Level 3	Evaluate Create	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
	Total	10	00 %	10	0 %	10	0 %	10	00 %	10	00 %

<sup>#</sup> CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	1. Mr. Manikandan AVM, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	2. Dr. Diwakar R Marur, SRMIST

Co. Co		18ECC103J Course Name	DIGITAL ELECTRONIC PRI	NCIPLES	Course atego		С					P	rofes	siona	l Core	Э				3	0	P 2	4
С	requisite ourses	18EES101J	Co-requisite Nil			rogres Cours		18EC	C20	3J													
Course	Offering	Department Electronics and Con	nmunication Engineering Dat	a Book / Codes/Standards	Nil																		
Course	Learning	g Rationale (CLR): The purpose of learn	ing this course is to:		L	.earnii	ng			ı			Pro	ogram	Lea	rning	Outco	mes (	PLO)				
CLR-1	: Unde	erstand binary codes, digital arithmetic oper <mark>a</mark>	tions and able to simplify Boolean log	ic expressions	1	2	3	15	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LR-2		ribe how basic TTL and CMOS gates ope <mark>ra</mark> t		Day (at least		1																ı	ء
LR-3		to design simple combinational logics <mark>using</mark>	basic gates and MSI circuits	and the latter of the later					7			5			i i							me	S C
LR-4		liarize with basic sequential logic com <mark>ponen</mark> analyze sequential logic circuits and <mark>Finite S</mark>		neir usage, and able to design	loom)	(%) k:	ıt (%)	N.	edge	9	ent	Research			tainab		Vork		Finance		<del></del>	anage	3. Analyze & Research
LR-5		v how to implement logic circuits u <mark>sing PLDs</mark>		The second	) (B	enc	ner		wle	S	mdo	Α,	age	Ф	onst		N V		inar	В	Ö	Ĕ	4
LR-6	: Use r	modern engineering tools such as PSPICE / Iments and methods used by te <mark>chnicians</mark> an	Logisim to carry out design experime d electronic engineers	nts and gain experience with	Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)		Engineering Knowledge	Problem Analysis	Development	Design,	Modern Tool Usage	& Culture	Environment & Sustainability		ndividual & Team Work	cation	gt. & F	ife Long Learning	Professional nent	Project Management	Analyz
					ofT	ted	ted		erii	m /	∞	. <u>is</u>	n T	∞ >	u H		ual	iù	Ĕ	gu	1: P em	. 2: igue	۔ ذ
ourse	Learning	g Outcomes (CLO): At the end of this cou	urse, learners will be able to:		Level	Expeci	Expeci	64	Engine	Proble	Design &	Analysis,	Moder	Society	Enviro	Ethics	Individ	Communication	Project Mgt. &	Life Lo	PSO-1: F Achieven	PSO – 2: Pro Techniques	- 050
CLO-1		lify Boolean expressions; carry out arithmeticorrection.	c operations with binary numbers; app	ply parity method for error detection	1	90	75		Н	-			•	-	-	-	-	-	-	-	-	-	-
CLO-2		ain the operational characteris <mark>tics / pro</mark> pertie I two major IC technologies, TT <mark>L and C</mark> MOS		ell as other types of IC devices	1	80	70	13	Н	-		-	•	-	-	-	-	-	-	-	-	-	-
LO-3		ify eight basic types of fixed-fu <mark>nction co</mark> mbin in building complete digital sys <mark>tems suc</mark> h as		te how the devices / circuits can be	2,3	90	75	W	•	М	Н	82	Н	-	-	-	-	-	-	-	-	-	-
LO-4	: Analy	ze and design Mealy and Moore models of	sequential circuits using several types	of flip-flops.	2,3	90	75		-	М	Н	-	Н	-	-	-	-	-	-	-	-	-	-
LO-5	: Imple	ement multiple output combinati <mark>onal logic</mark> cir	cuits using PLDs; Explain the operation	on of a CPLD and FPGA.	2	80	75		-	М	Н	-	L	-	-	-	-	-	-	-	-	-	
CLO-6	: Solve Logis	e specific design problem, which <mark>after com</mark> pl sim	etion will be verified using modern eng	gineering tools such as PSPICE /	2	90	75		F	М	Н	-	Н	-	-	-	Н	-	-	-	М	-	L
										ď								•		•		,	
Durati	on (hour)	Binary Codes, Digital Arithmetic and Simplification of Boolean Functions	Logic Families	Combinational S	ystem	S	- 100			Sequ	uentia	al Sys	stems				Men	nory a	nd Pro	ogran	nmabl	le Logi	С
		15	15	15						70	1	5								15			
S-1	SLO-1	Binary Codes, Digital Arithmetic and Simplification of Boolean Functions	Introduction	Binary arithmetic units	١,			Flip-flo								RA.	М Ме	mory	decod	ling			
	SLO-2	Error detecting codes	TTL Logic Family	Adder				JK flip-	-flop,	T flip	o-flop,	, D fli <sub>l</sub>	p-flop	)		RO							
S-2	SLO-1	Error correcting code	Totem-pole TTL	Design of Half adder				Maste	r-sla	ve RS	S flip-f	flop						mable ncepts		Dev	rices (I	PLDs).	
SLO-2 Hamming Code open-collector and tristate TTL Design of Full adder Master-slave JK flip-flop PROM																							
		•	0 1 111 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1																				

Course

Course

Course

Arithmetic number representation

LAB 1: Study of logic gates

SLO-1

SLO-1

SLO-2

SLO-2 Binary arithmetic

S-3

I T P C

functions using standard ICs

Design subtractor using logic gates

LAB 7: Implement combinational logic

Subtractor

Registers & Counters

Synchronous Counters

Shift registers (SISO, SIPO, PISO, PIPO)

LAB 10: Design and implement

PROM as PLD

using Logisim

Programmable Array Logic (PAL)

LAB 13: Construct combinational circuit

Schottkey TTL, standard TTL

decoder using logic gates

Metal Oxide Semiconductor logic families

LAB 4: Design and implement encoder and

characteristics

S-6	SLO-1	Hexadecimal arithmetic	N-MOS	n-bit parallel adder & subtractor	Universal shift register	Programmable Array Logic (PAL)
3-0	SLO-2	Hexadecimal arithmetic	P-MOS	look ahead carry generator	Counters: Asynchronous/Ripple counters	Programmable Logic Array (PLA)
	SLO-1	BCD arithmetic simplification	CMOS logic circuits	Decoder	Synchronous counters, Modulus-n Counter	Programmable Logic Array (PLA)
S-7	SLO-2	Minimization of Boolean Functions: Algebraic simplification	Characteristics of MOS logic	Encoder	Ring counter, Johnson counter	Design combinational circuits using PLD's
S-8	SLO-1	Problems on Algebraic simplification	Compare MOS logic circuits(CMOS) with TTL digital circuit	Multiplexer		Design combinational circuits using PLD's
	SLO-2	Karnaugh map simplification	Electrical characteristics	Demultiplexer	Mealy a <mark>nd Moore mo</mark> del	Design combinational circuits using PLD's
S 9-10		LAB 2: Design and implement Adder and Subtractor using logic gates	LAB 5: Design and implement Multiplexer and Demultiplexer using logic gates	LAB 8: Verify characteristic table of flip- flops	LAB 11: Construct and verify shift registers	LAB 14: Model Practical Examination
S-11		Problems on Karnaugh map simplification	Fan-out	Code converters	1.Synchronous IC.Jockeni seguenuai circuiis	Design of combinational circuits using PLD's
	SLO-2	Problems on Karnaugh map simplification	Propagation Delay	Magnitude comparators	Synchronous (Clocked) sequential circuits	Design sequential circuits using PLD's
	SLO-1	Quine McCluskey	Power dissipation	Magnitude comparators	Synchronous (Clocked) sequential circuits	Design sequential circuits using PLD's
S-12	SLO-2	Tabulation method	Noise margin	Parity generators (Odd parity)	Analyze and design synchronous sequential circuits	Design sequential circuits using PLD's
C 12	SLO-1	Problems on Quine McCluskey or Tabulation method.	Supply voltage levels	Parity generators (Even parity)	State reduction	Design sequential circuits using PLD's
S-13	SLO-2	Exercise problems using Tabulation method	Operational voltage levels	Implementation of combinational logic by standard IC's.	State assignment	Design sequential circuits using PLD's
S 14-15		Lab 3: Design and Implemen <mark>t 2-bit</mark> Magnitude Comparator usin <mark>g logic gat</mark> es	LAB-6: Design and implement code converters using logic gates	LAB 9: Construct and verify 4-bit ripple counter, Mod-10/Mod-12 ripple counters	Lab 12: Construct mini project work	LAB 15: University Practical Exam

	1.	Morris Mano M, Michael D. Ciletti, Digital Design with an Introduction to the Verilog HDL, 5th ed., Pearson Education,	4.	Ronald J. Tocci, Digital System Principles and Applications, 10 <sup>th</sup> ed., Pearson Education, 2009
Learning		2014	5.	Donald P Leach, Albert Paul Malvino, Goutam Saha, Digital Principles and Applications, 6th ed.,
Resources	2.	Charles H Roth (Jr), Larry L. Kinney, Fundamentals of Logic Design, 5th ed., Cengage Learning India Edition, 2010		Tata-Mcgraw Hill, 2008
	3.	Thomas L. Floyd, Digital Fundamentals, 10th ed., Pearson Education, 2013	6.	LAB MANUAL, Department of ECE, SR <mark>M Universi</mark> ty

Learning Asse	essment									Т	
	Bloom's		10 m/L	Conti	nuous Learning Ass	essment (50% weig	ıhtage)			Einal Evaminatio	n (50% weightage)
		CLA –	1 (10%)	CLA -	2 (15%)	CLA –	3 (15%)	CLA -	4 ( <mark>10%)#</mark>	I IIIai Lxaiiiiiaiio	ii (50% weigiilage)
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
r. Level 1	Remember Understand	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%
Level 2	Apply Analyze	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
Level 3	Evaluate Create	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
	Total	10	0 %	10	0 %	10	0 %	10	0 %	10	00 %

<sup>#</sup> CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	1. Mr. Viswanathan B, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	

Course Code	18ECC104T	Course Name	SIGNALS AND SYSTEMS		Cours Catego		С					Profe	ssion	al Coi	re					L -	Г Р I 0	2
Pre-requisite Courses	e 18EES101J	Flectronics and Co.	Co-requisite Nil Courses Nil mmunication Engineering Data Bool	k / Codes/Standards		rogre Cour	essive	18E0	C204	J												
Course Offerin	ід Бераніпені	Liectronics and con	Timunication Engineering   Data Book	r / Codes/Otandards	1																	
Course Learnii	ng Rationale (CLR):	The purpose of learr	ning <mark>this course i</mark> s to:	The state of the s	- L	.earni	ng					Pı	ograr	n Lea	rning	Outco	omes	(PLC	))			
CLR-1: Knc	ow about requirement	ts of signal and system a	a <mark>nalysis in co</mark> mmunication.		1	2	3	10	1 2	2 3	4	5	6	7	8	9	10	11	12	13	14	15
			<mark>lic Ćontinu</mark> ous time Signals using Fourier sen	ies and transforms				- 7						>								i.
			Laplace transform and Convolution integral	and the ballion	=	_					Research			Sustainability							S	Research
			time signals and system through DTFT, Conv	olution sum	Jon I	8	%)		ge	=	sea			ina		농		စ္ပ			l and	Š
		of Z-Transform for the			<u>ĕ</u>	ြင့်	ent	ъ.	Jed	l le	Re	e e		ısta		Š		Finance	_	nal	l Ĕ	~
CLR-6 : sysi	tems and also the ab blems	ility to apply m <mark>odern cor</mark>	domain approaches to the analysis of conting Inputation software tool for the analysis of ele		.evel of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)		Engineering Knowledge	Design & Development	(n)	Modern Tool Usage	Society & Culture	Environment & Su	ics	ndividual & Team Work	Communication	Project Mgt. & Fir	Life Long Learning	PSO-1: Professional Achievement	SO – 2: Project Management Techniques	O – 3: Analyze
Course Learnii	ng Outcomes (CLO):	At the e <mark>nd of this</mark> co	urse <mark>, learners</mark> will be able to:		Lev	Ä	EX	37.		Des l	Ans	Š	Soc	E	Ethics	<u>la</u>	Ö	P.	Life	PSO-: Achie	PSO Mana	OSG
CLO-1: Und	derstand the various	classifications of Signal	s and Systems	Control of Maria	1	65	60	1	Н .		-	-	-	-	-	-	-	-	-	-	-	-
CLO-2: Ana	alyze Periodic and Ap	periodic Co <mark>ntinuous t</mark> ime	Signals using Fourier series and Fourier Tra	nsform	2	65	60		- <i>F</i>	1 -	-	-	-	-	-	-	-	-	-	-	-	-
CLO-3: Ana	alyze and characteriz	e the Conti <mark>nuous tim</mark> e s	ystem through Laplace transform and Convol	lution integral.	2	65	60		- <i>F</i>	1 -	-	-	-	-	-	-	-	-	-	-	-	-
CLO-4: Ana	alyze and characteriz	e the Discr <mark>ete time s</mark> igna	als and system through DTFT, Convolution so	um	2	65	60		-   F	1 M	-	-	-	-	-	-	-	-	-	-	-	-
		e the Discr <mark>ete time s</mark> yste		Marin mark	2	65	60		- <i>H</i>	1 M	-	-	-	-	-	-	-	-	-	-	-	L
.i U-n ' i ' '	oly the mathematical plysis	technique <mark>s u</mark>	sed for continuous-time signal and discrete-t	time signal and system	2	65	60	M	- F	-	М	М	-	-	-	-	-	-	-	L	-	-
	•																•		•			
	Classification o	of Signals and <mark>Systems</mark>	Analysis of Continuous Time Signals	Analysis of LTI (	CT Syst	em		Ar	alysis	of DT	Signa	ls and	Syst	ems						DT Sy Insfor		
Duration (hou	r)	12	12	12							12								12			
SLO-1	1 Introduction to sig	nals and systems	Introduction to Fourier series	System modeling				Repre	sentat	ion of	seque	nces			Z	transf	orm –	- intro	ductio	on		
S-1	Requirements of s		Representation of Continuous time	5				Discre	te Tin	e Fou	rier Tı	ansfo	rm (D	TFT)	– Re	eaion	of cor	nvera	ence	of fini	e dura	tion

		Classification of Signals and Systems	Analysis of Continuous Time Signals	Analysis of LTI CT System	Analysis of DT Signals and Systems	Analysis of LTI DT System using Z-Transform
Durati	on (hour)	12	12	12	12	12
	SLO-1	Introduction to signals and systems	Introduction to Fourier series	System modeling	Representation of sequences	Z transform – introduction
S-1	SLO-2	Requirements of signal and system analysis in communication	Representation of Continuous time Periodic signals	Description of differential equations		Region of convergence of finite duration sequences-properties.
S-2	SLO-1	Continuous time signals (CT signals)	Fourier series: Trigonometric representation	Solution of Differential equation using classical method	DTFT of standard signals	Unilateral and bilateral z transforms
3-2		Discrete time signals (DT signals)	Fourier series: Trigonometric representation	Differential equation: Zero state response	Properties of DTFT	Properties of z transform
S-3	SLO-1	Representation of signals: Step, Ramp, Pulse, Impulse	Fourier series: Cosine representation	Differential equation: Zero Input response	Problems on Properties of DTFT	Practice problems
3-3	SLO-2	Representation of signals: Sinusoidal, Exponential	Fourier series: Cosine representation	Total Response using classical method	Inverse DTFT	Practice problems
	SLO-1	Basic operation on the signals	Symmetry conditions	Impulse response	Impulse response of a system with DTFT	Relation between DTFT and Z transform
S-4	SLO-2	Problems on signal operations	Properties of Continuous time Fourier series	Step response	Frequency response of a system with DTFT	Practice problems

S-5	SLO-1	Classification of CT and DT signals: Periodic & Aperiodic signals.	Practice problems on Fourier series	Frequency response	Step response	condition for causality in Z domain- Problems
5-5	SLO-2	Classification of CT and DT signals: Deterministic & Random signals.	Practice problems on Fourier series	Practice problems on solution of differential equation	Practice problems	condition for stability in Z domain-Problems
S-6	SLO-1	Energy signal	Gibb's Phenomenon	Convolution integral	Solution of linear constant coefficient difference equations	Inverse Z transform
	SLO-2	Power signal	Parseval's relation for power signals	Properties of convolution	Problems with and without Initial conditions	Power series expansion
S-7		Even & Odd signals	Power density spectrum,		Solution of difference equations using classical method	Inverse Z transform with Partial fraction
3-1	SLO-2	Even & Odd signals	Frequency spectrum.	Practice Problems	Zero input resp <mark>onse , Zero s</mark> tate response, Total response	Inverse Z transform with Partial fraction
	SLO-1	CT systems and DT systems	Fourier transform: Introduction	Analysis using Laplace transform	Practice problems	Residue method
S-8	SLO-2	Classification of systems: Static & Dynamic	Representation of Continuous time signals	ROC and Convergence of Laplace Transform	Practice problems	Convolution method
S-9	SLO-1	Superposition theorem	Properties of Continuous time Fourier transform	Properties of Laplace transform	DFT and IDFT	Analysis and characterization of DT system using Z-transform
5-9	SLO-2	Linear & Nonlinear system	Properties of Continuous time Fourier transform	Problems on properties of Laplace transform	Properties of DFT	Analysis and characterization of DT system using Z-transform
0.40	SLO-1	Time-variant & Time-invariant system	Parseval's relation for energy signals	Inverse Laplace transform	Practice problems	Practice problems
S-10	SLO-2	Time-invariant system	Energy density spectrum	Problems	Convolution sum	Practice problems
S-11	SLO-1	Causal system	Practice problems on Fourier Transform	Analysis of LTI system using Laplace transform	Convolution properties	Realization of Discrete time system- Direct form I, Direct Form II
3-11	SLO-2	Noncausal system	Practice problems on Fourier Transform	Analysis LTI system using Laplace transform-Problems	Linear Convolution,-Tabulation method, Matrix method	Realization of Discrete time system- Parallel and cascade form
S-12	SLO-1	Stable & Unstable,LTI System	Practice problems on properties of Fourier Transform	transionii		Practice problems
5-12	SLO-2	Unstable, LTI System	Practice problems on properties of Fourier Transform		Circular convolution-concentric circle method, matrix method	Practice problems

Lograina	1.	Alan V Oppenheim, Rona <mark>ld W. Sch</mark> afer Signals & Systems, 2 <sup>nd</sup> ed., Pearson Education, 2015
Learning Resources	2.	P.Ramakrishna Rao, Shankar Prakriya, Signals & Systems, 2nd ed., McGraw Hill Education, 2015
	3.	Simon Haykin, Barry Van Veen, Signals and Systems, 2 <sup>nd</sup> ed., John Wiley & Sons Inc., 2007

- Lathi B.P, Linear Systems & Signals, 2<sup>nd</sup> ed., Oxford Press, 2009
   John G. Proakis, Manolakis, Digital Signal Processing, Principles, Algorithms and Applications, 4<sup>th</sup> ed., Pearson Education, 2007

	Dlaam'a			Conti	inuous Learning Ass	essment (50% weigl		Final Evamination	(E00/ waightaga)				
	Bloom's Level of Thinking	CLA –	1 (10%)	CLA –	2 (15%)	CLA – 3	3 (15%)	CLA – 4	4 (10%)#	Final Examination (50% weightage)			
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice		
Level 1	Remember Understand	40 %		30 %	-	30 %	-	30 %	-	30%	-		
Level 2	Apply Analyze	40 %		40 %	-	40 %	-	40 %	-	40%	-		
Level 3	Evaluate Create	20 %	-	30 %	-	30 %		30 %	-	30%	-		
Total		10	0 %	10	0 %	100	) %	10	0 %	10	0 %		

<sup>#</sup>CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	



Cou		18ECC105T Course Name	ELECTROMAGNETICS AND TRANSMISSION	ONLINES	Course atego		С				Pro	fessio	nal Co	ore					T 0	P 0	C 3
Co	equisite urses	18EES101J, 18PYB101J Department Electronics and C	Co-requisite Courses  Mil Data Book	/ Codes/Standards		ogres	es	18ECC20													
Course	Offering	Department  Electronics and C	Data Book	/ Codes/Standards	Clai	K S T A	ible, i	3 . 450-20	00												
Course	Learning	Rationale (CLR): The purpose of lea	rning this course is to:	THE REAL PROPERTY.	L	earnin	ng					Progr	am Le	arning	Outco	omes	(PLO)	)			
CLR-1	: Gain i	knowledge on the basic concepts and ins	ig <mark>hts of Electri</mark> c field		1	2	3	1	2	3	4	5 (	6 7	8	9	10	11	12	13	14	15
CLR-2: Gain knowledge on the basic concepts and insights of Magnetic field and Emphasize the significance of Maxwell's equations.  CLR-3: Interpret the wave propagation in guided waveguide.  CLR-4: Acquire the fundamental knowledge on Transmission Line Theory.									PSO-1: Professional   Achievement	PSO – 2: Project Management Techniques	R r r r PSO - 3: Analyze & Research										
CLO-6			enerated using Maxwell's equations and how T int to another with minimum losses over a wide		2	60	60	М	Н	24	-	-	-   -	-	-	-	-	L	-	-	Н
Duratio	on (hour)	Electrostatics	Magnetostatics and Maxwells Equations 9	Electromagnetic Waves a	ınd Wa	avegui	ides	) <sup>†</sup>	ransm	issior	n Line	Theory	1		Tra				Calcula atchin	ator and	t t
S-1		Introduction	Energy density in electrostatic field	Introduction				Transmiss							roduc						
	SLO-2	Rectangular co-ordinate	Problem discussion.	Waves in general				Transmiss	sion lin	e par	amete	T				nart In			,,		
S-2		Cylindrical & Spherical Co-ordinate	Biot savart law-Magnetic field intensity due to Infinite line charge	Plane wave in lossiess die	I ransmission line equivalent circuit Input impedance calcu						nt, Standing wave ratio alculation in smith chart										
	SLO-2	Review of vector calculus	H- due finite and semi finite line charge	Plane wave in free space	1			Explanation	on					Pr	actice	proble	ems.				
	SLO-1	Coulomb's Law and field intensity	Ampere's circuital law& application: Infinite line current	Plane wave in good condu	ctor	Grd.		Transmiss	sion <mark>lin</mark>	e equ	<mark>iation</mark> d	derivat	ion	Si	ngle s	tub ma	atching	g Intr	oducti	on	
S-3	SLO-2 Problem based on coulomb's law Infinite Sheet current Problems based on plane waves in lossless, free space and good conductor Problem discussion.																				

Rectangular waveguide

Infinitely long coaxial Transmission line

Problem based on ACL.

Magnetic flux density

Electric field due to continuous charge

distribution-.Concept

SLO-2 Derivation of E due Infinite Line charge

Electric field due to sheet charge

SLO-1

SLO-1

S-4

S-5

lossless, free space and good conductor

Rectangular waveguide-Problems

Transverse Electric (TE) mode

Transmission line characteristics: lossless

line

Distortionless line.

Input impedance derivation

Problems solving in smith chart

Problems solving in smith chart

transformer

Impedance matching using Quarter wave

	SLO-2	Problem based on sheet charge	Problem based on magnetic field and flux.	Transverse Electric (TE) mode-problems	Problems for input impedance calculation.	Problems.
S-6	SLO-1	Electric field due to volume charge	Maxwell's equation for static field	Transverse Electric (TE) mode	Standing wave ratio	Single stub tuner
3-0	SLO-2	Electric flux density	Faraday's law	Transverse Electric (TE) mode-Problems	Calculation of standing wave ratio.	Problem discussion
S-7	SLO-1	Gauss law application-point charge	Transformer EMF	Wave propagation in guide	Reflection coefficient	Slotted Line (Impedance Measurement)
3-1	SLO-2	Electric flux due infinite line charge	Motional EMF	Problem discussion	Problem discussion.	Problem discussion
S-8	SLO-1	Electric flux due sheet charge	Displacement current.	Power Transmission	Shorted line, open circuited line	Transmission Lines as circuit Elements
3-0	SLO-2	Electric flux due coaxial cable	Maxwell's equation in time varying field	Calculation of Pavg and Ptotal	Matched line	Problem discussion
S-9	SLO-1	Relation between E&V	Time varying potential concepts	Power attenuation	Power calculations	Additional smith chart problem solving.
3-9	SLO-2	Electric dipole and flux lines	Time varying potential derivation.	Calculation of αTE and αTE	Problem discussion.	Additional smith chart problem solving.

Learning Resources	1. Matthew N. O. Sadiku., S. V. Kulkarni, Elements of Electromagnetics, 6 <sup>th</sup> ed., Oxford University Press, 2015 2. G. S. N. Raju, Electromagnetic Field Theory and Transmission Lines, Pearson Education, 2006 3. Nannapaneni Narayana Rao, Principles of Engineering Electromagnetics,6 <sup>th</sup> ed., Pearson Education, 2016	4. William H. Hayt,Jr., John A.Buck., Engineering Electromagnetics, 8th ed., Tata McGraw-Hill 2012 5. John D.Ryder, Networks, Lines and Fields, PHI, 2009
	3. Nannaparieni Narayana Rao, P <mark>rincipies o</mark> i Engineering Electromagnetics,o" ed., Pearson Education, 2016	

Learning Assess	sment												
	Bloom's		Continuous Learning Assessment (50% weightage)								n /E00/ woightaga)		
	Level of Thinking	CLA –	CLA – 1 (10%)		CLA – 2 (15%)		3 (15%)	CLA – 4	1 (1 <mark>0%</mark> )#	Final Examination (50% weightage)			
	Level of Thirtking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice		
Level 1	Remember Understand	40 %	531	30 %		30 %		30 %	-	30%	-		
Level 2	Apply Analyze	40 %		40 %		40 %		40 %	-	40%	-		
Level 3	Evaluate Create	20 %		30 %		30 %	TER S	30 %	-	30%	-		
	Total	10	0 %	10	0 %	10	0 %	10	0 %	10	00 %		

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Cour Cod		18ECC201J	Course Name		ANALOG E	LECTRONIC CIRCUITS		Cours Catego		С				ı	Profes	siona	al Cor	9				L 1	- P	C 4
Co	equisite urses	18ECC102J			Co-requisite Courses	1 <mark>8ECC202J</mark>			rogres Cours		18EC	<b>Ξ201</b> J	1											
Course	Offering	Department	Electro	nics and Con	nmunication Engineer	ng Data Book / C	odes/Standards	Nil																
Course	Learning	Rationale (CLR	): The pur	pose of learn	ing this course is to:	1256	TI-M		.earnir	ng					Pr	ograr	n Lea	ning Ou	tcome	s (PL	0)			
CLR-1:					ol <mark>ifier circuits fo</mark> r a give			1	2	3		2	3	4	5	6	7	8 9	10	11	12	13	14	15
CLR-2:					<mark>T amplifier c</mark> ircuits for						1			5			ility							
CLR-3: Understand the effects of negative feedback on amplifier circuits, and analyze the different RC at to determine the frequency of oscillation							d LC oscillator circuits	of Thinking (Bloom)	cy (%)	nt (%)	2	Dâns	nent	Research	0		Environment & Sustainability	Work	5	nce		<del>-</del>	hniques	-
CLR-4:								g (E	ienc	mel	1	S S	op ndo	٦,	age	e	Sus	Ē		⊒a	lg.	io	t de	ze &
CLR-5:	Understand how matched transister characteristics are used in the IC design and to be able to de							hinkin	Expected Proficiency (%)	Expected Attainment (%)	o de charles de la companya de la co	Problem Analysis	Development	Design, F	Modern Tool Usage	Society & Culture	ent & 9	Ethics Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO-1: Professional Achievement	2: Project ement Tech	Ang
CLR-6:	Gain	hands-on experie	ence to put th	eor <mark>etical co</mark> nd	cepts learned in the co	ourse to practice.		of T	ted	ted		D W	Design & [	Analysis,	Į.	⊗ >-	E L	<u> </u>	Z   E	Σ	guc	PSO-1: Profe Achievement	– 2:	PSO – 3: . Research
-					- Marie 1	# MINESTON		evel	bec	bec	3.	ald d	Sign	alys	lage	ciet	virc	Ethics		)ec	e Lc	Ģ ė	PSO-	00- 3868
Course		Outcomes (CLC			urse, learners will be a		A second	Le	ŭ	ы	ú	ة ا	P	A	ĕ	လွ	ᇤ	击	ြို	4	===	PS S	S 8	<u>. 요 &amp;</u>
CLO-1 :	ampli	ons, and to Analyze the free mine the bandwidth of the	circuit.	2,3	70	70	I	. M	1 H	6	-	-	-		-	-	-	-	-	-				
CLO-2	CLO-2: Analyze and design MOSFET amplifier circuits to meet certain specifications, and to Analyze the amplifier circuits, taking into account various circuit capacitors, to determine the bandwidth of the						circuit.	2,3	70	70	I		1 H	13	-	-	-		-	-	-	-	-	_
CLO-3 :	circui	ts to meet certair	n specification	S.		uits and oscillator circuits t	Marie Land	2,3	70	70	I	. 1	1 H	ŀ	-	-	-		-	-	-	-	-	-
CLO-4 :	type o	of power amplifie	r			maximum possible convers		2,3	70	70	** I	. M	1 H	3	-	-	-	-   -	-	-	-	-	-	-
CLO-5:	Desig	n the basic circu	it building blo	c <mark>ks that a</mark> re u	sed in the design of I	C amplifiers, namely curren	t mirrors and sources	2,3	70	70	I	. N	1 H	-	-	-	-		-	-	-	-	-	-
CLO-6	Analy	ze and design aı	nalog electron	i <mark>c circuits</mark> usi	ng discrete componer boratory with theoretic	nts, and take measurement	of various analog	3	90	80			Н	-	М	-	-	- N	-	-	М	Н	L	-
		В	BJT Amplifiers		L FE	Γ Amplifiers	Feedback amplifie	s & O	scillate	ors		Oscil	ators	& Pow	er Am	nlifie	rs	IC	Riasin	n & A	mplifi	ers with	n Activ	e Load
Duratio	n (hour)		15			15	15		oomat	0.0		Coom	utoro .	15	01711	.p.iiio		- 10	Diaoiii	9 4 7 1	1		171001	<u>5                                    </u>
0.4	SLO-1	Overview of DC	analysis of B	JT circ <mark>uits</mark>	Overview of FET Do	C circuit analysis	Basic feedback conce feedback structure	pts, ge	eneral		Crysta	al Osc	illators									Cascoo t source		ent
S-1	SLO-2	Overview of BJ	T models		Problem solving         Properties of negative feedback         Problem solving         Multi-transistor currence						urren	t sourc	e Prob	lem										
S-2								Feedback Topologies: Voltage-Series & Current-Series feedback connections								rces:	2-trans	istor N	10SFE					
	SLO-2	Problem solving			Problem solving		Problem solving				Proble	em sol	ving					Prob	lem so	lving				
S-3	SLO-1 AC analysis of Common-Emitter BJT amplifier config. using hybrid-π model AC analysis of Common-Source MOSFET amplifier configuration					Feedback Topologies. Current-Shunt feedba				Powe types	Amp.	l <mark>ifier</mark> s:	Defini	tions a	and a	mplifi					ent			
		Problem solving	7		Problem solving	Problem solving				Q poi	nt plac	emen	!				Problem solving							
S 4-5	SLO-1 Lab 1: Learning to design amplifier and Lab 4: Design & analyze differential amplifier				Lab 7: Design and and oscillators	alyze l	RC		Lab 1	o: BJT	& FE	T Curi	ent S	ource	s		13: De lifier w			nalyze oad	differe	ntial		
S-6					AC analysis of Com	mon-Gate MOSFET	Practical Feedback Ar	nplifie	r Circu						circuit	with								

		amplifier configuration using hybrid-π model	amplifier configuration			active load
	SLO-2	Problem solving	Problem solving	Problem solving	Heat sink	Problem solving
S-7	SLO-1	AC analysis of Common-Collector BJT amplifier config. using hybrid-π model	AC analysis of Common-Drain MOSFET amplifier configuration	Oscillators: Principles of Oscillation	Class A amplifier	Analysis of CS FET amplifier circuit with active load
Ī	SLO-2	Problem solving	Problem solving	Types of Oscillators	Problem solving	Problem solving
S-8	SLO-1	Multi-stage amplifier configurations: CE - CE, CE - CC amplifiers	BiFET amplifier configuration	Audio Frequency Oscillators: RC Phase- Shift Oscillator	Class B and Class AB push-pull amplifiers	DC and small-signal analysis of basic BJT differential pairs
Ī	SLO-2	Problem solving	Problem solving	Problem solving	Problem solving	Problem solving
S		Lab 2: Design and analyze BJT amplifier	Lab 5: Design and analyze negative feedback	Lab 8: Design and analyze LC	Lab 11: Desig <mark>n and analyze</mark> BJT CE	Lab 14: Model Practical Examination
9-10	SLO-2	configurations	amplifier configurations	oscillators	amplifier with active load	Lab 14. Modert ractical Examination
S-11	SLO-1	Multi-stage amplifier configurations: CE - CB, and CC - CC amplifiers	Low Frequency response analysis of a basic FET CS amplifier	Audio Frequency Oscillators: Wein Bridge Oscillator	Class C amplifiers	DC and small-signal analysis of basic FET differential pairs
	SLO-2	Problem solving	Problem Solving	Problem Solving	Problem solving	Problem solving
S-12	SLO-1	Low Frequency response analysis of a basic BJT CE amplifier	High Frequency response analysis of a basic FET CS amplifier	Radio Frequency Oscillators: Hartley Oscillator	Class D and Class E amplifiers	Analysis of BJT differential amplifier with active load
	SLO-2	Problem Solving	Problem Solving	Problem solving	Amplifier distortions	Problem solving
S-13	SLO-1	High Frequency response analysis of a basic BJT CE amplifier	Design problems in MOSFET amplifier configurations	Radio Frequency Oscillators: Colpitts & Clapp Oscillators	IC Biasing & Amplifiers with Active Load: BJT current sources: 2- & 3-transistor current sources	Analysis of FET differential amplifier with active load
	SLO-2	Problem Solving	Operational voltage levels	Problem solving	Problem solving	Problem solving
S	SLO-1	Lab 3: Design and analyze multistage	Lab 6: Design and analyze MOSFET amplifier	Lab 9: Classes of power amplifier	Lab 12: Design and analyze FET CS	Lab 15: End Semester Practical
14-15		amplifier configurations	configurations	(efficiency calculation)	amplifier with active load	Examination

	1.	David A. Bell, Electronic Devices and Circuits, 5 <sup>th</sup> ed., Oxford University Press, 2015
Learning	2.	Donald Neamen, Electr <mark>onic Circu</mark> its: Analysis and Design, 3 <sup>rd</sup> ed., McGraw-Hill Education, 2011
Resources	3.	Muhammad Rashid, Microelectronic Circuits: Analysis & Design, 2 <sup>nd</sup> ed., Cengage Learning, 2010
	4.	Adel S. Sedra, Kenneth C. Smith, Microelectronic Circuits: Theory and Applications, OUP, 2014

- 5. Robert L. Boylestad, Louis Nashelsky, Electronic Devices and Circuit Theory, 11th ed., Pearson Education, 2013
- 6. Albert P. Malvino, David J. Bates, Electronic Principles, 8th ed., Tata McGraw Hill, 2015

Learning Assessr	ment										
	Bloom's		(Carl.)	Cont	inuous Learning Asse	essment (50% weig	htage)			Final Evamination	n (50% weightage)
		CLA –	1 (10%)	CLA -	2 (15%)	CLA –	3 (15%)	CLA –	4 <mark>(10%)#</mark>	Filiai Examination	i (50% weightage)
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
r. Level 1	Remember Understand	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%
Level 2	Apply Analyze	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
Level 3	Evaluate Create	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
	Total	10	0 %	10	00 %	10	0 %	10	0 %	10	0 %

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Cour		18ECC202J Course Name	LINEAR IN	ITEGRATED CIRCUITS	3	Cou Cate		С					I	Profes	siona	al Cor	е					L T	P 2	C 4
Co	equisite urses	18ECC102J	Co-requisite Courses	18ECC201J			Progre Cour		Nil															
Course	Offering	Department Electronics and Comi	munication Engineer	ing Data Book	/ Codes/Standards	N	il .																	
						H																		
Course	Learning	Rationale (CLR): The purpose of learning	g t <mark>his course i</mark> s to:	1000	H. Commercial Commerci		Learni	ng						Pro	ogran	n Lea	rning	Outco	omes	(PLC	))			
CLR-1		the basic principles, configurations and prac		o-amp		1	2	3	1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CLR-2		rstand the various linear and non-linear a <mark>ppli</mark>					Т.		٠	f.,,			H2			iit								
CLR-3		rstand the operation and analysis of op <mark>-amp</mark>				l (E	(%)	(%		e	٠.	±	ear			лар		논		a			nes	
CLR-4		fy the active filter types, filter respons <mark>e chara</mark>					ें	int (		edc	×	ner	Res	Φ		stail		Wo		ance		ज्ञ	ij	∞ర
CLR-5		knowledge on data converter termin <mark>ology, its</mark> D/A conversions.	performance param	neters, and various circu	it arrangements for A/D	I of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)		Engineering Knowledge	Problem Analysis	Design & Development	Design, Res <mark>earch</mark>	Modern Tool Usage	Society & Culture	Environment & Sustainability		ndividual & Team Work	Ę	Finance	Life Long Learning	SO-1: Professional chievement	PSO – 2: Project Management Techniques	– 3: Analyze arch
CLR-6	Gain I	hands-on experience to put theor <mark>etical con</mark> ce	epts learned in the co	ourse to practice.	A COLUMN THE	ig	Po	Atta		y Br	ınal	Dev	Des	00	C	ent		& T	Satic	)t. 8	Lea	rofe ent	Proj ent	Ana
				-100	Section of the second	Į.	6	ted		eri	m	∞	is, l	Ľ	∞ >	JIII		ual	Ĭ.	Ĕ	пg	E F	2:    em	က် ဉ်
Course	Learning	Outcomes (CLO): At the end of this cour	rea learners will be	able to:	1.67	evel	bec	pec		gine	plde	sign	Analysis,	der	ciet	viro	Ethics	ivid	Communication	Project Mgt. &	2	PSO-1: Profe Achievement	SO – lanag	PSO – 3: / Research
		, ,					Ĭ X		100	En		De	Ani	₩ W	So	En	Eth	pul	ပိ	Pro	Life	PS Act	PS Ma	S &
CLO-1		the DC and AC characteristics <mark>of operat</mark> ional				3		70		Н	М	- 1	-	-	-	-	-	-	-	-	-	-	-	
CLO-2		date and design the linear and <mark>non-linea</mark> r app				3	85	75			М	Н		-	-	-	-	-	-	-	-	-	-	-
CLO-3		in and compare the working o <mark>f multivib</mark> rators			al purpose opamp	3					М	Н		-	-	-	-	-	-	-	-	-	-	-
CLO-4		ify and comprehend the worki <mark>ng princi</mark> ple of				3		80			M	Н	-	-	-	-	-	-	-	-	-	-	-	-
CLO-5	A l	ate the function of application specific ICs su				3	85	75			М	Н	-	-	-	-	-	-	-	-	-	М	-	Н
CLO-6		rze and design electronic circu <mark>its and s</mark> ystem are experimental results in the <mark>laborato</mark> ry wit			i various arialog circuits to	3	85	75	146	-	Μ	Н	-	М	-	-	-	М	-	-	-	Η	L	-
	comp	are experimental results in the laboratory will	in theoretical analysis			-		-																
Duratio	n (hour)	15	F .	15	15								15								15			
S-1		Op-amp symbol, terminals, packages	Basic op-amp circuinverting voltage an		Waveform Generators: Si Generators - Design	ne-w	ave		Filter Activ			rison i	betwe	en P	assiv	<mark>e a</mark> no		gital to pecific			onve	rsion: ı	DAC	
3-1	SI O-2	Op-amp-Specifications	Voltage follower	ipiillers	Implementation & Solving	n nro	hlems					.s Desi	an				- 1-	olving						
		Block diagram Representation of op-amp		averaging amplifiers,	Square Wave generators-							ations						eighte			DAC			-
S-2	SLO-2	Ideal op-amp & practical op-amp - Open Ioop & closed loop configurations	AC amplifiers	a averaging ampliners,	Implementation & Solving							& Sol		oroble	ms			olving			Dito			
	SLO-1	DC performance characteristics of op-amp	Linear Applications.  Amplifiers	: Instrumentation	Triangle wave generators	S	711	W	Desi	gn of	HPF	& So	lving	proble	ems		R-	2R La	ndder	DAC				
S-3	SLO-2	Solving Problems	plifiers, Solving	Saw-tooth Wave generate	ors.			Desi	gn of	BPF	& Solv	v <mark>ing</mark> p	roble	ms		Sc	olving	probl	ems					
S 4-5					Lab 7: Waveform generators: using op-			p-	Lab Band			of LF	PF, H	PF, B	PF ai	nd	La	Lab 13: Flash Type ADC						
		AC performance characteristics of op-amp	V-to-I Converters		amp & 555 Timer IC 555 Timer: Circuit sch	omet	ic					iters I Reje	ct Fil	tore			In	verted	R-2F	2 l ad	der D	AC.		
S-6		Solving Problems	I-to-V converters		Operation and its applicat		10						ot I II	.010				onolith			עטו ט	,10		
S-7		Frequency response						s applications Solving problems  Onostable operation State Variable Filters – All Pass Filters				ers,	Analog to Digital conversion: ADC											
3-1	SI O-2	Frequency response		Applications & Solving problems Solving problems Solving problems Solving problems																				
	JLU-2	i roquerioy response	Integrators		Applications & Solving problems   Solving problems   Solving problems																			

S-8	SLO-1	Frequency compensation	Non-linear Applications: Precision Rectifiers	IC 555 Timer: Astable operation	Switched Capacitor Filters.	Ramp Type ADC
3-0	SLO-2	Frequency compensation	Wave Shaping Circuits (Clipper and Clampers)	Applications & Solving problems	Solving problems	Solving problems
S	SLO-1	Lab 2: Integrators and Differentiators	Lab 5: Wave shaping circuits	Lab 8: Waveform generators: using op-	Lab 11: IC Voltage regulators	Lab 14: Simulation experiments using EDA
9-10	SLO-2	Lab 2. Integratore and Differentiatore	Lab o. Wave draping circuite	amp & 555 Timer	Lab 11: 10 Voltage Togalatore	tools
S-11	SLO-1	Basic op-amp internal schematic	Log and Antilog Amplifiers,	PLL: Operation of the Basic PLL	Voltage Regulators: Basics of Voltage Regulator	Successive Approximation ADC
3-11	SLO-2	operations of blocks	Analog voltage multiplier circuit and its applications,	Glosed loop analysis of PLI	Specifications and characteristic parameters	Solving problems
C 12	SLO-1	Basic op-amp internal schematic	Operational Trans-Conductance Amplifier (OTA)	Voltage Controlled Oscillator	Linear Voltage Regulators using Op-amp,	Dual Slope ADC
S-12	SLO-2	operations of blocks	Comparators : operation		IC Regulators (78xx, 79 <mark>xx, LM 317</mark> , LM 337, 723),	Flash Type ADC,
0.40	SLO-1	Review of data sheet of an op-amp.	Comparators applications	PLL applications	Switching Regulators -operation	Solving problems on Flash Type ADC,
S-13	SLO-2	Solving Problems	Sample and Hold circuit.	Solving problems	Types	Monolithic ADC
S 14-15	SLO-1 SLO-2	Lab 3: Rectifiers	Lab 6: Waveform generators: using op- amp & 555 Timer	Lab 9: Design of LPF, HPF, BPF and Band Reject Filters	Lab 12: R-2R ladder DAC	Lab 15: Simulation experiments using EDA tools

۱		1. Ramakant A. Gayakwad. Op-Amps and Linear Integrated Circuits, 4th ed., Prentice Hall, 2000	LADONA
			David A
		1.2 David A. Bell, Operational Amplitiers and Linear ICs, 3 <sup>rd</sup> ed., OUP, 2013	
۱		8	David La
۱	Learning	1.3 Roy Choudhury Shail Jain Linear Integrated Circuits, 4th ed. New Age International Publishers, 2014	
۱			Muhamn
	Resources	4. Robert F. Coughlin, Frederick F. Driscoll, Operational-Amplifiers and Linear Integrated Circuits, 6th ed.,	2004
۱		Pronting Hall 2001	2004

5. Sergio Franco, Design with operational amplifier and analog integrated circuits, McGraw Hill, 1997

- 6. LABORATORY MANUAL, Department of ECE, SRM University
- 7. David A Bell, Laboratory Manual for Operational Amplifiers & Linear ICs, 2nd ed., D.A. Bell, 2001
- 8. David La Lond, Experiments in Principles of Electronic Devices and Circuits, Delmar Publishers, 1993
- 9. Muhammed H Rashid, Introduction to PSpice using OrCAD for circuits and electronics, 3rd ed., Pearson, 2004
- 10. L. K. Maheshwari, M. M. S. Anand, Laboratory Experiments and PSPICE Simulations in Analog Electronics, PHI, 2006

Learning Assessn	nent										
	Bloom's		100	Conti	nuous Learning Ass	essment (50% weig	htage)			Final Evamination	n (50% weightage)
	Level of Thinking	CLA –	1 (10%)	CLA –	2 (15%)	CLA –	3 (15%)	CLA – 4	4 ( <mark>10%)#</mark>		ii (50% weightage)
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%
Level I	Understand	2070	2070	10/0	1378	1370	1370	1070	1370	1370	1370
Level 2	Apply	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
Level 2	Analyze	2070	2070	2070	2070	2070	2070	2070	2070	2070	2070
Level 3	Evaluate	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
Level 3	Create	1070	1076	1370	1370	13/6	1370	13/0	1370	1570	1370
	Total	10	0 %	10	0 %	10	0 %	10	0 %	10	00 %

<sup>#</sup> CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	1. Mr. Manikandan AVM, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	2. Dr. M. Sangeetha, SRMIST

## **ACADEMIC CURRICULA**

**Professional Core Courses** 

## ELECTRONICS AND COMMUNICATION ENGINEERING

Regulations - 2018



## SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956) Kattankulathur, Kancheepuram, Tamil Nadu, India

Course Code	18EC C203J	Course	М	· ·	CONTROLLER AND INTERFACING	_	ourse	- (	2				Pro	ofess	ional	Core					L -	ГР	С
Course Cous	1020 02000	Name		TECH	HNIQUES	Ca	ategor	У							- Ionai						3 (	J 2	4
Dre-requis	ite Courses	18ECC	1031	Co-requisite Courses	Nil		Proc	roccive	e Cours	00						18EC	`E20/	1   1	BECE2	205 1			
Course Offering Do				Communication Engineering	Data Book / Codes/Standards		FIU	I CSSIVE	Cours	<b>C</b> 3					Nil	TOLC	,LZU4	10, 10	LULZ	2000			
Course Cherning Di	эрагинон	Lioution	100 4114 0	on manioation Engineering	Bata Book / Codes/Citalidards																		-
Course Learning R	ationale (CLR):	The purpose	of learnin	g this course is to:	5 Printer	L	earnir	ng					Pi	rogra	m Lea	arning	Outo	comes	s (PLC	O)			
CLR-1: Undersi	and basic architec	ture of Intel 80	36 microp	processor and Intel 8051 Micro	controller	1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
and per CLR-3: Interfac CLR-4: Use the CLR-5: Undersi CLR-6: Provide  Course Learning C	ipheral chips e a microprocessor computer to write land the hardware, strong foundation Outcomes (CLO):	r / microcontrol and assemble / software inter for designing re At the end of	ler to externation of the second seco	ernal I/O devices and perform d also run them by downloadin I their applications, and as wel applications using microproce se, learners will be able to:	essors and microcontrollers.	Level of Thinking (Bloom)	Expected Proficiency (%)	S Expected Attainment (%)	Engineering Knowledge	Problen	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO-1: Professional Achievement	PSO – 2: Project Management Techniques	PSO – 3: Analyze & Research
				icroprocessor based personal	computer system	1	60		-	Н	-	-	L	-	-	-	-	-	-		-	-	-
				oprocessor. / microcontroller	COTTA STRATEGIC VALLE	2	60	70	М	-	-	-		-	-	-	-	-		М	-		<u> </u>
					e target microprocessor / microcontroller	3	60	70	-		Н	-	Н	-	-	-	-	-	-		-		L
				cessors & Microcontrollers.		1	60	70	-	М	-	-		-	-	-	-	-	-	Н	-		<u> </u>
	e their practical kno				devices the second of the second	3	60	70	-		М	-	Н	-	-	-	-	Н	-		-		Н
CLO-6: Design.	interface and proc	rom momoni o	hine and	various paripharal chine with r	microprocessor / microcontroller	3	60	70			M	_	Н	_		_	_			Н	. 1	-	M

Duratio	n (hour)	Intel 8086 – Architectu <mark>re, Signals</mark> and Features	Programming with Intel 8086	8086 Interfacing with Memory and Programmable Devices	Intel 8051 – Architecture and Programming	Interfacing of 8051
		15	15	15	15	15
S-1	SLO-1	Introduction: History of computers, Block diagram of a microcomputer	Addressing modes of 8086	Semiconductor memory interfacing	Introduction: Differences between microprocessor and microcontroller	8051 parallel ports, and
3-1	SLO-2	Intel 80x86 evolutions		Dynamic RAM interfacing	Intel's family of 8-bit microcontrollers, and feature of 8051 microcontroller	its programming
S-2	SLO-1	Features of 8086 microprocessor	Instruction Set of 8086: Data Transfer Instructions	Programmable Peripheral Interface 8255	Architecture of 80 <mark>51</mark>	8051 timers, and
3-2	SLO-2	Register organization of 8086	Example programs	Interfacing 8255 with 8086 and programming		its programming
S-3	SLO-1	Architecture of 8086	Data Conversion Instructions, Arithmetic Instructions	Interfacing ADC with 8086 and programming	Signal descriptions of 8051	8051 interrupts, and
S-S	SLO-2		Example programs	Interfacing DAC with 8086 and programming		its programming
S-4,5		Lab-1: (a) Learning to Program with 8086 processor kit; Learning the hardware features of the 8086 processor kit	Lab-4: General Purpose Programming in 8086	Lab-7: Interfacing DAC / ADC with 8086 / 8051	Lab-10: Programming timer / counter in 8086 / 8051	Lab-13: Simulation of 8051 using Keil Software

S-6	SLO-1	Instruction queue and pipelining	Logical instructions and Processor control instructions	Stepper Motor interfacing	Register set of 8051	8051 serial port, and
	SLO-2	Segmentation of memory used with 8086	Example programs		Operational features of 8051	its programming
0.7	SLO-1	Methods of generating physical address in 8086		Programmable Interval Timer 8254	Memory and I/O addressing by 8051	Interfacing program memory with 8086
S-7	SLO-2	Pin signals of 8086: Common signals	Example programs	Interfacing 8254 with 8086 and programming	Interrupts and Stack of 8051	Interfacing data memory with 8086
S-8	SLO-1	Minimum mode signals	Branch Instructions	Programmable Interrupt Controller 8259	Addressing modes of 8051	Interfacing input devices: push-button / matrix keypad
S-0	SLO-2	Maximum mode signals	Example programs	Interfacing 8259 with 8086 and programming	0 - 10	Example programs
S-9,10	SLO-1 SLO-2	Lab-2: General Purpose Programing in 8086	Lab-5: Simulation of 8086 using MASM Software / 8086 Emulator	Lab-8: Interfacing DC motor / stepper motor / servo motor with 8086 / 8051	Lab-11: Programming interrupts in 8086 / 8051	Lab-14: Model Practical Exam
0.44	SLO-1	Minimum mode 8086 system <mark>, and</mark>	Assembly Language Programming of 8086	Programmable Keyboard / Display Controller 8279	8051 Instruction Set: Arithmetic and Logical Instructions	Interfacing display devices: LED / 7- segment / LCD displays
S-11	SLO-2	Timings	Assembly Language Programming of 8086	Interfacing 8279 with 8086 and programming	Example Programs	Example programs
C 10	SLO-1	Maximum mode 8086 sy <mark>stem, and</mark>	Stack structure, and	Programmable Communication Interface 8251 USART	Data Transfer Instructions	Interfacing DAC
S-12	SLO-2	Timings	rela <mark>ted</mark> programming	Interfacing 8251 with 8086 and programming	Example Programs	Interfacing ADC
S-13	SLO-1	Intel 8088 Microprocessor: Pins signals and Architecture	Interrupt structure, and	DMA Controller 8257	Boolean Variable Instructions and Branch Instructions	Interfacing DC motor / stepper motor / servo motor
5-13	SLO-2	Differences between 8086 & 8088 microprocessors	related programming	Interfacing 8257 with 8086 and programming	Example Programs	Example programs
S-14,15	SLO-1 SLO-2	Lab-3: General Purpose Programing in 8086	Lab-6: Interfacing 8255 with 8086 / 8051	Lab-9: General Purpose Programming in 8051	Lab-10: Programming serial communication in 8086 / 8051	Lab-15: End-Semester Exam

	1.	K. M. Bhurchandi and A. K. Ray, "Advanced Microprocessors and Peripherals-with ARM and an
		Introduction to Microcontrollers and Interfacing ", Tata McGraw Hill, 3rd edition 2015
Learning	2.	Muhammad Ali Mazidi and Janice GillispieMazidi, "The 8051 - Microcontroller and Embedded
Resources		systems", 7th Edition, Pearson Education, 2011.
	3.	Doughlas.V.Hall, "Microprocessor and Interfacing: Programming and Hardware", 3rd edition,
		McGraw Hill, 2015

- 4. Kenneth.J.Ayala, "8051 Microcontroller Architecture, Programming and Applications", 3rd edition, Thomson, 2007
- 5. Subrataghoshal "8051 Microcontroller Internals Instructions , Programming And Interfacing", 2nd edition Pearson 2010
- 6. Yu-cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086/8088 family-Architecture, programming and design", 2nd edition, Prentice Hall of India, 2007

Learning Assess	sment			Willy Mill	VIV. VOV.	12 6120	DISTRICT OF STREET	ESA.			
	Bloom's	11.11	170	Cont	inuous Learning As	sessment (50% weig	ghtage)			Final Evamination	(E00/ weightegs)
	Level of Thinking	CLA -	· 1 (10%)	CLA –	2 (15%)	CLA –	3 (15%)	CLA – 4	(10%)#	Final Examination	n (50% weightage)
	Level of Thirtking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%
Level 2	Apply	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
Level 2	Analyze	20%	20%	20%	20%	20%	20%	20%	20%	2076	2070
Level 3	Evaluate	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
	Create Total	10	<u> </u> )0 %	100	) %	100	) %	10	<u> </u> 0 %	10	l 0 %

# CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	1. Mr. Manikandan AVM, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	



Course Code 18	ECC204J	Course Name		DIGITAL SIGN	AL PROCESSING		Cours Catego	-	С				Pi	rofess	ional C	Core				l	L T 3 0	P 2	C 4
Pre-requisite	Courses	18ECC	C104T	Co-requisite Courses	Nil		Pro	gressiv	e Cour	ses					18ECE	243J	. 18E0	CE24	!4J, 18	8ECE	245T		
Course Offering Depart	artment	Electroi	nics and Co	mmunicati <mark>on Engineering</mark>	Data Book / Codes/Standards										Nil		,						
Course Learning Rati (CLR):	1116	purpose of learn			SCH M		earnir	g					F	rogra	m Lea	rning	Outco	mes	(PLO	)			
				rsion of analog signals.		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12		14	15
CLR-3 : Design dig CLR-4 : Design IIR CLR-5 : Understan	ital FIR filter of filters using be a sampling ratechniques for	using windowing both direct metho te conversion an r digital conversi	technique a nd and meth nd apply it fo ons, filter d	and frequency sampling meth nod involving conversion of ar or applications like QMF, sub	nalog filter to digital filter	evel of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Sommunication	Project Mgt. & Finance	Fong	OSO-1: Professional Achievement OSO - 2: Project Management	- 4. niqu	⊃SO – 3: Analyze & Research
	the knowledg	ge of sampl <mark>ing ar</mark>	<mark>nd q</mark> uantiza	tion and understand the error	s that arise due to quantization.	1	80	70	H	-	-		-	-	Ŧ	-	-	-	-	-		-	-
				nputation by using FFT algori		1	75	70		М	-	-	-	-	-	-	-	-	-	-	-	-	
		several methods			WALL SHIP FOR THE	3	75	70		М	Н	-	4	-	-	-	-	-	-	-	-	-	Н
		several me <mark>thods</mark>			Make the Wall	3	75	70			Н	-	-	-	-	-	-	-	-	-	-	-	Н
		nultirate DS <mark>P and</mark>			2 10 2 10 2 10 2	1	70	70		М	-		-	-	-	-	-	-	-	-	-	-	- ]
CLO-6: Apply the	concents of d			rate signal processing for rea		2	70	70		М		-	_								М		

Duratio	on (hour)	Signals and Wa <mark>veforms</mark>	Frequency Transformations	FIR Filters	IIR Filters	Multirate signal Processing
Durauc	on (nour)	15	15	15	15	15
S-1	SLO-1	Basic Elements of DSP	Realization of digital filters Direct form of realization		Design of digital IIR filters Comparison of FIR and IIR filters	Introduction to Multirate signal processing
3-1	SLO-2	Advantages and applications of DSP	Cascade form of realization	Causality, its implication Characteristics of practical frequency selective filters	Analog IIR filter design	Decimation
	SLO-1	Continuous Time vs Discrete time signals	Parallel form of realization	Frequency response of symmetric FIR filter	Properties of Butterworth filters	Interpolation
S-2	SLO-2	Continuous valued vs discrete valued signals	Introduction to DFT		Properties of chebyshev filters Comparison of Butterworth and chebyshev filters	Spectrum of interpolated signal
S-3	SLO-1	Concepts of frequency in analog signals	Computation of DFT	Frequency response of symmetric FIR filter	Analog IIR filter design	Sampling rate conversion by a rational factor I/D
3-3	SLO-2	Continuous and discrete time sinusoidal signals	Prop <mark>erties of DFT Perio</mark> dicity, linearity and symmetry properties	N is even	Design of low pass Butterworth filter	Anti-aliasing and anti-imaging filters
S-4	SLO-1 SLO-2	Lab 1 :Generation of basic signals	Lab 7: Linear convolution	Lab 13: Design of digital FIR Low Pass, High Pass filter using rectangular window	Lab 19: Design of analog Butterworth filter	Lab 25: Interpolation
S-5	SLO-1 SLO-2	Lab 2: Unit step, ramp and impulse	Lab 8: Circular convolution	Lab14: Design of digital FIR Band Pass, Band Stop filter using rectangular window	Lab 20: Design of analog Chebyshev filter	Lab 26: Effect of interpolation in frequency domain

Duratio	on (hour)	Signals and Waveforms	Frequency Transformations	FIR Filters	IIR Filters	Multirate signal Processing
Duranc	on (nour)	15	15	15	15	15
S-6	SLO-1	Sampling of analog signals Sampling theorem	Circular convolution	Frequency response of anti-symmetric FIR filter	Analog IIR filter design	Polyphase structure of decimator Polyphase decimation using z transform
3-0	SLO-2	Aliasing Quantization of continuous amplitude signals	Matrix method and concentric circle method	N is odd and N is even	Design of low pass Chebyshev filter	Polyphase structure of interpolator Polyphase interpolation using z transform
	SLO-1	Analog to digital conversion Sample and hold,	Efficient Computation of the DFT	Design of FIR filters Fourier series method	Design of digital filters Impulse invariance method	Advantages of multirate DSP
S-7	SLO-2	Quantization and coding	Divide and Conquer Approach to Computation of the DFT Using FFT	Need for filter design using window Comparison of various windowing techniques	Design of <mark>digital filters Bili</mark> near transformation	Applications of multirate DSP
S-8	SLO-1	Oversampling A/D converters	N Point DFT Decimation-in-Time FFT Radix-2 FFT Algorithm	Filter Design using windowing technique	Design of digital filters Impulse invariance method	Practical Applications of multirate DSP
5-0	SLO-2	Digital to analog conversion Sample and hold	N Point DFT Decimation-in-Frequency FFT	Rectangular window	Design of digital filters Bilinear transformation	interfacing of digital systems with different sampling rates
S-9	SLO-1 SLO-2	Lab 3: Generation of waveforms	Lab9: Autocorrelation and cross correlation	Lab 15: Design of digital FIR Low Pass and High Pass filter using Hanning and Hamming window	Lab 21: Design of digital Butterworth filter using impulse invariance method	Lab 27: Decimation
S-10	SLO-1 SLO-2	Lab 4: Continuous and discrete time	Lab10: Spectrum analysis using DFT	Lab 16: Design of digital FIR Band Pass and Band Stop filter using Hanning and Hamming window	Lab 22: Design of digital Butterworth filter using bilinear transformation	Lab 28: Effect of decimation in frequency domain
S-11	SLO-1	Oversampling D/A conv <mark>erters</mark>	Radix-2 FFT Algorithm Implementation of FFT Using DIT	Filter Design using windowing technique Hanning window	Design of digital Chebyshev filters	Practical Applications of multirate DSP Sub band coding of speech signals
5-11	SLO-2	Quantization noise	Implementation of FFT Using DIF	Filter Design using windowing technique Hamming window	Impulse invariance method	Filter banks Analysis filter bank
S-12	SLO-1	Errors due to truncation	IDFT	Filter Design using windowing technique	Design of digital Chebyshev filters	Synthesis filter bank
3-12	SLO-2	Probability of error	Using DIT FFT	Black mann window	Bilinear transformation	Subband coding filterbank
0.42	SLO-1	Errors due to rounding	IDFT	Design of FIR filters	Frequency transformation in analog domain	Quadrature Mirror Filter
S-13	SLO-2	Probability of error	Using DIF FFT	Frequency sampling method	Frequency transformation in digital domain	Alias free filter bank
S-14	SLO-1 SLO-2	Lab 5: Study of sampling theorem	Lab 11: Efficient computation of DFT using FFT	Lab 17: Design of digital FIR Low Pass, High Pass, Band pass and band stop filter using Black mann window	Lab 23: Design of digital Cheby shev filter using impulse invariance method	Lab 29: Design of anti-aliasing filter
S-15	SLO-1 SLO-2	Lab 6: Aliasing effects	Lab12: Computation of IDFT	Lab 18: Design of digital FIR filter using frequency sampling method	Lab 24: Design of <mark>digital Cheb</mark> y shev filter using bilinear tra <mark>nsformation</mark>	Lab 30: Design of anti-imaging filter

Learning Resources  1. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing, Principles, Algorithms and Applications", Pearson Education, 4th edition, 2014 2. Alan V. Oppenheim, Ronald W. Schafer, "Discrete-Time Signal Processing", Pearson Education, 1st edition, 2015	<ol> <li>Sanjit Mitra, "Digital Signal Processing –A Computer Based Approach", McGraw Hill, India, 4th Edition, 2013.</li> <li>Fredric J. Harris, "Multirate Signal Processing for Communication Systems", 1st edition, Pearson Education, 2007</li> </ol>
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	Bloom's			Cont	tinuous Learning Asse	essment (50% weig	htage)			Final Evamination	(EOO/ woightogo)		
	Level of Thinking	$(1 \Delta = 1)$		CLA -	CLA – 2 (15%)		3 (15%)	CLA – 4	l (10%)#	Final Examination (50% weightage)			
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice		
Level 1	Remember Understand	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%		
Level 2	Apply Analyze	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%		
Level 3	Evaluate Create	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%		
	Total	10	0 %	10	00 %	100	0 %	10	0 %	10	0 %		

# CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	Dr. M.S. Vasanthi,, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	



Course Code	18ECC205J	Course Name	ANALOG AND	DIGITAL COMMUNICATION		Cours atego		C			Р	rofess	ional	Core				3	T 0	P 2	C 4
Pre-requ Course Offering	uisite Courses Department	18MAB203T	Co-requisite Courses ECE	Nil Data Book / Codes/Standards			Progre	ssive Co	urses				CC30 Nil	1T, 18	BECC3	02J, 1	18ECE	:221T	& 18E	ECE223	}T
Course Learning	Rationale (CLR):	The purpose of learning	n <mark>g this course</mark> is to:		1	_earni	ng		H			Progr	ram L	earnir	ng Out	comes	(PLC	))			
	luce and Understa emodulators	and the need for modulation	<mark>, various A</mark> mplitude modulator	s/demodulators, frequency modulators	1	2	3	1	2	3	4	5	6	7	8	9 1	0 1	1 12	13	14	15
CLR-3: Introd CLR-4: Analy CLR-5: Introd CLR-6: Gain	mance luce basics of Digi ze the pass band luce basics of spre hands-on experier	ital modulation and detection data transmission technique ead spectrum techniques an ince to put theoretical conce	n techniques es in terms of probability of ern nd information theory concepts pts learned in the course to pr	THE REAL PROPERTY AND THE PERSON	rel of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	-	呈	Environment & Sustainability	-	Individual & Team Work	Collinging & Finance	Long Learning	–1: Pro	Nevement O – 2: Project Management	PSO – 3: Analyze & Research
Course Learning			se, learners will be able to:		Level		Exp		Pro	Des	Ana	Mo	Soc	En	Ethics			Life		PSO Tech	PS(
		ts of analo <mark>g modulat</mark> ion and		With the second second	2	80	70	М	-	-		-	-	-	-	- <i>F</i>	1 -	-	Н	-	-
CLO-2: Learn	the function of ra-	dio transmi <mark>tters and</mark> receive	ers and familiarize with noise p	erformance of various receivers	2	85	75		М	Н	-	-		-	-	-   -			Н	-	-
CLO-3: Under	rstand various dig	ital modula <mark>tion sche</mark> mes an	d matched filter receiver		2	75	70	M	-	-	-	-	-	-	-	-   .	.   -	-	-	М	Н
CLO-4: Under	rstand and analyz	e various d <mark>igital pas</mark> s band	data transmission schemes		2	85	80	-	11-	-	M	-	-	-	-	-   -	.   -		-	М	-
			ectrum and error coding technic		2	85	75	-	Н	-	-	-	-	-	-	-   -			М		Н
CLO-6 : Analy	ze the operation on the compare exp	of analog an <mark>d digital c</mark> ommu perimental results in the lab	inication systems and take me poratory with theoretical analys	asurement of various communication	2	85	75	-	-	Н	-	Н	-	-	- 1	┥ .	-   -	М	-	М	Н

Durat	on (hour)	Analog Modulation	Radio Transmitters and Receivers	Digital Modulation System and Baseband Detection	Passband Data Transmission	Spread Spectrum Techniques and Information theory Concepts
		15	15	15	15	15
S-1	SLO-1	Modulation, Need for Modulation,	AM transmitter : Low Level,	Pulse modulation systems, Overview of PAM,PWM,PPM	Overview of ASK, FSK, PSK	Spread spectrum Communications, Frequency Hopping Spread Spectrum (FHSS)
3-1		Amplitude Modulation, Types of Amplitude Modulation	AM transmitter : High Level Transmitter	Pulse modulation systems, Overview of PAM,PWM,PPM	Overview of ASK, FSK, PSK	Spread spectrum Communications, Frequency Hopping Spread Spectrum (FHSS)
S-2	SLO-1	Double sideband Full carrier	FM transmitter: Direct Method	Pulse modulation systems, Sampling and quantization	Generation, Signal Space Diagram and detection of FSK	Direct Sequence Spread Spectrum (DSSS)
3-2	SLO-2	Double sideband Full carrier	FM transmitter: Direct Method	Pulse modulation systems, Sampling and quantization	Generation, Signal Space Diagram and detection of FSK	Direct Sequence Spread Spectrum (DSSS)
	SLO-1	Double sideband Suppressed carrier	FM transmitter: Indirect Method	PCM systems	Probability of Error for FSK	Direct Sequence Spread Spectrum (DSSS)
S-3		Single sideband Suppressed carrier, VSB	FM transmitter: Indirect Method	Bandwidth of PCM, PCM TDM signal multiplexing, Limitations of PCM system	Probability of Error for FSK	Code Division Multiple Access of DSSS
S 4-5	SLO-1 SLO-2	Lab-1: AM modulator and Demodulator	Lab-4: Pre emphasis and De-emphasis	Lab-7: DPCM and its Demodulation	Lab-10: QPSK Modulation and Demodulation	Lab-13: Mini Project

Duration	on (hour)	Analog Modulation	Radio Transmitters and Receivers	Digital Modulation System and Baseband Detection	Passband Data Transmission	Spread Spectrum Techniques and Information theory Concepts
		15	15	15	15	15
S-6	SLO-1	Generation of AM waves: Linear method-Collector modulator	Classification of radio receiver, Functions and Characteristics of radio receiver	Data formatting	Generation, Detection, Signal Space Diagram of PSK	Code Division Multiple Access of DSSS
3-0	SLO-2	Generation of AM waves: Linear method- Collector modulator	Tuned Radio Frequency receiver	Data formatting	Generation, Detection, Signal Space Diagram of PSK	OFDM Communication
S-7	SLO-1	Non-linear Modulation-Balanced Modulator	Super-heterodyne receiver- AM	Differential PCM (DPCM)	Probability of Error for PSK	OFDM Communication
5-1	SLO-2	Non-linear Modulation-Balanced Modulator	Super-heterodyne receiver- AM	Differential PCM (DPCM)	Probability of Error for PSK	OFDM Communication
0.0	SLO-1	Demodulation of AM waves : Linear diode detector	Super-heterodyne receiver- FM	Delta modulation (DM)	Generation, signal space diagram and detection of QPSK	Measures of Information
S-8	SLO-2	Demodulation of AM waves : Linear diode detector	Super-heterodyne receiver- FM	Delta modulation (DM), Noise in DM	Generation, signal space diagram and detection of QPSK	Measures of Information
S 9-10	SLO-1 SLO-2	Lab-2: DSB-SC modulator and demodulator	Lab-5: PAM,PPM,PWM modulation and demodulation	Lab-8: DM and its Demodulation	Lab-11: DPSK Modulation and Demodulation	Lab-14: Model Practical Exam
0.44	SLO-1	Frequency modulation, Types of FM	Sources of Noise	Demodulation and detection process	Probability of Error for QPSK	Source encoding, Shannon's Channel capacity theorem
S-11	SLO-2	Narrow Band FM, Wide Band FM, Phase modulation	Sources of Noise	Demodulation and detection process	Probability of Error for QPSK	Shannon's Channel capacity theorem
0.40	SLO-1	Generation of Narrowband FM	Noise in AM (Envelope Detection),	Maximum likelihood receiver structure, Matched filter receiver	Generation, signal space diagram and detection of π/4 QPSK	Linear block codes
S-12	SLO-2	Generation of Narrowband FM	Noise in AM (Envelope Detection),	Maximum likelihood receiver structure, Matched filter receiver	Generation, signal space diagram and detection of π/4 QPSK	Linear block codes
C 12	SLO-1	Demodulation of FM : Foster seely discriminator	Noise in FM	Probability error of the Matched filter, Intersymbol interference, Eye pattern	Generation, signal space diagram and detection of QAM	Cyclic codes
S-13	SLO-2	Demodulation of FM : Foster seely discriminator	Threshold effect, Pre-emphasis and De- emphasis	Probability error of the Matched filter, Intersymbol interference, Eye pattern	Generation, signal space diagram and detection of QAM	Cyclic codes
S 14-15	SLO-1 SLO-2	Lab-3: FM Modulator and Demodulator	Lab-6: Pulse Code Modulation and Demodulation		Lab-12: BER performance analysis of various Modulation Schemes	Lab-15: University Practical Exam

	1.	Simon Haykin and Michael Moher, "Communication Systems," 5th edition, John Wiley & Sons,	5.	Taub & Schilling, "Principle of Communication Systems", McGraw Hill Inc, 2nd Edition, 2003.
		2013		6. John G. Proakis, "Digital Communication", McGraw Hill Inc, 5th Edition, 2008.
Loorning	2.	Singh. R. P & Sapre. S. D, "Communication Systems: Analog & Digital," 3rd edition, McGrawHill	10	7. B.P. Lathi, "Modern Digital and Analog Communication System", Oxford University Press, 3rd Edition,
Learning		Education, Seventh Reprint, 2016.		2005.
Resources	3.	Simon Haykin, "Communication Systems", John Wiley & Sons, 4th Edition, 20008.	8.	Shu Lin, Daniel Costello, "Error control coding – Fundamentals and Applications", Prentice Hall, Upper Saddle
	4.	Bernard Sklar, "Digital Communication, Fundamentals and Application", Pearson Education Asia,	-	River, NJ, 2nd Edition, 2004.
		2nd Edition, 2001	9.	Lab Manual

	Bloom's			Cont	tinuous Learning Asse	essment (50% weig	htage)			Final Evamination	o (EOO) woightage)
		CLA –	1 (10%)	CLA -	- 2 (15%)	CLA –	3 (15%)	CLA – 4	l (10%)#	Final Examinatio	n (50% weightage)
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%
Level 2	Apply Analyze	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
_evel 3	Evaluate Create	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
	Total	10	0 %	10	00 %	100	0 %	10	0 %		-

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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	L III



Course Coo	de 18ECC206J	Course Name	VLSI D	ESIGN		Course atego		С			Pi	Professional Core				l (	_ T	P 2	C 4		
Pre-	requisite Courses	18EC	C103J Co-requisite Courses	Nil		Р	rogres	sive Cou	rses							18EC	E301	J			
Course Offer	ring Department	Electro	onics and Communication Engineering	Data Book / Codes/Standards									Nil								
(CLR):		•	ng this course <mark>is to:</mark> uage for FPGA in electronic design automa	ation of digital circuits	L 1	earnin	g 3	1	2	3	4	Prog	ram l	Learni 7	ing Ou	utcom	es (Pl	LO) 11   12	13	14	15
CLR-2: D	esign, construct and	simulate VLSI add		anon or arguar on ource			H	9													
CLR-3: Understand MOSFET operation  CLR-4: Implement a given logic function using appropriate logic styles for improved performance  CLR-5: Understand the basic processes in IC fabrication, steps in the fabrication of MOS ICs, and as well the layout design rules.							t (%)	dge	Ó	ent	Research			Sustainability		Work		9	l Achievement	ınagement	Research
	lse modern engineer oith the design and ar		HSPICE / Modelsim / Xillinx to carry out descuits and systems.	sign experiments and gain experience	f Thinking (Bloom)	Expected Proficiency (%)	ed Attainment	Engineering Knowledge	n Analysis	Design & Development	Design,	Tool Usage	& Culture	∞ర		⊑	.≘	Project Mgt. & Finance Life Long Learning	: Professional	2: Project Management ques	3: Analyze &
Course Lear (CLO):	ning Outcomes At th	ne end of this <mark>cour</mark>	rse, learners will be able to:		Level of	Expecte	Expected	Engine	Problem	Design	Analysis,	Modern	Society	Environment	Ethics	Individual	Commu	Project Mgt. Life Long Le	PSO-1	PSO – 2: Technique	PS0 -
	esign and implemen	t digital circu <mark>its usi</mark>	ing Verilog HDL to simulate and verify the	designs.	3	85	75		Н	Н	-	Н	-	-	-	-	-		-		-
			<mark>ts, a</mark> dder cells and multipliers to address th		3	85	75		Н	Н	-	Н	-	-	-	-	-		-	-	-
CLO-3: E	xamine the characte	ristics of MO <mark>S tran</mark>	nsistors	TOTAL TO A STATE OF THE	2	80	70	Н	М	-	-	-	-	-	-	-	-		-	-	-
			<mark>lex l</mark> ogic gates designed using different log		2	80	70	7	L	L	-	-	-	-	-	-	-		-	-	-
			<mark>d un</mark> derstand the physical implementation o		2	80	70		L	L	-	-	-	-	-	-	-		-	-	-
CLO-6: <i>U</i>	lse HSPICE compute	er analysis pr <mark>ogran</mark>	<mark>n an</mark> d Verilog HDL for simulation and analy	ysis of MOS circuits and building blocks	3	85	75	-	M	M	- 1	Н	-	-	-	Н	М	L M	-	-	Μ

Dunatia		Introduction to Verilog HDL & Coding	Subsystem Design	MOS Transistor	CMOS Inverter and Circuit Design Styles	Microelectronic Materials
Duratio	n (hour)	15	15	15	15	15
	SLO-1	Introduction to HDL & Verilog HDL	General VLSI System Components: Multiplexers		CMOS Inverter Characteristics: Operation and properties of static CMOS inverter	Properties of basic materials used in microelectronics: Silicon, Silicon dioxide
S-1	SLO-2	Introduction to Verilog HDL, modules and ports	MOS structure: accumulation, depletion, inversion; nMOS transistor: cutoff, linear, saturation regions of operation		VTC of static CMOS inverter	Polysilicon and Silicon Nitride
S-2	SLO-1	Lexical Conventions: White Space and Comments, Operators	Comparators	MOS Transistor under Static Conditions: The threshold voltage	DC Inverter Calculations	IC Fabrication: Wafer Formation, Photolithography,Well,Channel Formation
5-2	SLO-2	Numbers, Strings, Identifiers, System Names, and Keywords	priority encoder	Resistive operation	Symmetrical Inverter	Silicon Dioxide (SiO <sub>2</sub> ), Isolation, Gate Oxide
	SLO-1	Verilog Data Types: Nets, Register Variables, Constants	shift and rotate operations	Saturation region	Inverter switching characteristics	Gate, Source/Drain Formations, Contacts and Metallization, Passivation, Metrology
S-3	SLO-2	Referencing Arrays of Nets or Regs	Adders: Standard adder cells	Current-voltage characteristics	Output capacitance	Recurring Process: Diffusion, Ion Implantation, Deposition, Etching, Planarization
S-4, 5	SLO-1		Lab-3: Design using FSM and ASM charts	Lab-6: Realization of VLSI multipliers - I		

Duratio	n (hour)	Introduction to Verilog HDL & Coding	Subsystem Design	MOS Transistor	CMOS Inverter and Circuit Design Styles	
Duratio	ii (iioui)	15	15	15	15	15
	SLO-2	Lab-0: Verilog Operators: Arithmetic, Bitwise, Reduction, Logical, Relational, Shift, Conditional, Concatenation, Expressions and Operands, Operator Precedence	-0	IF VC I:	Lab-9: Design and Analysis of CMOS Inverter using HSPICE	Lab-12: Design and Analysis of 4-input Dynamic NAND gate using HSPICE
S-6	SLO-1	Verilog modelling: Gate-level modelling	Ripple Carry Adder (RCA)	Dynamic behavior: MOSFET Capacitances, MOS structure capacitances	Secondary Parasitic Effects: Leakage Currents, Parasitic Resistances	Simplified CMOS Process flow
	SLO-2	Realization of Combinational and sequential circuits	Carry Look-Ahead Adder (CLA)	Channel capacitance and Junction (or, depletion) capacitances	Inverter layout	
0.7	SLO-1 Compilation and simulation of Verilog code		Carry Select Adder (CSL)	Parasitic Resistances, viz., Drain and Source Resistance, Contact Resistance	Power-Delay Product: Static Power Consumption	Layout design rules: Well rules, transisto rules
S-7	SLO-2	Test bench	Carry Save Adder (CSA)	Non-ideal I-V effects: Mobility Degradation, Velocity Saturation	Dynamic Power Consumption, Total Power Consumption, PDP	Contact rules, metal rules, via rules and other rules
	SLO-1	Dataflow modelling	Carry Skip Adder (CSK)	Channel Length Modulation, Threshold Voltage Effects	CMOS Circuit Design Styles: Static CMOS logic styles	Gate Layouts
S-8	SLO-2	Realization of Combinational and sequential circuits	Carry Bypass Adder (CBA)	Leakage, Temperature Dependence, Geometry Dependence, Subthreshold Current	CMOS circuits, pseudo-nMOS, tristate circuits, clocked CMOS circuits	Stick diagrams
S-9, 10	SLO-1 SLO-2	Lab-1: Realization of combinational and sequential circuits using gate-level and dataflow modeling	Lab-4: Realization of VLSI adders - I	Lab-7: Realization of VLSI multipliers - II	Lab-10: (a) Design, Analysis of complex CMOS gate using HSPICE (b) Design, Analysis of Pseudo-NMOS gates using HSPICE	Lab-13: Model Practical Examination
S-11	SLO-1	Behavioral modelling	Multipliers: Multiplication (unsigned, shift/add multiplication algorithms, multiplication of signed numbers, types of multiplier architectures)	Short-channel MOSFETS: Hot carriers, Lightly-Doped Drain (LDD)	Differential Cascade Voltage Switch Logic (DCVSL), Pass Transistor Logic (PTL)	and Oxide Thicknesses, Silicon-on-
	SLO-2	Realization of Combinational and sequential circuits	Braun multiplier	MOSFET scaling	Dynamic CMOS logic styles: Basic dynamic logic	Insulator, High-k Gate Dielectrics, Higher Mobility, Plastic Transistors,)
	SLO-1	Switch-level modelling	Baugh-Wooley multiplier	Short-channel effects: Negative Bias Temperature Instability, oxide breakdown	Signal integrity issues in dynamic design	Interconnects
S-12	SLO-2	Realization of MoS circuits	Wallace Tree multiplier	Drain-Induced Barrier Lowering (DIBL), Gate-Induced Drain Leakage (GIDL), Gate Tunnel Current	Signal integrity issues in dynamic design	Circuit elements
S-13	SLO-1	Design using FSM	Booth multiplier	Tutorials	Domino Logic Circuits: Differential Domino logic, multiple-output domino	Beyond conventional CMOS
	SLO-2	Realization of sequential circuits	Booth multiplier	Tutorials	Compound domino, NORA, TSPC	Tutorials
S-14, 15	SLO-1 SLO-2	Lab-2: (a) Realization of digital circuits using behavioral modeling (b) Realization of MOS circuits using switch-level mdeling	Lab-5: Realization of VLSI adders - II	Lab-8: Realization of RAM & ROM	Lab-11:(a)Design,Analysis of AND/NAND gate in DCVSL using SPICE (b) Design, Analysis of Pass-Transistor gates and CPL gates using HSPICE	Lab-14: End-Semester Practical Examination

	1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second
Learning	Edition, Feb 2003, Prentice Hall of India.
Resources	2. Weste, Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th ed., Addision-Wesley, 2011.
	3. Wayne Wolf, "Modern VLSI Design: IP-based Design", 4th edition, PHI, 2009.

- 4. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Wiley, (3/e), 2010. 5. John P. Uyemura, "CMOS Logic Circuit Design", Kluwer, 2001.
- 6. S. Palnitkar , Verilog HDL A Guide to Digital Design and Synthesis, Pearson , 2003
- 2011. 7. Paul. R.Gray, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, (4/e), 2001.
  - 8. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999

Learning Asse	essment											
	Bloom's			Contir	nuous Learning Ass	essment (50% weig	htage)			Final Examinatio	n (EOO) waishtasa)	
	Level of Thinking	CLA – 1 (10%)		CLA – 2 (15%)		CLA –	3 (15%)	CLA – 4	4 (10%)#	Final Examination (50% weightage)		
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	
Level 1	Remember	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%	
Level I	Understand	2070	2070	1070	1070	1070	1070	1070	1070	1070	1070	
Level 2	Apply	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	
LCVCI Z	Analyze	2070	2070	2070	2070	2070	2070	2070	2070	2070	2070	
Level 3	Evaluate	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%	
Level 3	Create	10%	1076	1376	1376	1376	1076	1376	1376	10%	1576	
	Total 100 %		100	100 %		100 %		0 %	100 %			

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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	2. Dr. J. Manjula, SRMIST



Course Code	18ECC301T	Course Name	WIRELESS COMMUNICATION		Cour Categ		С				Professional Core					L 3	T F	C C		
Pre-requisite Course Offering		18ECC205J, 18ECC105T Electronics and Commun	Co-requisite Courses       ication Engineering   Data Book / Codes/Stand	Nil ards		Prog	ıressive	Cours	ses			^	Vil			18EC	E2207	Γ		
Course Learning (CLR):	g Rationale The	e purpose of learning this cours <mark>e is t</mark>	0:	100	Lea	ning					Pr	ograr	m Lear	ning	Outc	omes	(PLO)	)		
CLR-1: Unde	rstand the eleme	nts of Wireless Communic <mark>ation and</mark>	mobile communications	•	1 2	3	1	2	3	4	5	6	7	8	9 ′	0 11	12	13	14	15
CLR-3 : Analy CLR-4 : Study CLR-5 : Acqu CLR-6 : Unde	ze how to apply	e Radio Wave Propagation - Large S Mobile Radio Wave Propagation - S d Diversity concepts in wireless con e of Wireless System and Standards n various wireless systems	Small Scale Fading Innunications		of I ninking (Bloom)	Attainment	Engineering Knowledge	Ane	n & Development	sis, Design, Res <mark>earch</mark>	$\vdash$	y & Culture	Environment & Sustainability	H G	Individual & Team Work	Communication Project Mgt. & Finance	ong Learning	PSO-1: Professional Achievement	- 2: Project gement Techniques	3: Analyz ch
Course Learning (CLO):	AL	the end of this <mark>course, le</mark> arners will b		3	Expected		Fncip	Problem	Design	Analysis,	Modern	Society	Enviro Sustai	Ethics	Indivic	Comm	Life Lo	PSO- Achiev	PSO – Manage	PSO- Resea
CLO-1: Acqu	ire the knowledge	e of Wireless <mark>communi</mark> cation and ba	sic cellular concepts		2 75	60	H	-	-	-	-	-	-	-	-		М	М	-	L
		ntial Radio w <mark>ave propa</mark> gation and mo		1839 2	2 75		H		H	Н	-	-	-	-	-		М	Μ	-	Н
		ous perform <mark>ance anal</mark> ysis of mobile	communication system.		2 75		H		Н	-	-	-	-	-	-		-	-	-	Н
		of Diversity a <mark>nd capac</mark> ity concepts			2 75		H		- 1		-	-	-	-	-		-	-	-	Н
		arious stand <mark>ards of M</mark> obile Communi			2 75		H		-	-	-	-	-	-	-		М	М	-	L
CLO-6: Explo	ore the various co	ncepts of wireless communication, is	ts design with respect to fading and link performan	ce 2	2   75	60	H	H	Н	Н	M	-	-	-	-   ,	И -	M	М	-	H

				the transfer of the same of the same of		
Durat	ion (hour)	Wireless communication: Mobile communications	Large Scale Fading	Small Scale Fading	Improvement on Link performance	Wireless systems and standards
		12	12	12	12	12
S 1	SI ( )_1	Introduction to wireless commu <mark>nication and mobile radio communication</mark>	Introduction to Radio wave Propagation	Introduction Small scale multipath propagation	Introduction to diversity, equalization and	AMPS Voice modulation Process
S-1 SLO-2		Classification of wireless communications - simplex, half duplex, dull duplex	Large scale and small scale fading	Impulse response model of multipath channel	capacity	AINIFS VOICE Modulation Frocess
		Paging and Cordless systems	Friis transmission equation- Free space	Impulse response model of multipath channel	Space diversity	GSM system architecture and its interfaces
S-2	SLO-2	Cellular telephone systems	propagation model - pathloss model	Small scale multipath measurements - Direct Pulse measurement	Scanning diversity	GSIN System architecture and its interfaces
S-3	SLO-1	Timing diagram - landline to mobile	Two Ray model	Small scale multipath measurements - Sliding correlator measurement	Maximal ratio combiner	GSM frame structure
3-3	SLO-2	Timing diagram - mobile to mobile	Two Kay Model	Small scale multipath measurements - Swept frequency measurement	Equal gain diversity	- GSM tranie structure
J 3LO-1		Basic antenna parameters, Far field and near field	Simplified pathloss model	Parameters of mobile multipath channels -	Rake Receiver	GSM speech operations input - output
S-4	SLO-2	Frequency reuse, sectored and omni- directional antennas	Emperical model - Okumara	Time dispersion and Coherent bandwidth	Take Receiver	oom speech operations input - output
S-5	SLO-1	Channel assignment strategies	Emperical model - Hata model		Capacity in AWGN	Forward CDMA process

Durati	on (hour)	Wireless communication: Mobile communications	Large Scale Fading	Small Scale Fading	Improvement on Link performance	Wireless systems and standards
		12	12	12	12	12
	SLO-2	Handoff and its types		Parameters of mobile multipath channels - Doppler spread and Coherent time	100	
	SLO-1			Types of fading: Flat and Frequency		
S-6	SLO-2	Interference and system capacity	Piecewise linear model - log normal model	selective fading	Capacity of flat fading channels	Reverse CDMA Process
S-7	SLO-1	Trunking and Grade of Service	Shadowing	Types of fading: Flat and Frequency	Favolinar and its made	Multiparrier madulation
5-7	SLO-2	Trunking and Grade of Service	Combined pathloss and shadowing	selective fading	Equalizer and its mode	Multicarrier modulation
S-8	SLO-1	Cell splitting	Cell splitting Outage Probabilty		Adaptive equalizer block diagram	OFDM Transmitter Block diagram
	SLU-2	5		Types of fading: Fast and Slow fading		
S-9	SLO-1	Sectoring	Cell Coverage Area	Types of fading: Fast and Slow fading	Types of Equalizers - elementary level only	OFDM Receiver Block diagram
	SLU-2	- Costorning	Con Coverage 7 ii cu	Types of family. Tast and Slow family	Types of Equalizate statistically force only	or Bir Nocoron Brook diagram
S-10	SLO-1	Microcell zone concepts	Solving problems – Brewster angle	Ricean distribution	Introduction to MIMO antennas	Importance of Cyclic Prefix
0-10	SLO-2	Wildrocell Zone concepts	Colving problems – Brewster angle	Tricean distribution	introduction to winvio antennas	Importance of Oyene Frenz
S-11	SLO-1 SLO-2	Umbrella cells	Solving problems –empirical model	Rayleigh distribution	Introduction to MIMO antennas	Case study - Modern antennas
S-12	SI O 1	Solving Problems	Solving problems – friis transmission formula		Case study :Recent trends in Diversity and MIMO antennas	Case study - Modern antennas

		1.	Rappaport.T.S., "Wireless Communications: Principles and Practice", 2 <sup>nd</sup> Edition, Pearson, 2011.
	Loorning	2.	John D Kraus , Ronald J Marhefka, Ahmed S Khan "Antenna and Wave Propagation", 4th Edition, Tata
ш	Learning		McGraw Hill, 2010
	Resources	3.	Constantine Balanis. A, "Antenna Theory: Analysis and Design", 3rd Edition, John Wiley, 2012.
		4.	Andreas.F.Molisch., "Wireless Communications", Wiley, 2nd Edition-2005, Reprint-2014

- Andrea Goldsmith, "Wireless Communications", Cambridge University Press, Aug 2005
   Schiller, "Mobile Communications", Pearson Education Asia Ltd., Reprint 2012
   Lee W.C.Y., " Mobile Communications Engineering: Theory and Applications", McGraw Hill, New York, 2nd Edition, 1998

Learning Ass	essment					A Shirt						
	Dia ami'a		100	Conti	nuous Learning Asse	essment (50% weig	htage)			Final Evansination	n (EOO) (waishtana)	
	Bloom's Level of Thinking	CLA –	1 (10%)	CLA –	2 (15%)	CLA –	3 (15%)	CLA – 4	4 (1 <mark>0%)#</mark>		n (50% weightage)	
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	
Level 1	Remember Understand	40 <mark>%</mark>	- 1	30 %	53/4	30 %	- 10/	30 %		30%	-	
Level 2	Apply Analyze	40 %		40 %		40 %		40 %	<u> </u>	40%	-	
Level 3	Evaluate Create	20 %	<b>1</b>	30 %	AKC A. A.	30 %	LINE	30 %	<b> </b>       -	30%	-	
	Total	100	0 %	100 %		10	0 %	10	0 %	100 %		

# CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	1. Dr. Sandeep Kumar P, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	2. Dr. T. Ramarao, SRMIST

Course C	Code 1	BECC302J	Course Name	MICROWAV	/E & OPTIC	AL COMMUNICATIONS		Cours		С					Profe	ssion	al Co	re				L 3		P 2	C 4
	Pre-requisite Offering Dep		18ECC205J Electronics and	Co-requisite Courses Communication Engineering	Data Book	Nil / Codes/Standards						Pr	ogres	sive (	Cours	es	N	il	,	18EC	E22	6T & 18	ECE32	<u>23T</u>	
(CLR): CLR-1 :		I ne pur licrowave active de	pose of learning this c		5	MAY C	1	_earn	ing 3	1	1	2	3	4	Prog	gram 6		ning Ou	tcome			13	14		15
CLR-2 : CLR-3 : CLR-5 : CLR-6 :	Explore N Analyze ( Measurer Explore (	nents Optical Communica Microwave and opt	ements cal Sources, Amplifier ntion System Design a ical components	5/	ors , Receive	er and Performance	evel of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)		Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Res <mark>earch</mark>	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics ndividual & Team Work	Communication	Project Mgt. & Finance	ife Long Learning	⊃SO–1: Professional Achievement	PSO – 2: Project Management Fechniques	<b>=</b>	) – 3: Analyze & Kesearch
(CLO): CLO-1 : CLO-2 : CLO-3 :	Acquire k	nowledge on the to nicrowave passive	device <mark>s and co</mark> mpon	ansmission, microwave generato ents.		ciated components.	2 2 2	80 80 80	70 70 70		H Eng	- M	н Н	M H I Ana	Moc	- Soc	- Env	r · · Ethics	- Cor	- Pro	- Life	PSO.	PSO Tech		OSA L M H
CLO-4: CLO-5:	CLO-4: Familiarize with the fundamentals of light transmission through fiber CLO-5: Design a basic optical communication system.  Understand the working principle of microwaye components. Microwaye measurements, entired sources, detector and						2 2 2	80 80 80	70 70	i	H H	H	- - H	M H	-	-	-		-	-	-	L M M	-	j	L M H
	fibers on (hour)	<u> </u>	15	15		15		00	10			"	15			i		-   -			1			<u></u>	<u>-</u>
S-1	SLO-1 SLO-2	Introduction to m	icrowaves <mark>and optic</mark> al	High frequency parameters: S S matrix analysis for N-port mid device		Impedance matching.	Elements of Optical fiber communication Point-to-Point link –Analog syst considerations and design step					lesig	n												
S-2	SLO-1 SLO-2	History of Microw Microwave transi Applications; Max	rave Enginee <mark>ring,</mark> mission and	Directional coupler	e vin	VSWR and Impedance meas	R and Impedance measurement Functional block diagram of a Transmitter and receiver module Point-to-Point link – Digital considerations and design					lesig	n												

Insertion loss measurements

Measurement of Power

Lab- 7 Practice session

Measurement of Frequency and Q factor

Optical fiber structure, Light Propagation in

Digital Link Design: Link power budget

Overview of Analog links: Radio over

Lab- 13 Design of basic Optical

Communication system using

computational tool

Rise time budget

Fiber;

Optical fibers: Ray theory, Total Internal

Aperture, propagation and bending losses

Optical Sources: Light source materials,

Lab- 10 Measurement of Numerical

reflection, Skew rays

of optical fiber

LED Structures

LED Characteristics

SLO-1

SLO-2

SLO-1

SLO-2

SLO-1

SLO-2

SLO-1

SLO-2

S-3

S-4-5

S-6

S-7

Microwave Tubes

Klystron amplifier

Klystron

Lab- 1 Characteristics of Reflex

Reflex Klystron oscillators

Magnetron oscillators

E and H plane Tee

antenna

Magic Tee

Lab- 4 Gain and radiation pattern of Horn

Microwave Circulators, Isolators

Duratio	n (hour)	15	15	15	15	15
S-8	SLO-1 SLO-2	Microwave Bipolar Transistors Field effect transistor	Attenuators and Phase Shifters		Semiconductor Laser Diode, Laser Characteristics	Key link parameters
S-9-10	SLO-1 SLO-2	Lab- 2 Study of power distribution in Directional coupler, E plane, H plane and Magic Tee	Lab- 5 Characteristics of filters, Microstrip patch antenna and parallel line coupler	Lab- 8 DC characteristics of LED and Laser diode	Lab- 11 Analysis of Analog optical link	Lab- 14 Practice Session
S-11	SLO-1 SLO-2	IMPATT, TRAPATT and Tunnel diode	Rectangular Waveguides	IMeasurement of Scallering parameters	Optical Detectors: PIN and APD photo detector	Multichannel System: Need for multiplexing Operational principles of WDM, DWDM
S-12	SLO-1 SLO-2			Measurement of Scattering parameters	Responsivity and efficiency of APD	WDM Components: Coupler/Splitter, Fabry Perot Filter
S-13	SLO-1		Power Dividers	Functioning details of Vector Network Analyzer; Signal Analyzer; Spectrum analyzers	Fiber attenuation and dispersion	WDM Components: Optical MEMS switches
S-14-15		Lab- 3 Impedance measurement by slotted line method	Lab- 6 Design of RF Filters and Amplifier using computational tool	Lab- 9 DC characteristics of PIN and APD photo-diode	Lab- 12 Analysis of Digital optical link	Lab- 15 Study experiment - Gunn Diode (Microwave) and Optical WDMA (Optical)

	1 4	D '114 D "41"
	1.	David M. Pozar, "Microwave Engineering", 4th Edition, John Wiley & Sons, 2012.
	2.	David M. Pozar, "Microwave & RF Design of Wireless Systems", John Wiley & Sons, 2001.
	3.	Samuel Y. Liao, "Microwave Devices and Circuits", 3rd Edition, Pearson Education, 2013.
Learning	4.	Robert. E. Collin, "Foundations for Microwave Engineering", 2nd edition, Wiley, Reprint 2014.
Resources	5.	Annapurna Das, Sisir K. Das, "Microwave Engineering", 3rd Ed., McGraw Hill, 2015.
Resources	6.	I. Hunter, "Theory and design of microwave filters", The Institution of Engineering &Technology,
		2001.
	7.	Keiser G, "Optical Fiber Communication Systems", 5th Edition, 6th Reprint, McGraw Hill Education
		(India), 2015.

- 8. Vivekanand Mishra, Sunita P. Ugale, "Fiber Optic Communication: Systems and Components", Wiley-India, 1st edition, 2013
- 9. Djafar.K. Mynbaev and Lowell and Scheiner, "Fiber Optic Communication Technology", Pearson Education Asia, 9th impression, 2013
- 10. John M. Senior, "Optical fiber Communications: Principles and Practice", Pearson Education, 3rd Edition,
- 11. R.P. Khare, "Fiber Optics and Optoelectronics", Oxford University Press, 2007.

  12. Rajiv Ramaswami, Kumar N. Sivaranjan, Galen H.Sasaki "Optical Networks A practical perspective", 3nd edition, 2013

Learning Asse	essment			Martin -								
	Bloom's		1 - 2 V	Cont	tinuous Learning Ass	essment (50% weig	htage)			Final Examination	n (E00/ waightaga)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA –	3 (15%)	CLA –	4 ( <mark>10%)#</mark>	Final Examination (50% weightage)		
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	
Level 1	Remember Understand	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%	
Level 2	Apply Analyze	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	
Level 3	Evaluate Create	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%	
	Total	10	0 %	10	00 %	10	0 %	10	0 %	10	00 %	

<sup>#</sup> CLA - 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	2. Dr. T. Ramarao, SRMIST

Course Code	18ECC303J	Course Name	COMPUTER COMMU	NICATION NETWORKS		ourse tegory	/	С	Professional Core			L T P 3 0 2		C 4						
Pre-requ Course Offering	uisite Courses Department	18CSS101J Electronics and	Co-requisite Courses Communication Engineering	Nil Data Book / Codes/Standards	-			Prog	ressive	Course	es			Nil	18	ECE3	20T			
Course Learning Rationale CLR):  The purpose of learning this course is to:							ng	Ē		h	F	Progra	m Lear	ning Ou	ıtcome	es (PL	.O)			
	uce the basic cor	cepts in the field of comp	<mark>uter networ</mark> ks.		1	2	3	1	2 3	4	5	6	7	8 9	10	11	12	13	14	15
CLR-3 : Acquii CLR-4 : Analy. CLR-5 : Famili	re knowledge of ze the various iss arize the various the networking of	nal aspects of OSI model, the Network Layer protoco ues and challenges of Tra Application Layer Protoco concepts to analyze the pe	ols ansport Layer. ols. erformance of Routing protocols		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics Individual & Team Work	tion	Project Mgt. & Finance	Life Long Learning	PSO-1: Professional Achievement	PSO – 2: Project Management Techniques	PSO – 3: Analyze &
	ss the basic serv	ices and con <mark>cepts rel</mark> ated	to internetworking.		1	60	65		-			-	Н		-	-	M	-	-	-
		nodel archit <mark>ecture an</mark> d its			1	60	65		- N				L		-	-	-	-	-	Н
		etwork Laye <mark>r concep</mark> ts, me		WITH WITH SILVER	2	65	65		- H		-	L	М		-	-	-	-	-	-
CLO-4: Descr	ibe the services a	and techniq <mark>ues of Tra</mark> nspo	ort Layer.		1	60	65	l la			-	-	М		-	-	-	-		Н
		vices and p <mark>rotocols i</mark> n Ap <sub>l</sub>			1	60	65	-	- N	-	-	-	-	-   -	-	-	-	-	-	Н
CLO-6: Analy	ze the various Ne	tworking co <mark>ncepts a</mark> nd Ro	outing protocols.	Control of the second s	2	60	65				L	_	-	-   -	-	-	M	-	-	H

Duratio	on (hour)	Data Communicat <mark>ion &amp; Networking Basics                                   </mark>	Osi Lower Layers	Network Layer	Transport Layer	Application Layer
		15	15	15	15	15
S-1	SLO-1	Introduction to Data Commu <mark>nication and Networking</mark>	Network models	Introduction to Network Layer	Introduction to Transport Layer	Introduction to Application Layer
3-1	SLO-2	Data transfer modes-Serial and Parallel transmission	OSI layer architecture	Need for Internetworking	TCP/IP Model	Application Layer Paradigms
S-2	SLO-1	Protocols & Standards	Data Link Layer-Introduction	Addressing-Classful	User Datagram Protocol(UDP)	Client Server Interaction
3-2	SLO-2	Layered Architecture	Link Layer Addressing	Addressing-Classful	User Datagram Protocol(UDP)	Client Server Interaction
	SLO-1	Principles of Layering & Description	Error Detection	Addressing-Classless	Transmission Control Protocol(TCP)	SIP
S-3		Brief description of concepts in OSI & TCP/IP model	Error Detection	Addressing-Classless	Transmission Control Protocol(TCP)	SIP
S 4-5	SI O-2	Lab 1: To build and configure a simple network of four nodes connected with point-to-point links.	Lab 4: To simulate token ring protocol and to study its performance.	Lab 7:To simulate CSMA/CA protocol and to study its performance	Lab 10: Implementation and study of Selective Repeat protocol.	Lab 13: Create a Socket (TCP&UDP) between two computers and enable file transfer between them.
S-6		Switching Types- Circuit- & Packet switching	Error Correction	Network Layer Protocol-IPV4	TCP Services & Features	Compression Techniques
3-0		Switching Types- Message switching, Comparison of switching types	Error Correction	Internet Protocol(IP)-IPV4	TCP Services & Features	Compression Techniques

Duratio	n (hour)	Data Communication & Networking Basics	Osi Lower Layers	Network Layer	Transport Layer	Application Layer
		15	15	15	15	15
S-7	SLO-1	LAN, MAN & WAN	Data link control-LLC	Internet Protocol(IP)-IPV6	Congestion Control	Introduction to Cryptography
5-1	SLO-2	LAN, MAN & WAN	Data link control-LLC	Internet Protocol(IP)-IPV6	Congestion Control	Types, Attacks and Services
0.0	SLO-1	Network topologies-Types	Data link control-MAC	Routing Protocols- Distance Vector& Link State	Congestion Control	DES
S-8	SLO-2	Comparison of topologies	Data link control-MAC	Routing Issues-Delivery, Forwarding and Routing	Congestion Control	DES
S	SLO-1	Lab 2: To simulate star and bus network	Lab 5: Implementation of Error detection	Lab 8: Implementation and study of stop	Lab 11: To configure a network using Link	Lab 14: Implementation of Data Encryption
9-10	SLO-2	topologies.	and Correction scheme.	and wait protocols	State Routing protocol.	and Decryption.
S-11	SLO-1	IEEE standards for LAN-Ethernet	Flow & Error Control Protocol	Routing Information Protocol-RIP	QOS-Quality of Service	RSA
5-11	SLO-2	Types of Ethernet	Flow & Error Control Protocol	Routing Information Protocol-RIP	QOS-Quality of Service	RSA
S-12	SLO-1	Token Bus	ARQ Schemes	Open Shortest Path First-OSPF	Techniques to improve QOS	Email
5-12	SLO-2	Token Ring	ARQ Schemes	Open Shortest Path First-OSPF	Techniques to improve QOS	FTP
0 10		FDDI	HDLC	Border Gateway Protocol-BGP	Techniques to improve QOS	HTTP
S-13	SLO-2	FDDI	HDLC	Border Gateway Protocol-BGP	Techniques to improve QOS	SNMP
S	SLO-1	Lab 3: To simulate token bus protocol	Lab 6:To simulate CSMA/CD protocol and	Lab 9: Implementation and study of Go	Lab 12: To configure a network using	Lab 15: Mini Project
14-15	SLO-2	and to study its performan <mark>ce.</mark>	to study its performance	back N protocol.	Distance Vector Routing protocol.	Lab 13. Willii FTOJEGI

Learning	1. Behrouz A.Fehrouzan, "Data communication & Networking", Mc-Graw Hill, 5th Edition Reprint, 2014.
Resources	2. Andrew S.Tanenbaum <mark>, "Compu</mark> ter Networks", Pearson Education India, 5th Edition, 2013.
Resources	3. William Stallings, "Data & Computer Communication", Pearson Education India, 10th Edition, 2014

- 4. James F. Kurose, Keith W. Ross, "Computer Networking: A Top–Down Approach Featuring the Internet", Pearson Education, 6<sup>th</sup> Edition, 2013.
- 5. "Lab Manual", Department of ECE, SRM Institute of Science and Technology

Learning Ass	sessment			The second second		Carlo Carlo	200						
_	Dle em'e			Contir	nuous Learning Asse	essment (50% weig	htage)			Final Examination	n (FOO) weighteen		
	Bloom's	CLA -	1 (10%)	CLA – 2	CLA – 2 (15%)		3 (15%)	CLA –	4 (10%)#	Final Examination (50% weight			
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice		
Lovel 1	Remember	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%		
Level 1	Understand	20%	20%	10%	10%	10%	10%	1376	13%	10%	10%		
Level 2	Apply	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%		
Level 2	Analyze	2070	2078	2070	2070	2070	2070	2070	2078	2070	2070		
Level 3	Evaluate	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%		
revel 2	Create	1070	1070	10/0	13/0	13/0	1370	1370	1376	1370	1370		
	Total	10	0 %	100	) %	10	0 %	10	0 %	10	00 %		

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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	

Course Code	18ECC350T	Course Name	CC	OMPREHENSION	Course Category	С		Pro	ofessio	onal C	ore			L	T 1	P 0	C 1
Pre-requisite Courses Nil Co-requisite Courses Nil Progressive Courses									Nil								
Course Offering Department Electronics and Communication Engineering Data Book / Codes/Standards Nil																	
Course Learning Ra(CLR):	ationale The purpos	e of learning this cour <mark>se</mark>	e is to:	SCH	Soling)		Learning			Pro	gram L	earning	g Outco	mes (l	PLO)		
	kills to solve real world	d problems in Analog ar	nd Digital Electronics (Discrete	e & IC)			1 2 3	1	2	3 4	5	6 7	8 9	10	11 1:	2 13	14 15
			nd Digital Communication	A TOTAL STREET		7 7				ج.							
										t g			ج ا	≤	a>		
CLR-4: Acquire s	kills to solve real world	d problems i <mark>n Micropro</mark> d	essors & Microcontrollers, an	d VLSI Design			cy (	edc		nen	a)		Work	2	Finance		
CLR-5 : Acquire skills to solve real world problems in Electromagnetics and Transmission Lines										ndo I	gag	ഉ	E		i-   i	20	
CLR-3: Acquire skills to solve real world problems in Signals & Systems, and DSP  CLR-4: Acquire skills to solve real world problems in Microprocessors & Microcontrollers, and VLSI Design  CLR-5: Acquire skills to solve real world problems in Electromagnetics and Transmission Lines  CLR-6: Acquire skills to solve real world problems in Microwave and Optical Communications									alys	Development	'  ຼັ∷  :	Culture ent &	Team	tion	જ હૈ	5	
- Thin   Thin   Att   Paris   Paris									Ang	& De		z   E	~	ica i	Mgt.	ול	
CLR-3: Acquire skills to solve real world problems in Signals & Systems, and DSP  CLR-4: Acquire skills to solve real world problems in Microprocessors & Microcontrollers, and VLSI Design  CLR-5: Acquire skills to solve real world problems in Electromagnetics and Transmission Lines  CLR-6: Acquire skills to solve real world problems in Microwave and Optical Communications  Course Learning Outcomes (CLO):  At the end of this course, learners will be able to:								Ⅱ Engineering Knowledge	Problem Analysis	Design & Development Analysis, Design, Research	Modern Tool Usage	Society & Cultuenvironment &	Ethics Individual 8.	Communication	Project Mg	PSO - 1	1 1 1
CLO-1: Practice and gain confidence and competence to solve problems in Analog and Digital Electronics (Discrete & IC)								Н		H L	L	L L	LL	. L	LL	. M	L M
CLO-1: Practice and gain confidence and competence to solve problems in Analog and Digital Electronics (Discrete & IC)  3 85 80 H H  CLO-2: Practice and gain confidence and competence to solve problems in Analog and Digital Communication  3 85 80 H H  H								Н	M L	L	L L	L L	. L	L L	. M	M M	
CLO-3: Practice and gain confidence and competence to solve problems in Signals & Systems, and DSP								Н	Н	M L	L	L L	L L	. L	L L	. M	L M
CLO-4: Practice and gain confidence and competence to solve problems in Microprocessors & Microcontrollers, and VLSI Design								Н	Н	M L	L	L L	L L	. L	L L	. M	
CLO-5 : Practice and gain confidence and competence to solve problems in Electromagnetics and Transmission Lines								Н		H L	L	L L	L L	. L	L L	. M	
CLO-6: Practice and gain confidence and competence to solve problems in Microwave and Optical Communications																	
F			4767		447.0												
Duration (hour)			3-		3		3							3			
											Tutorial on Optical Communication						
SLO-2   F	SLO-2   Problem Solving   Prob					blem Solving				Problem Solving							
S-2 SLO-1 7					Tutorial on VLSI Design				_	Model Test							
						Problem Solving					Model Test						
			Tutorial on Digital Signal Prod				Tutorial on Microwave Communication Problem Solving				Final Test Final Test						
SLO-2 Problem Solving Problem Solving Problem Solving Problem						em Solving				rına	ı rest						
Learning Resource	1. R.S.Khurm S.Chand &		al Engineering: Conventional a	and Objective Types,	2. R.K.Jain, Conventi Khanna Publishers, 201		bjective Type Qu	estion	& Ans	wers c	n Meci	nanical	Engine	eering	for Coi	mpetit	ions,

Learning Ass	sessment											
	Bloom's		Final Examination									
		CLA – 1 (20%)		CLA – 2 (30%)		CLA – 3 (30%)		CLA – 4 (20%)#		Filiai Examination		
	Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	
Level 1	Remember	40%	-	30%	-016	30%	-	30%	-	-		
	Understand										-	
Level 2	Apply	40%		40%	Drive.	40%	41	40%	-	-	_	
	Analyze										_	
Level 3	Evaluate	20%	13/-	30%		30%	10	30%		-		
	Create	20%							-		-	
	Total	<mark>100 %</mark>		100 %		100 %		10	0 %		-	

# CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu	1. Mr. Manikandan AVM, SRMIST
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in	2. Dr. V. Nithya, SRMIST

