ACADEMIC CURRICULA

Professional Core Courses

ELECTRONIS AND COMPUTER ENGINEERING

Regulations - 2018

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Kancheepuram, Tamil Nadu, India

Course Code	18ECC211J	Course Name	SOLID STATE SEMICONDUCTOR DEVICES	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*18EES101J*	Co-requisite Courses	*Nil*	Progressive Courses	*18ECC201J*
Course Offering Department	*Electronics and Communication Engineering*	Data Book / Codes/Standards		*Nil*	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	*Understand the basics of semiconductors and PN junction diode operation, characteristics and models*			
CLR-2 :	*Study and identify the various special diodes.*			
CLR-3 :	*Interpret the operation, characteristics and biasing arrangements of BJT.*			
CLR-4 :	*Interpret the operation, characteristics and biasing arrangements of MOSFET.*			
CLR-5 :	*Construct the diode and transistor circuits for various applications.*			
CLR-6 :	*Know the fabrication steps of monolithic IC.*			

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	Learning			Program Learning Outcomes (PLO)													
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	*Describe the operation and characteristics of PN junction diode and evaluate the parameters of a PN junction diode.*	*1*	*80*	*70*	*L*	*H*	*-*	*H*	*L*	*-*	*-*	*-*	*L*	*L*	*-*	*H*	*H*	*M*	*-*
CLO-2 :	*Identify the various special diodes and describe their features.*	*1*	*85*	*75*	*M*	*H*	*L*	*M*	*L*	*-*	*-*	*-*	*M*	*L*	*-*	*H*	*H*	*M*	*-*
CLO-3 :	*Characterize the different configurations of BJT and its biasing arrangement*	*2*	*75*	*70*	*M*	*H*	*M*	*H*	*L*	*-*	*-*	*-*	*M*	*L*	*-*	*H*	*H*	*M*	*-*
CLO-4 :	*Recognize the MOSFET operation, characteristics and its biasing methods*	*1*	*85*	*80*	*M*	*H*	*M*	*H*	*L*	*-*	*-*	*-*	*M*	*L*	*-*	*H*	*H*	*M*	*-*
CLO-5 :	*Implement and analyze the various diode and transistor circuits*	*3*	*85*	*75*	*H*	*H*	*M*	*H*	*L*	*-*	*-*	*-*	*M*	*L*	*-*	*H*	*H*	*M*	*H*
CLO-6 :	*Explain the monolithic IC fabrication of active and passive components*	*2*	*80*	*70*	*L*	*H*	*-*	*H*	*L*	*-*	*-*	*-*	*L*	*L*	*-*	*H*	*H*	*M*	*-*

Module		*Semiconductor Basics*	*Special diodes*	*Bipolar Junction Transistors*	*MOS Field Effect Transistors*	*Diode and Transistor circuits*
Duration (hour)		15	15	15	15	15
S-1	SLO-1	*Intrinsic and Extrinsic semiconductors*	*Zener diode*	*Device structure*	*Device structure of D and E-MOSFET*	*Rectifiers-Half Wave*
	SLO-2	*Semiconductor conductivity, Drift and diffusion current*	*Backward diode*	*Physical operation of BJT*	*Physical operation of D and E MOSFET*	*Center tapped Full wave and Bridge rectifier*
S-2	SLO-1	*PN Junction Theory: PN junction formation, energy band structure*	*Varactor diode*	*BJT configurations*	*Current voltage characteristics- Drain characteristics*	*Zener diode voltage regulator*
	SLO-2	*PN junction with open circuited terminals (Equilibrium condition)*	*Step Recovery diode*	*Common Emitter – Current-voltage characteristics*	*Transfer characteristics*	*Diode clipping circuits*
S-3	SLO-1	*Forward biased PN Junction*	*Point contact diode*	*Common Base – Current-voltage characteristics*	*Derivation of Drain current*	*Diode Clamping circuits*
	SLO-2	*Reverse biased PN junction, V-I characteristics*	*PIN diode*	*Common Collector – Current-voltage characteristics*	*Derivation of Transconductance*	*Envelope and Peak to peak detectors*
S 4-5	SLO-1	*Lab 1: PN Junction diode characteristics*	*Lab 4 : Diode clipping and Clamping circuits*	*Lab 7 :BJT Characteristics – Common Emitter, Common base and Common Collector*	*Lab 10: MOSFET Characteristics*	*Lab 13: PSPICE Simulation: MOSFET Common Source and Common Drain VI characteristics*
	SLO-2					
S-6	SLO-1	*PN Junction diode: Ideal diode and V-I characteristics ,*	*Tunnel diode*	*BJT Biasing and Thermal stabilization: DC load line*	*Body Effect*	*Voltage multipliers*

	SLO-2	*Current components in P-N diode*	*Schottky barrier diode*	*Operating point*	*Temperature Effects on V-I characteristics*	*Diode Digital Logic circuits*
S-7	SLO-1	*Temperature effects on PN junction diode characteristics*	*Gunn diode*	*Bias stability*	*Configurations of MOSFET-Common source*	*BJT as an Amplifier*
	SLO-2	*Calculation of Depletion width*	*Impatt diode*	*Base bias*	*Common Gate and Common Drain*	*BJT as a Switch*
S-8	SLO-1	*Potential barrier*	*Opto Electronic devices: Photo emissivity and Photo Electric Theory*	*Collector Feedback bias*	*Biasing in MOS amplifier circuits: Biasing by fixing Vgs*	*MOSFET as an amplifier*
	SLO-2	*Diode Resistance*	*Photo conductivity*	*Emitter feedback bias*	*Biasing in MOS amplifier circuits: Biasing by fixing Vgs*	*MOSFET as a switch*
S 9-10	SLO-1	*Lab 2: Zener diode characteristics*	*Lab 5: Zener diode voltage regulator*	*Lab 8: BJT Biasing circuits- voltage divider bias and Feedback bias*	*Lab 11: MOSFET Biasing Circuits for common source and Common drain*	*Lab 14 : PSPICE Simulation: Diode Rectifiers, Clipping , Clamping and voltage multipliers*
	SLO-2					
S-11	SLO-1	*Transition and Diffusion Capacitance*	*LED*	*Voltage divider bias*	*Biasing using drain to gate feedback resistor*	*Integrated Circuits: Basic Monolithic Integrated Circuits*
	SLO-2	*DC load line analysis*	*Laser diode*	*Voltage divider bias*	*Biasing using drain to gate feedback resistor*	*Steps of Fabrication*
S-12	SLO-1	*Modeling of a diode: Ideal diode model*	*PIN Photodiodes*	*Bias compensation*	*CMOS FET*	*Integrated resistors and capacitors*
	SLO-2	*Piecewise linear model*	*Avalanche Photodiodes*	*BJT Models: h-parameters*	*Introduction to FinFET and TFET*	*Monolithic diodes*
S-13	SLO-1	*Small signal model*	*Solar Cells & Photo Transistors*	*Hybrid π model*	*Small signal operation and Models: DC bias point*	*Integrated transistors*
	SLO-2	*Problem solving on depletion width, diode capacitance and resistance, diode currents, DC load line*	*Opto couplers & Photo Multiplier tube*	*Eber's Moll Model*	*Small signal Equivalent circuit of MOSFET*	*Integrated MOSFET*
S 14-15	SLO-1	*Lab 3: Diode Rectifier circuits: Half wave, Center tapped Full wave and Bridge rectifiers*	*Lab 6: Diode Envelope detectors and voltage multipliers*	*Lab 9: BJT as an amplifier and switch*	*Lab 12:PSPICE Simulation: BJT common emitter and common Collector VI Characterisitcs*	*Lab 15 : PSPICE Simulation: CMOS Inverter*
	SLO-2					

Learning Resources	1. *Adel.s. Sedra, Kenneth.c.Smith, "Microelectronic Circuits, Theory and Applications", Oxford University Press, 6th Edition,2009* 2. *Jacod Millman, Christos.C.Halkias, Satyabrata Jit, " Electronic Devices and Circuits", Mc Graw Hill Private Limited, fourth Edition, 2015.*	3. *David .A.Bell, "Electronic Devices and Circuits" Oxford University Press, 5th Edition,2008* 4. *Anil.K.Maini, Varsha Agarwal, "Electronic Devices and Circuits", John Wiley and Sons, First edition,2009*

Learning Assessment											
	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
Level 2	Apply Analyze	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
Level 3	Evaluate Create	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Total	100 %		100 %		100 %		100 %		-	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*Dr. J. Manjula, Associate Professor, Dept of ECE*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	

Course Code	18ECC212J	Course Name	FUNDAMENTALS OF COMPUTER SYSTEM DESIGN	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	18EES101J	Co-requisite Courses	*Nil*	Progressive Courses	18ECC311J
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/Standards		*Nil*	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	Learning		
		1	*2*	*3*
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	*Understand binary codes, digital arithmetic operations and able to simplify Boolean logic expressions*			
CLR-2 :	*Able to design simple combinational logics using basic gates and MSI circuits, familiarize with basic sequential logic components*			
CLR-3 :	*Understand of the basic structure and operation of a digital computer.*			
CLR-4 :	*To learn about CPU, Stack and Register Organisation*			
CLR-5 :	*Know how data transfer and pipelining concept is implemented*			

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLO-1 :	*Review and articulate Logic gates*	*3*	*80*	*70*
CLO-2 :	*Apply the basic knowledge of logic gates to design combinational circuits*	*3*	*85*	*75*
CLO-3 :	*Classify different type of flip-flops, and construct the counters using the same*	*3*	*75*	*70*
CLO-4 :	*To learn about CPU, Stack and Register Organisation*	*3*	*85*	*80*
CLO-5 :	*Know how data transfer and pipelining concept is implemented*	*3*	*85*	*75*

Program Learning Outcomes (PLO)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	*L*	*H*	-	*H*	*L*	-	-	-	*L*	*L*	-	*H*	-	-	-
CLO-2 :	*M*	*H*	*L*	*M*	*L*	-	-	-	*M*	*L*	-	*H*	-	-	-
CLO-3 :	*M*	*H*	*M*	*H*	*L*	-	-	-	*M*	*L*	-	*H*	-	-	-
CLO-4 :	*M*	*H*	*M*	*H*	*L*	-	-	-	*M*	*L*	-	*H*	-	-	-
CLO-5 :	*H*	*H*	*M*	*H*	*L*	-	-	-	*M*	*L*	-	*H*	-	-	*H*

Module		Binary Codes, Digital Arithmetic and Simplification of Boolean Functions	Combinational Circuits	Sequential Circuits	Basic Computer Organization And Design and Programming The Basic Computer	Central Processing Unit and pipeline processing
Duration (hour)		15	15	15	15	15
S-1	SLO-1	*Binary Codes*	*Basic about combinational circuit, Difference between combinational and sequential circuit*	*Flip-flop and Latch: SR latch*	*Basic Computer Organization And Design: Instruction codes, Computer registers*	*Central Processing Unit : Introduction, General Register Organization, Stack Organization*
	SLO-2	*Digital Arithmetic and Simplification of Boolean Functions*	*Design of half adder*	*JK flip-flop, T flip-flop, D flip-flop*	*Instruction codes, Computer registers*	*Introduction, General Register Organization, Stack Organization*
S-2	SLO-1	*Arithmetic number representation*	*Design of full adder*	*Master-slave RS flip-flop*	*Computer instructions*	*Instruction format*
	SLO-2	*Binary arithmetic*	*Design of substractor*	*Master-slave JK flip-flop*	*Computer instructions*	*Instruction format*
S-3	SLO-1	*Introduction about BCD, Excess 3, Gray code*	*Code converter*	*Registers & Counters*	*Timing and Control, Instruction cycle*	*Addressing Modes*
	SLO-2	*BCD arithmetic simplification*	*Code converter*	*Shift registers (SISO, SIPO, PISO, PIPO)*	*Timing and Control, Instruction cycle*	*Addressing Modes*
S 4-5	SLO-1	*Lab 1: To study and perform about logic gates.*	*Lab 4 : To study and perform about Half substractor and full substractor*	*Lab 7 : To study and perform about Decoder, Demultiplexer, and Multiplexer.*	*Lab 10: To study and perform about J-K and T flip flop.*	*Lab 13: Design and implementation of Synchronous Counters*
	SLO-2					
S-6	SLO-1	*Digital logic gates*	*N bit parallel adder and substractor*	*Universal shift register*	*Memory-Reference Instructions*	*Data transfer and manipulation*
	SLO-2	*Basic theorems and properties of Boolean algebra*	*Look ahead carry generator*	*Counters: Asynchronous/Ripple counters*	*Input-output and interrupt*	*Data transfer and manipulation*
S-7	SLO-1	*Basic theorems and properties of Boolean algebra*	*Decoder*	*Synchronous counters, Modulus-n Counter*	*Design of Basic computer*	*Program Control, Reduced Instruction Set Computer (RISC)*
	SLO-2	*Minimization of Boolean Functions: Algebraic simplification*	*Encoder*	*Ring counter, Johnson counter*	*Design of Basic computer*	*Program Control, Reduced Instruction Set Computer (RISC)*

S-8	SLO-1	*Problems on Algebraic simplification*	*multiplexer*	*Up-Down counter*	*Design of Accumulator Unit*	*Pipeline Processing: Parallel Processing*
	SLO-2	*NAND and NOR implementation*	*demultiplexer*	*Mealy and Moore model*	*Design of Accumulator Unit*	*Parallel Processing*
S 9-10	SLO-1 SLO-2	*Lab 2: To study and perform about NAND and NOR as a universal gates.*	*Lab 5: To design 3-bit odd/even parity generator and checker.*	*Lab 8: To realize Boolean functions using multiplexer.*	*Lab 11: To study universal shift register.*	*Lab 14 : Model Practical Examination*
S-11	SLO-1	*Karnaugh map simplification*	*Implementation of combinational circuit using decoder, encoder, multiplexer, demultiplexer.*	*Synchronous (Clocked) sequential circuits*	*Programming The Basic Computer : Introduction, Machine Language*	*Pipelining*
	SLO-2	*Problems on Karnaugh map simplification*	*Implementation of combinational circuit using decoder, encoder, multiplexer, demultiplexer.*	*Synchronous (Clocked) sequential circuits*	*Assembly Language, the Assembler*	*Pipelining*
S-12	SLO-1	*Problems on Karnaugh map simplification*	*Magnitude comparator*	*Synchronous (Clocked) sequential circuits*	*Program loops*	*Arithmetic Pipeline*
	SLO-2	*Quine McCluskey or tabulation method*	*Magnitude comparator*	*Analyze and design synchronous sequential circuits*	*Programming Arithmetic and logic operations.*	*Arithmetic Pipeline*
S-13	SLO-1	*Problems on Quine McCluskey or Tabulation method*	*Parity generator (even parity)*	*State reduction*	*Subroutines.*	*Instruction Pipeline*
	SLO-2	*Problems on Tabulation method*	*Odd parity generator*	*State assignment*	*I-O Programming*	*Instruction Pipeline, RISC pipeline*
S 14-15	SLO-1 SLO-2	*Lab 3: To study and perform about Half Adder and full Adder.*	*Lab 6: To design and implement circuit that converts binary code to gray code and gray to binary code.*	*Lab 9: To study and perform about R-S and D flip flop.*	*Lab 12: Design and implementation of Asynchronous Counters*	*Lab 15 : University Practical Exam*

Learning Resources	1. Morris Mano M, Michael D. Ciletti, Digital Design with an Introduction to the Verilog HDL, 5th ed., Pearson Education, 2014 2. M. Morris Mano Computer System Architecture 3rd edition, Pearson Education ,2012	3. Andrew S. Tanebaum , Structured Computer Organization., 6h edition, Pearson Education, 2013. 4. Hayes, J.P., "Computer Architecture and Organization", 5th Edition, Tata Mc-Graw Hill, 2005.

Learning Assessment											
	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
Level 2	Apply Analyze	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
Level 3	Evaluate Create	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Total	100 %		100 %		100 %		100 %		100 %	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*Dr. Damodar Panigrahy, Assistant Professor, Dept of ECE*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	

ACADEMIC CURRICULA

Professional Core Courses

ELECTRONICS AND COMPUTER ENGINEERING

Regulations - 2018

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)
Kattankulathur, Kancheepuram, Tamil Nadu, India

Course Code	18ECC202J	Course Name	LINEAR INTEGRATED CIRCUITS	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*18ECC102J or 18ECC211J*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	Data Book / Codes/Standards		*Nil*	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	Learning		
		1	2	3
CLR-1 :	*Study the basic principles, configurations and practical limitations of op-amp*			
CLR-2 :	*Understand the various linear and non-linear applications of op-amp*			
CLR-3 :	*Understand the operation and analysis of op-amp oscillators, single chip oscillators and frequency generators*			
CLR-4 :	*Identify the active filter types, filter response characteristics, filter parameters and IC voltage regulators.*			
CLR-5 :	*Gain knowledge on data converter terminology, its performance parameters, and various circuit arrangements for A/D and D/A conversions.*			
CLR-6 :	*Gain hands-on experience to put theoretical concepts learned in the course to practice.*			

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLO-1 :	*Infer the DC and AC characteristics of operational amplifiers and its effect on output and their compensation techniques*	*3*	*80*	*70*
CLO-2 :	*Elucidate and design the linear and non-linear applications of an opamp and special application ICs*	*3*	*85*	*75*
CLO-3 :	*Explain and compare the working of multivibrators using special application IC 555 and general purpose opamp*	*3*	*75*	*70*
CLO-4 :	*Classify and comprehend the working principle of data converters and active filters*	*3*	*85*	*80*
CLO-5 :	*Illustrate the function of application specific ICs such as Voltage regulators, PLL and its application in communication*	*3*	*85*	*75*
CLO-6 :	*Analyze and design electronic circuits and systems using linear ICs, and take measurement of various analog circuits to compare experimental results in the laboratory with theoretical analysis*	*3*	*85*	*75*

Program Learning Outcomes (PLO)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO–1	PSO – 2:	PSO – 3:
CLO-1	*H*	*M*	*H*	-	-	-	-	-	-	-	-	-	-	-	-
CLO-2	*M*	*M*	*H*	-	-	-	-	-	-	-	-	-	-	-	-
CLO-3	*L*	*M*	*H*	-	-	-	-	-	-	-	-	-	-	-	-
CLO-4	*L*	*M*	*H*	-	-	-	-	-	-	-	-	-	-	-	-
CLO-5	*L*	*M*	*H*	-	-	-	-	-	-	-	-	-	*M*	-	*H*
CLO-6		*H*	*H*	-	*M*	-	-	-	*M*	-	-	-	*H*	*L*	-

Module		1	2	3	4	5
Duration (hour)		15	15	15	15	15
S-1	SLO-1	*Op-amp symbol, terminals, packages*	*Basic op-amp circuits: Inverting & Non-inverting voltage amplifiers*	*Waveform Generators: Sine-wave Generators - Design*	*Filters: Comparison between Passive and Active Networks*	*Digital to Analog Conversion: DAC Specifications*
	SLO-2	*Op-amp-Specifications*	*Voltage follower*	*Implementation & Solving problems*	*Active Network Design*	*Solving problems*
S-2	SLO-1	*Block diagram Representation of op-amp*	*Summing, scaling & averaging amplifiers,*	*Square Wave generators- Design*	*Filter Approximations*	*Weighted Resistor DAC*
	SLO-2	*Ideal op-amp & practical op-amp - Open loop & closed loop configurations*	*AC amplifiers*	*Implementation & Solving problems*	*Design of LPF & Solving problems*	*Solving problems*
S-3	SLO-1	*DC performance characteristics of op-amp*	*Linear Applications: Instrumentation Amplifiers*	*Triangle wave generators*	*Design of HPF & Solving problems*	*R-2R Ladder DAC*
	SLO-2	*Solving Problems*	*Instrumentation Amplifiers, Solving Problems*	*Saw-tooth Wave generators.*	*Design of BPF& Solving problems*	*Solving problems*
S 4-5	SLO-1 / SLO-2	*Lab-1:Basic op-amp circuits*	*Lab 4: Comparators*	*Lab 7: Waveform generators: using op-amp & 555 Timer*	*Lab 10: Design of LPF, HPF, BPF and Band Reject Filters*	*Lab 13: Flash Type ADC*
S-6	SLO-1	*AC performance characteristics of op-amp*	*V-to-I Converters*	*IC 555 Timer: Circuit schematic*	*Design of Band Reject Filters*	*Inverted R-2R Ladder DAC*
	SLO-2	*Solving Problems*	*I-to-V converters*	*Operation and its applications*	*Solving problems*	*Monolithic DAC*
S-7	SLO-1	*Frequency response*	*Differentiators*	*IC 555 Timer: Monostable operation*	*State Variable Filters – All Pass Filters,*	*Analog to Digital conversion: ADC specifications*
	SLO-2	*Frequency response*	*Integrators*	*Applications & Solving problems*	*Solving problems*	*Solving problems*

Module		1	2	3	4	5
Duration (hour)		15	15	15	15	15
S-8	SLO-1	*Frequency compensation*	*Non-linear Applications: Precision Rectifiers*	*IC 555 Timer: Astable operation*	*Switched Capacitor Filters.*	*Ramp Type ADC*
	SLO-2	*Frequency compensation*	*Wave Shaping Circuits (Clipper and Clampers)*	*Applications & Solving problems*	*Solving problems*	*Solving problems*
S 9-10	SLO-1	*Lab 2: Integrators and Differentiators*	*Lab 5: Wave shaping circuits*	*Lab 8: Waveform generators: using op-amp & 555 Timer*	*Lab 11: IC Voltage regulators*	*Lab 14: Simulation experiments using EDA tools*
	SLO-2					
S-11	SLO-1	*Basic op-amp internal schematic*	*Log and Antilog Amplifiers,*	*PLL: Operation of the Basic PLL*	*Voltage Regulators: Basics of Voltage Regulator*	*Successive Approximation ADC*
	SLO-2	*operations of blocks*	*Analog voltage multiplier circuit and its applications,*	*Closed loop analysis of PLL*	*Specifications and characteristic parameters*	*Solving problems*
S-12	SLO-1	*Basic op-amp internal schematic*	*Operational Trans-Conductance Amplifier (OTA)*	*Voltage Controlled Oscillator*	*Linear Voltage Regulators using Op-amp,*	*Dual Slope ADC*
	SLO-2	*operations of blocks*	*Comparators : operation*	*Solving problems*	*IC Regulators (78xx, 79xx, LM 317, LM 337, 723),*	*Flash Type ADC,*
S-13	SLO-1	*Review of data sheet of an op-amp.*	*Comparators applications*	*PLL applications*	*Switching Regulators -operation*	*Solving problems on Flash Type ADC,*
	SLO-2	*Solving Problems*	*Sample and Hold circuit.*	*Solving problems*	*Types*	*Monolithic ADC*
S 14-15	SLO-1	*Lab 3: Rectifiers*	*Lab 6: Waveform generators: using op-amp & 555 Timer*	*Lab 9: Design of LPF, HPF, BPF and Band Reject Filters*	*Lab 12: R-2R ladder DAC*	*Lab 15: Simulation experiments using EDA tools*
	SLO-2					

Learning Resources	1. *Ramakant A. Gayakwad, Op-Amps and Linear Integrated Circuits, 4th ed., Prentice Hall, 2000* 2. *David A. Bell, Operational Amplifiers and Linear ICs, 3rd ed., OUP, 2013* 3. *Roy Choudhury, Shail Jain, Linear Integrated Circuits, 4th ed., New Age International Publishers, 2014* 4. *Robert F. Coughlin, Frederick F. Driscoll, Operational-Amplifiers and Linear Integrated Circuits, 6th ed., Prentice Hall, 2001* 5. *Sergio Franco, Design with operational amplifier and analog integrated circuits, McGraw Hill, 1997*	6. *LABORATORY MANUAL, Department of ECE, SRM University* 7. *David A Bell, Laboratory Manual for Operational Amplifiers & Linear ICs, 2nd ed., D.A. Bell, 2001* 8. *David La Lond, Experiments in Principles of Electronic Devices and Circuits, Delmar Publishers, 1993* 9. *Muhammed H Rashid, Introduction to PSpice using OrCAD for circuits and electronics, 3rd ed., Pearson, 2004* 10. *L. K. Maheshwari, M. M. S. Anand, Laboratory Experiments and PSPICE Simulations in Analog Electronics, PHI, 2006*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember / Understand	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
Level 2	Apply / Analyze	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
Level 3	Evaluate / Create	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Total	100 %		100 %		100 %		100 %		-	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Mr. Manikandan AVM, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Dr. M. Sangeetha, SRMIST*

Course Code	18CSC203J	Course Name	COMPUTER ORGANIZATION AND ARCHITECTURE	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Computer Science and Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
CLR-1 :	Utilize the functional units of a computer	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-2 :	Analyze the functions of arithmetic Units like adders, multipliers etc.			
CLR-3 :	Understand the concepts of Pipelining and basic processing units			
CLR-4 :	Study about parallel processing and performance considerations.			
CLR-5 :	Have a detailed study on Input-Output organization and Memory Systems.			
CLR-6 :	Simulate simple fundamental units like half adder, full adder etc			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	Identify the computer hardware and how software interacts with computer hardware	2	80	70	H	H	-	-	-	-	-	-	M	L	-	M	-	-	-
CLO-2 :	Apply Boolean algebra as related to designing computer logic, through simple combinational and sequential logic circuits	3	85	75	H	H	H	-	H	-	-	-	M	L	-	M	-	-	-
CLO-3 :	Analyze the detailed operation of Basic Processing units and the performance of Pipelining	2	75	70	H	H	H	H	-	-	-	-	M	L	-	M	-	-	-
CLO-4 :	Analyze concepts of parallelism and multi-core processors.	3	85	80	H	-	-	H	-	-	-	-	M	L	-	M	-	-	-
CLO-5 :	Identify the memory technologies, input-output systems and evaluate the performance of memory system	3	85	75	H	-	H	H	-	-	-	-	M	L	-	M	-	-	-
CLO-6 :	Identify the computer hardware, software and its interactions	3	85	75	H	H	H	H	H	-	-	-	M	L	-	M	-	-	-

Module		1	2	3	4	5
Duration (hour)		15	15	15	15	15
S-1	SLO-1	Functional Units of a computer	Addition and subtraction of Signed numbers	Fundamental concepts of basic processing unit	Parallelism	Memory systems -Basic Concepts
	SLO-2	Operational concepts	Problem solving	Performing ALU operation	Need, types of Parallelism	Memory hierarchy
S-2	SLO-1	Bus structures	Design of fast adders	Execution of complete instruction, Branch instruction	applications of Parallelism	Memory technologies
	SLO-2	Memory locations and addresses	Ripple carry adder and Carry look ahead adder	Multiple bus organization	Parallelism in Software	RAM, Semiconductor RAM
S-3	SLO-1	Memory operations	Multiplication of positive numbers	Hardwired control	Instruction level parallelism	ROM,Types
	SLO-2	Memory operations	Problem Solving	Generation of control signals	Data level parallelism	Speed,size cost
S 4-5	SLO-1	Lab 1: To recognize various components of PC-Input Output systems Processing and Memory units	Lab4:Study of TASM Addition and Subtraction of 8-bit number	Lab-7: Design of Half Adder Design of Full Adder	Lab-10: Study of Array Multiplier Design of Array Multiplier	Lab-13: Study of Carry Save Multiplication Program to carry out Carry Save Multiplication
	SLO-2					
S-6	SLO-1	Instructions, Instruction sequencing	Signed operand multiplication	Micro-programmed control-	Challenges in parallel processing	Cache memory
	SLO-2	Addressing modes	Problem solving	Microinstruction	Architectures of Parallel Systems - Flynn's classification	Mapping Functions
S-7	SLO-1	Problem solving	Fast multiplication- Bit pair recoding of Multipliers	Micro-program Sequencing	SISD,SIMD	Replacement Algorithms
	SLO-2	Introduction to Microprocessor	Problem Solving	Micro instruction with Next address field	MIMD, MISD	Problem Solving

Module		1	2	3	4	5
Duration (hour)		15	15	15	15	15
S-8	SLO-1	*Introduction to Assembly language*	*Carry Save Addition of summands*	*Basic concepts of pipelining*	*Hardware multithreading*	*Virtual Memory*
	SLO-2	*Writing of assembly language programming*	*Problem Solving*	*Pipeline Performance*	*Coarse Grain parallelism, Fine Grain parallelism*	*Performance considerations of various memories*
S 9-10	SLO-1	*Lab-2:To understand how different components of PC are connected to work properly Assembling of System Components*	*Lab 5: Addition of 16-bit number Subtraction of 16-bit number*	*Lab-8: Study of Ripple Carry Adder Design of Ripple Carry Adder*	*Lab-11: Study of Booth Algorithm*	*Lab-14: Understanding Processing unit Design of primitive processing unit*
	SLO-2					
S-11	SLO-1	*ARM Processor: The thumb instruction se*	*Integer division – Restoring Division*	*Pipeline Hazards-Data hazards*	*Uni-processor and Multiprocessors*	*Input Output Organization*
	SLO-2	*Processor and CPU cores*	*Solving Problems*	*Methods to overcome Data hazards*	*Multi-core processors*	*Need for Input output devices*
S-12	SLO-1	*Instruction Encoding format*	*Non Restoring Division*	*Instruction Hazards*	*Multi-core processors*	*Memory mapped IO*
	SLO-2	*Memory load and Store instruction in ARM*	*Solving Problems*	*Hazards on conditional and Unconditional Branching*	*Memory in Multiprocessor Systems*	*Program controlled IO*
S-13	SLO-1	*Basics of IO operations.*	*Floating point numbers and operations*	*Control hazards*	*Cache Coherency in Multiprocessor Systems*	*Interrupts-Hardware, Enabling and Disabling Interrupts*
	SLO-2	*Basics of IO operations.*	*Solving Problems*	*Influence of hazards on instruction sets*	*MESI protocol for Multiprocessor Systems*	*Handling multiple Devices*
S 14-15	SLO-1	*Lab -3To understand how different components of PC are connected to work properly Disassembling of System Components*	*Lab-6: Multiplication of 8-bit number Factorial of a given number*	*Lab-9: Study of Carry Look-ahead Adder Design of Carry Look-ahead Adder*	*Lab-12: Program to carry out Booth Algorithm*	*Lab-15: Understanding Pipeline concepts Design of basic pipeline.*
	SLO-2					

Learning Resources	1. *Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5th ed., McGraw-Hill, 2015* 2. *Kai Hwang, Faye A. Briggs, Computer Architecture and Parallel Processing", 3rd ed., McGraw Hill, 2016* 3. *Ghosh T. K., Computer Organization and Architecture, 3rd ed., Tata McGraw-Hill, 2011* 4. *P. Hayes, Computer Architecture and Organization, 3rd ed., McGraw Hill, 2015.*	5. *William Stallings, Computer Organization and Architecture – Designing for Performance, 10th ed., Pearson Education, 2015* 6. *David A. Patterson and John L. Hennessy Computer Organization and Design - A Hardware software interface, 5th ed., Morgan Kaufmann,2014*

Learning Assessment												
	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Understand										
Level 2	Apply	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
	Analyze										
Level 3	Evaluate	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Create										
	Total	100 %		100 %		100 %		100 %		-	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. T. V. Sankar, HCL Technologies Ltd, Chennai, sankar_t@hcl.com	*1. Prof. A.P. Shanthi, ANNA University Chennai, a.p.shanthi@cs.annauniv.edu*	*1.Dr. V. Ganapathy, SRMIST* *2. Dr. C. Malathy, SRMIST* *3. Mrs M.S.Abirami, SRMIST*

Course Code	18CSC303J	Course Name	DATABASE MANAGEMENT SYSTEMS	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Computer Science and Engineering	Data Book / Codes/Standards		Nil	

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
CLR-1 :	Understand the fundamentals of Database Management Systems, Architecture and Languages	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-2 :	Conceive the database design process through ER Model and Relational Model			
CLR-3 :	Design Logical Database Schema and mapping it to implementation level schema through Database Language Features			
CLR-4 :	Familiarize queries using Structure Query Language (SQL) and PL/SQL			
CLR-5 :	Familiarize the Improvement of the database design using normalization criteria and optimize queries			
CLR-6 :	Understand the practical problems of concurrency control and gain knowledge about failures and recovery			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Program Learning Outcomes (PLO)														
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
					Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	Acquire the knowledge on DBMS Architecture and Languages	3	80	70	H	M	L	L	-	-	-	-	L	L	L	H	-	-	-
CLO-2 :	Apply the fundamentals of data models to model an application's data requirements using conceptual modeling tools like ER diagrams	3	85	75	H	H	H	H	H	-	-	-	H	H	H	H	-	-	-
CLO-3 :	Apply the method to convert the ER model to a database schemas based on the conceptual relational model	3	75	70	H	H	H	H	H	-	-	-	H	H	H	H	-	-	-
CLO-4 :	Apply the knowledge to create, store and retrieve data using Structure Query Language (SQL) and PL/SQL	3	85	80	H	H	H	H	H	-	-	-	H	H	H	H	-	-	-
CLO-5 :	Apply the knowledge to improve database design using various normalization criteria and optimize queries	3	85	75	H	H	L	M	L	-	-	-	M	M	M	L	-	-	-
CLO-6 :	Appreciate the fundamental concepts of transaction processing- concurrency control techniques and recovery procedures	3	85	75	H	H	L	H	L	-	-	-	H	L	L	L	-	-	-

Module		1	2	3	4	5
Duration (hour)		15	15	15	15	15
S-1	SLO-1	What is Database Management System	Database Design	Basics of SQL-DDL,DML,DCL,TCL	Relational Algebra – Fundamental Operators and syntax, relational algebra queries, Tuple relational calculus	Transaction concepts, properties of transactions, serializability of transactions, testing for serializability, System recovery,
	SLO-2	Advantage of DBMS over File Processing System	Design process	Structure Creation, alternation		
S-2	SLO-1	Introduction and applications of DBMS	Entity Relation Model	Defining Constraints-Primary Key, Foreign Key, Unique, not null, check, IN operator		
	SLO-2	Purpose of database system				
S-3	SLO-1	Views of data	ER diagram	Functions-aggregation functions	Pitfalls in Relational database, Decomposing bad schema	Concurrency Control
	SLO-2			Built-in Functions-numeric, date, string functions, string functions, Set operations,	Functional Dependency – definition, trivial and non-trivial FD	
S 4-5	SLO-1	Lab 1: SQL Data Definition Language Commands on sample exercise	Lab4 : Inbuilt functions in SQL on sample exercise.	Lab 7 : Join Queries on sample exercise. * Frame and execute the appropriate DDL,DML,DCL,TCL for the project	Lab10: PL/SQL Procedures on sample exercise. * Frame and execute the appropriate Join Queries for the project	Lab 13: PL/SQL Exception Handling * Frame and execute the appropriate PL/SQL Procedures and Functions for the project
	SLO-2	* The abstract of the project to construct database must be framed				
S-6	SLO-1	Database system Architecture	Keys , Attributes and Constraints	Sub Queries, correlated sub queries	closure of FD set , closure of attributes irreducible set of FD	Two- Phase Commit protocol, Recovery and Atomicity
	SLO-2					
S-7	SLO-1	Data Independence	Mapping Cardinality	Nested Queries, Views and its Types	Normalization – 1Nf, 2NF, 3NF,	Log-based recovery

Module		1	2	3	4	5
Duration (hour)		15	15	15	15	15
	SLO-2					
S-8	SLO-1	*The evolution of Data Models*	*Extended ER - Generalization, Specialization and Aggregation*	*Transaction Control Commands Commit, Rollback, Savepoint*	*Decomposition using FD- dependency preservation,*	*concurrent executions of transactions and related problems*
	SLO-2					
S 9-10	SLO-1	*Lab 2: SQL Data Manipulation Language Commands * Identification of project Modules and functionality*	*Lab 5: Construct a ER Model for the application to be constructed to a Database*	*Lab 8: Set Operators & Views.* Frame and execute the appropriate In- Built functions for the project*	*Lab 11: PL/SQL Functions * Frame and execute the appropriate Set Operators & Views for the project*	*Lab 14: PL/SQL Trigger * Frame and execute the appropriate PL/SQL Cursors and Exceptional Handling for the project*
	SLO-2					
S-11	SLO-1	*Degrees of Data Abstraction*	*ER Diagram Issues Weak Entity*	*PL/SQL Concepts- Cursors*	*BCNF*	*Locking mechanism, solution to concurrency related problems*
	SLO-2					
S-12	SLO-1	*Database Users and DBA*	*Relational Model*	*Stored Procedure, Functions Triggers and Exceptional Handling*	*Multi- valued dependency, 4NF*	*Deadlock*
	SLO-2					
S-13	SLO-1	*Database Languages*	*Conversion of ER to Relational Table*	*Query Processing*	*Join dependency and 5NF*	*two-phase locking protocol, Isolation, Intentlocking*
	SLO-2					
S 14-15	SLO-1	*Lab 3: SQL Data Control Language Commands and Transaction control commands to the sample exercises * Identify the issues that can arise in a business perspective for the application*	*Lab 6: Nested Queries on sample exercise * Construction of Relational Table from the ER Diagram*	*Lab9: PL/SQL Conditional and Iterative Statements * Frame and execute the appropriate Nested Queries for the project*	*Lab 12: PL/SQL Cursors * Frame and execute the appropriate PL/SQL Conditional and Iterative Statements for the project*	*Lab 15 : * Frame and execute the appropriate PL/SQL Cursors and Exceptional Handling for the project * Demo of the project*
	SLO-2					

Learning Resources	1. *Abraham Silberschatz, Henry F. Korth, S. Sudharshan, Database System Concepts‖, Sixth Edition, Tata McGraw Hill,2011.* 2. *Ramez Elmasri, Shamkant B. Navathe, Fundamentals of Database Systems‖, Sixth Edition, Pearson Education,2011.* 3. *CJ Date,A Kannan,S Swamynathan, An Introduction to Database Systems, Eight Edition, Pearson Education,2006.*	4. *Martin Gruber, Understanding SQL, Sybex,1990* 5. *SharadMaheshwari,I ntroduction toSQLandPL/SQL,2d ed.,LaxmiPublications,2016.* 6. *RaghuramaKrishnan, JohannesGehrke, DatabaseManagementSystems, 3rdEdition, McGrawHill Education, 2003.*

Learning Assessment											
	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember / Understand	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
Level 2	Apply / Analyze	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
Level 3	Evaluate / Create	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Total	100 %		100 %		100 %		100 %		-	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Dr.Mariappan Vaithilingam, Engineering Leader *Amazon, dr.v.m@ieee.org*	*1. Prof. A.P. Shanthi, ANNA University Chennai, a.p.shanthi@cs.annauniv.edu*	*1. Ms. Sasi Rekha Sankar SRMIST*
2. Mr. Badinath, SDET, Amzon, sbadhrinath@gmail.com		*2. Mr.Elizer, SRMIST*

Course Code	18ECC311J	Course Name	MICROCONTROLLERS AND INTERFACING	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*18ECC212J*	Co-requisite Courses	*Nil*	Progressive Courses	*18ECC411J*
Course Offering Department	*Electronics and Communication Engineering*	Data Book / Codes/Standards		*Nil*	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	Learning		
		1	2	3
		Level of Thinking(Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	*Understand basic architecture of Intel 8086 microprocessor*			
CLR-2 :	*Learn 8051 microcontroller architecture and programming*			
CLR-3 :	*Interface a 8051 microcontroller to external input/output devices and perform input/output device programming in assembly*			
CLR-4 :	*Learn PIC microcontrollers (Programmable Interface Controllers)architecture and programming*			
CLR-5 :	*Interface a PIC microcontroller to external input/output devices and perform input/output device programming in assembly and Embedded C*			
CLR-6 :	*Provide strong foundation for designing real world applications using microcontrollers.*			

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*			
CLO-1 :	*Apply a basic concept of digital fundamentals to Microprocessor based personal computer system*	*1*	*60*	*70*
CLO-2 :	*Solve basic binary math operations using the microprocessor. / microcontroller*	*2*	*60*	*70*
CLO-3 :	*Demonstrate programming proficiency using the various addressing modes of the target microprocessor / microcontroller*	*3*	*60*	*70*
CLO-4 :	*Distinguish and analyze the properties of Microprocessors & Microcontrollers.*	*1*	*60*	*70*
CLO-5 :	*Illustrate their practical knowledge through laboratory experiments.*	*3*	*60*	*70*
CLO-6 :	*Design and interface of various peripheral chips with 8051 and PIC microcontroller*	*3*	*60*	*70*

Program Learning Outcomes (PLO)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO – 1	PSO – 2:	PSO – 3:
CLO-1 :		*H*			*L*										
CLO-2 :	*M*											*M*			
CLO-3 :		*M*	*H*		*H*										*L*
CLO-4 :		*M*										*H*			
CLO-5 :		*M*	*M*		*H*					*H*					*H*
CLO-6 :			*M*		*H*							*H*	*L*		*M*

Module		8051 Microcontroller	8051 peripherals	External peripheral interfacing	PIC microcontroller	PIC peripheral Interfacing
Duration (hour)		15	15	15	15	15
S-1	SLO-1	*Basics of Microprocessor*	*Comparisons between Microprocessors and microcontroller*	*LCD interfacing*	*PIC Architecture*	*Timers*
	SLO-2	*Basics of Microprocessor*	*8051 architecture, Pin functions*	*LCD interfacing*	*Registers organization*	*Interrupts*
S-2	SLO-1	*8086 registers and its functions*	*Memory organization*	*Keyboard interfacing*	*Memory organization*	*I/O ports*
	SLO-2	*8086 registers and its functions*	*Special Function Registers*	*Keyboard interfacing*	*Addressing modes*	*I2C bus*
S-3	SLO-1	*Instruction set of 8086 and simple programs*	*Instruction set-classification*	*Interfacing with external ROM*	*Instruction set: classification*	*LCD Interfacing*
	SLO-2	*Instruction set of 8086 and simple programs*	*Instruction set-addressing modes*	*Interfacing with external RAM*	*logical operation*	*LCD Interfacing*
S 4-5	SLO-1 SLO-2	*Lab 1: Program(s) to demonstrate data transfer operation, logical operation*	*Lab 4 : Program(s) – Basic Assembly language programming*	*Lab 7 :Interfacing LED / 7-segment / LCD displays/ keyboard*	*Lab 10: Program(s) to demonstrate logical operation*	*Lab 13: Interfacing LCD displays*
S-6	SLO-1	*Microprocessor bus, and signals*	*C Programming*	*ADC interfacing*	*Arithmetic operation*	*CCP modules*
	SLO-2	*Microprocessor bus, and signals*	*C Programming*	*ADC interfacing*	*Arithmetic operation*	*Flash and EPROMS*
S-7	SLO-1	*8086 Hardware architecture*	*I/O programming*	*DAC interfacing*	*branching*	*ADC Interfacing*
	SLO-2	*8086 Hardware architecture*	*I/O programming*	*DAC interfacing*	*branching*	*ADC Interfacing*
S-8	SLO-1	*Min mode system configuration*	*Timer programming*	*Sensor interfacing*	*time delay loop*	*DAC Interfacing*
	SLO-2	*Min mode system configuration*	*Timer programming*	*sensor interfacing*	*time delay loop*	*DAC Interfacing*

Module		8051 Microcontroller	8051 peripherals	External peripheral interfacing	PIC microcontroller	PIC peripheral Interfacing
Duration (hour)		15	15	15	15	15
S 9-10	SLO-1	*Lab 2: Program(s) to demonstrate arithmetic operation, shift operation*	*Lab 5: Program(s) Timer and counter*	*Lab 8: Interfacing ADC / DAC*	*Lab 11:Program(s) to demonstrate arithmetic operation*	*Lab 14 : Interfacing ADC / DAC*
	SLO-2					
S-11	SLO-1	*Max mode system configuration*	*Programming the 8051 to transfer data serially*	*Stepper motor interfacing*	*CALL*	*PIC timer programming*
	SLO-2	*Max mode system configuration*	*Programming the 8051 to receive data serially*	*Stepper motor interfacing*	*CALL*	*serial port programming*
S-12	SLO-1	*Advanced instructions,*	*8051 interrupts*	*DC motor interfacing*	*Programming in assembly*	*serial port programming*
	SLO-2	*Interrupt processing*	*Programming timer interrupts*	*DC motor interfacing*	*Programming in assembly*	*interrupt programming*
S-13	SLO-1	*HALT and WAIT for test states*	*Programming external hardware interrupts*	*DS12887 RTC interfacing*	*Programming in Embedded C*	*CCP programming*
	SLO-2	*DMA*	*Programming serial communication interrupts*	*DS12887 RTC interfacing*	*Programming in Embedded C*	*CCP programming*
S 14-15	SLO-1	*Lab 3: Program(s) to demonstrate decision making and looping operation*	*Lab 6: Program(s) – Serial communication using interrupt*	*Lab 9: Interfacing DC motor / stepper motor / servo motor*	*Lab 12:Program(s) to demonstrate CALL function*	*Lab 15 Program(s)Timer / Serial / Interrupt / CCP*
	SLO-2					

Learning Resources	1. *Krishna Kant, "Microprocessor and Microcontrollers, Architecture, Programming and System Design 8085, 8086, 8051, 8096", PHI, 2011.* 2. *Muhammad Ali Mazidi and Janice GillispieMazidi, "The 8051 - Microcontroller and Embedded systems", 7th Edition, Pearson Education, 2011.* 3. *Kenneth.J.Ayala, "8051 Microcontroller Architecture, Programming and Applications", 3rd edition, Thomson, 2007* 4. *Subrataghoshal " 8051 Microcontroller Internals Instructions ,Programming And Interfacing",2nd* 5. *Muhammad Ali Mazidi-Rolin-D-Muckinlay, Danny Caussey. "PIC MICROCONTROLLER AND EMBEDDED SYSTEM USING ASSEMBLY AND C FOR PIC 18"* 6. *John B Beatman. "DESIGN WITH PIC MICROCONTROLLERS" prentice Hall*

Learning Assessment											
	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Understand										
Level 2	Apply	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
	Analyze										
Level 3	Evaluate	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Create										
	Total	100 %		100 %		100 %		100 %		-	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*Dr. R. Manohari, Assistant Professor/ECE Dept*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	

Course Code	18ECC312T	Course Name	HARDWARE INTERFACING AND NETWORKING	Course Category	C	Professional Core	L	T	P	C
							3	0	0	3

Prerequisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes/ Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
CLR-1 :	CAN is widely used wired quasi real time network; it is essential to know about the standard, electrical requirements and signaling	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-2 :	CANopen is an industry standard application protocol used with CAN as underlying layer. It is used in many industrial controllers			
CLR-3 :	LIN bus, MODBUS, ProfiBus are widely used automotive networks; they also appear along with CAN.			
CLR-4 :	Flexray protocol is a latest sophisticated protocol standard for use in automotive control networks.			
CLR-5 :	Automotive Ethernet is an emerging networking in automotive applications. As an upcoming field it is essential to know about it and acquire basic skills.			
CLR-6 :	Understand the practical problems of concurrency control and gain knowledge about failures and recovery			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Program Learning Outcomes (PLO)														
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
					Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLO-1 :	Know and understand the CAN electrical, mechanical standards and signaling methods.	3	80	70	H														
CLO-2 :	Know and understand the CANopen protocol and will be able to analyze a typical application.	3	85	75	H	L	L												
CLO-3 :	Know and understand the LINbus, MODBUS, and Profibus protocols and the software interfacing	3	75	70	H	L	L												
CLO-4 :	Know and understand the Flexray protocol, its application using software interfaces in “C”, study corresponding support hardware chips	3	85	80	M	M	M											L	
CLO-5 :	Know and understand the Automotive Ethernet, its specific EMI, EMC requirements as applied to automotive environment, study corresponding support hardware chips.	3	85	75	M	M	M												L

Module		CAN bus Introduction	CAN and CANopen	Profibus, LINbus, MODBUS	Flexray Protocol	Automotive Ethernet
Duration (hour)		9	9	9	9	9
S-1	SLO-1	Introduction to CAN	CANopen overview	Profibus, network topologies	Introduction to Flexray	Intro to Automotive networking
	SLO-2	Electrical properties	CANopen overview	Profibus, network topologies	Bus architectures	Intro to Automotive networking
S-2	SLO-1	CAN signaling and data rates	Communication requirements for embedded networking	Network configuration	Protocol operation control context	Electrical requirements
	SLO-2	CAN signaling and data rates	Communication requirements for embedded networking	Network configuration	Operational overview	Electrical requirements
S-3	SLO-1	CAN data frame format	The object dictionary concept	Active components	Protocol operation control process	Network layer protocols. TCP/IP, UDP
	SLO-2	CAN data frame format	The object dictionary concept	Active components	Protocol operation control process	Network layer protocols. TCP/IP, UDP
S-4	SLO-1	Collision and arbitration	Communication entries	Passive components: connectors, cables, etc.	Behavior during normal operation	Ports and sockets
	SLO-2	Design examples	SDO and PDO	Testing of profibus	Coding and decoding	Ports and sockets
S-5	SLO-1	Error handling	SDO and PDO	LIN bus basics	Coding and decoding	Ports and sockets
	SLO-2	Error state diagram	PDO linking	LIN bus basics	Flexray Payload	Ports and sockets
S-6	SLO-1	CAN controller block diagram and working	Identifying objects COB-ID	LINbus protocol; master slave configuration	Wakeup and startup	Audio, video bridging

	SLO-2	*CAN controller block diagram and working*	*EDS and DCF*	*LINbus protocol; master slave configuration*	*Wakeup and startup*	*Audio, video bridging*
S-7	*SLO-1*	*Software for CAN controller interfacing*	*PDO communication*	*Basics of MODBUS*	*Clock synchronization*	*Audio/Video transport protocol - IEEE1722*
	SLO-2	*Software for CAN controller interfacing*	*PDO communication*	*Basics of MODBUS*	*Clock synchronization*	*Audio/Video transport protocol*
S-8	*SLO-1*	*CAN development tools*	*SDO communication*	*MODBUS protocol*	*Controller host interface*	*Measurement, calibration, diagnostics*
	SLO-2	*CAN development tools*	*SDO communication*	*MODBUS protocol*	*Controller host interface*	*Measurement, calibration, diagnostics*
S-9	*SLO-1*	*Demonstration of a typical CAN connection*	*Network management and safety critical features*	*MODBUS application*	*System parameters*	*Case studies*
	SLO-2	*Demonstration of a typical CAN connection*	*Network management and safety critical features*	*MODBUS application*	*System parameters*	*Case studies*

Learning Resources

1. *Olaf Pfeiffer, Andrew Ayre and Christian Keydel, "Embedded networking with CAN and CANopen", Copper hill Technologies Corporation, 2008.*
2. *Reference: www.can-cia.org"*
3. *SGS-Thompson, "Lin Application note AN1278", SGS - Thompson Ltd,. 2002.*
4. *Modbus-IDA, "MODBUS application protocol specification", Modbus-IDA, 2006.*
5. *Siemens, "Profibus network manual", Siemens manual, 2009.*
6. *Xiu Ji, "Profibus in practice: System Architecture and Design", CRC press, 2015.*
7. *Domnique parot, "Flexray and its applications: Real time multiplexed network", Wiley online library, 2012.*
8. *Charles M. Kozierok, Colt Correa, Robert B. Boatright, Jeffery Quesnelle, "Automotive Ethernet: A definitive guide", Intrepid Control Systems, 2014.*
9. *FlexRay Consortium, "FelxRay Communication system: Protocol specifications", FexRay Consortium, 2010.*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)				Final Examination (50% weightage)
		CLA – 1 (10%)	CLA – 2 (15%)	CLA – 3 (15%)	CLA – 4 (10%)#	
		Theory	Theory	Theory	Theory	Theory
Level 1	Remember	*40%*	*15%*	*15%*	*15%*	*15%*
	Understand					
Level 2	Apply	*40%*	*20%*	*20%*	*20%*	*20%*
	Analyze					
Level 3	Evaluate	*20%*	*15%*	*15%*	*15%*	*15%*
	Create					
	Total	100 %	100 %	100 %	100 %	100 %

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc.,

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anui Kumar, Bombardier Transportation, Ahmedabad, kumaranui.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University,*	*1. Prof. V. Nataraian SRMIST*
2.Dr.Mariappan Vaithilingam, Engineering Leader Amazon, dr.v.m@ieee.org	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	

Course Code	18ECC313J	Course Name	EMBEDDED HARDWARE AND OPERATING SYSTEMS	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*18ECC311J*	*Co-requisite Courses*	*Nil*	*Progressive Courses*	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	*Data Book / Codes/ Standards*	*Data catalog of MSP420 or any other M-CORTEX uP*		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	To understand the complex embedded system functions
CLR-2 :	To study high end processors used in embedded systems
CLR-3 :	To implement complex requirements with simple coding with operating systems.
CLR-4 :	To design processor-based functions with OS concepts
CLR 5:	To apply RTOS implementation on embedded systems design

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLO-1 :	Read and understand many microprocessor instructions and their use.	3	80	70
CLO-2 :	To implement and write code in assembly and C for embedded applications.	3	85	75
CLO-3 :	Understand the concepts and requirements of RTOS, in general basic OS principles.	3	75	70
CLO-4 :	The implementation and use of RTOS for embedded programs	3	85	80
CLO-5 :	Gain knowledge in related sample use cases.	3	85	75

Program Learning Outcomes (PLO)														
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
M														
	H	H		M				M						
				M										
		H	M	M				M					L	
L	L			L										M

Module		***Microprocessor and Microcontroller***	***I/O Programming***	***Thread Management***	***Time Management***	***Case Studies***
Duration (hour)		***15***	***15***	***15***	***15***	***15***
S-1	*SLO-1*	Cortex-M processor architecture	Parallel I/O programming	Introduction to RTOS	Spin-lock semaphore	Real time systems: Data acquisition system
	SLO-2	Cortex-M processor architecture	Sample programs	Introduction to RTOS	Cooperative scheduler	Approach
S-2	*SLO-1*	Cortex-M processor architecture	Interrupt processing basics	Concurrent programming	Blocked state	Performance metrics
	SLO-2	Cortex-M processor architecture	System tick; periodic interrupts	Thread fundamentals	Implementation	Examples
S-3	*SLO-1*	ARM Cortex assembly language - part1	Conditional execution	Shared resources and Critical sections	Thread rendezvous	Multilevel feedback queue
	SLO-2	Programming exercises	Conditional execution	Consumer producer problem	Example	priority scheduler
S 4-5	*SLO-1*	Practice: ARM Cortex assembly language with simulator	Practice: Interrupts and timers in C and assembly	Practice: Simple thread programming in RTOS	Practice: Two semaphore implementation	Practice: Priority based scheduling; threads and communications
	SLO-2	Practice: ARM Cortex assembly language with simulator	Practice: Interrupts and timers in C and assembly	Practice: Simple thread programming in RTOS	Practice: One semaphore implementation	Practice: Priority based scheduling; threads and communications
S-6	*SLO-1*	ARM Cortex assembly language - part2	UART programming	Switching threads	FIFO & Little's theorem	DMA / high speed interface
	SLO-2	Programming exercises	UART programming	Profiling the OS	FIFO & Little's theorem	DMA / high speed interface

S-7	*SLO-1*	ARM Cortex microcontroller interface standards	Digital signal time measurement	Semaphores and implementation	Three semaphore implementations	Solid state disk
	SLO-2	IDE software tools	Use of timers and compare, capture registers.	Operations on semaphores	Three semaphore implementations	Flash device driver
S-8	*SLO-1*	Embedded debugging tools in Keil IDE	SSI interface	Resource sharing	Kahn process networks	SD card interface
	SLO-2	Embedded debugging example with simulation	SSI interface	Conditional variable	Kahn process networks	SD card interface
S 9-10	SLO-1	Practice: C & assembly programming using Keil IDE and kit - I	Practice: Debugging hardware with target board	Practice: Multithreaded application in RTOS	Practice: Multithreaded application with communication.	Practice: Semaphore implementation experiment in RTOS
	SLO-2	Practice: C & assembly programming using Keil IDE and kit - I	Practice: Debugging hardware with target board	Practice: Multithreaded application in RTOS	Practice: Multithreaded application with communication.	Practice: Semaphore implementation experiment in RTOS
S-11	*SLO-1*	Memory management -1	SSI programming with interrupt	Thread communications	Thread sleeping	Communication systems with Ethernet
	SLO-2	Memory management -2	Analog I/O; A/D converter interfacing	Thread communications	Thread sleeping	Communication systems with ethernet
S-12	*SLO-1*	Embedded debugging tools in Keil IDE	Programming example	Process management	Deadlocks, monitors	Application layer protocols for embedded systems
	SLO-2	Embedded debugging example with simulation	Programming example	Process management	Deadlocks, monitors	Application layer protocols for embedded systems
S-13	*SLO-1*	Review class	OS considerations of I/O devices	Dynamic linking and loading	Fixed scheduling	CoAP, MQTT
	SLO-2	Review class	OS considerations of I/O devices	Dynamic linking and loading	Fixed scheduling	CoAP, MQTT
S 14-15	*SLO-1*	Practice: C & assembly programming using Keil IDE and kit – II	Practice: A/D interfacing	Practice: Program profiling	Practice: Priority based scheduling; threads and communications	Practice: Any application program using RTOS
	SLO-2	Practice: C & assembly programming using Keil IDE and kit – II	Practice: A/D interfacing	Practice: Program profiling	Practice: Priority based scheduling; threads and communications	Practice: Any application program using RTOS

Learning Resources	1. *Jonathan Valvano, "Real time operating systems for ARM Cortex-M Microcontrollers, Embedded systems - Volume 3", Jonathan Valvano, 2017.* 2. *Andrew Sloss et all, "ARM system developers guide", Elsevier, 2004.* 3. *Quing Li, "Real time techniques for embedded systems", CMP Books, 2003.*	4. *K.C. Wang, "Embedded and Real time operating systems", Springer, 2017.* 5. *www.arm.com, for ARM cortex M references*

Learning Assessment											
	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Understand										
Level 2	Apply	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
	Analyze										
Level 3	Evaluate	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Create										
	Total	100 %		100 %		100 %		100 %		-	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, Conf. Paper etc.,

Course Designers		
Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Prof. V. Natarajan, Professor, ECE Dept, SRMIST*
2.Dr.Mariappan Vaithilingam, Engineering Leader Amazon, dr.v.m@ieee.org	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	*2. Dr. Ruhan Bevi, Associate Professor/ECE*

Course Code	18ECC411J	Course Name	FPGA Based Embedded Systems	Course Category	C	Professional Core	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*18ECC203J or 18ECC212J*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	Data Book / Codes/ Standards	*Nil*		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	*Many high volume embedded systems need to be function specific*
CLR-2 :	*These systems have to be cost effective, with short development time.*
CLR-3 :	*FPGAs/PSoCs are cost effective solution for specific embedded modules and low-power designs.*
CLR-4 :	*Platform FPGAs will find future applications.*
CLR-5 :	*Designing systems with Platform FPGAs is a necessary skill.*
CLR-6 :	*Many high volume embedded systems need to be function specific*

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLR-1 :	*Micro controller subsystem understanding*	*2*	*80*	*50*	*M*														
CLR-2 :	*Understanding and designing with PSoCs*	*3*	*99*	*70*		*H*	*H*		*M*				*M*						
CLR-3 :	*Understanding of Platform FPGAs*	*2*	*80*	*70*					*M*										
CLR-4 :	*Understanding of FPGA architecture design*	*3*	*90*	*70*			*H*	*M*	*M*				*M*						
CLR-5 :	*Designing with Platform FPGAs (examples)*	*2*	*90*	*85*	*L*	*L*			*L*										*M*
CLR-6 :	*Micro controller subsystem understanding*	*2*	*80*	*50*	*M*														

Module		Microcontrollers and embedded systems	PSoC3/5	Platform FPGAs	System Design – I	System Design – II
Duration (hour)		15	15	15	15	15
S-1	SLO-1	*Embedded systems performance criteria - Interrupts*	*PSoC3/5 architecture overview*	*Design challenges, life cycle*	*Design quality: correctness, reliability, resilience.*	*Spatial design: Principles of parallelism*
	SLO-2	*Embedded systems performance criteria - Interrupts*	*PSoC3/5 architecture overview*	*Metrics: measures of success*	*Modules and interfaces*	*Granularity, degree of parallelism*
S-2	SLO-1	*Embedded systems performance criteria - DMA*	*PSoC3 architecture details and 8051 instructions*	*PLD basics*	*Abstraction and state,*	*Spatial organizations*
	SLO-2	*Latency and problems*	*PSoC3 architecture details and 8051 instructions*	*FPGA configurations*	*Cohesion and coupling and control flow graph*	*Spatial organizations*
S-3	SLO-1	*Embedded system subsystems: A/D conversion*	*PSoC C language*	*VHDL and Verilog intro*	*Origin of Platform FPGA Designs*	*Identifying parallelism*
	SLO-2	*Digital ports & its current capacity*	*Interrupt priority and nesting*	*VHDL and Verilog intro*	*Platform FPGA components*	*Ordering, dependence, uniform dependence vectors*
S 4 - 5	SLO-1	*Practice : Keil IDE – 8051 Simulation experiment*	*Practice: PSoC 8051 simulation program in C*	*Practice: VHDL and Verilog practice session*	*Practice: Creating IP core*	*Practice: Useful VHDL topics for spatial design*
	SLO-2	*Practice : Keil IDE – 8051 Simulation experiment*	*Practice: PSoC 8051 simulation program in C*	*Practice: VHDL and Verilog practice session*	*Practice: Creating IP core*	*Practice: Useful VHDL topics for spatial design*

Module		Microcontrollers and embedded systems	PSoC3/5	Platform FPGAs	System Design – I	System Design – II
Duration (hour)		15	15	15	15	15
S-6	SLO-1	*Introduction to other digital interfaces*	*The concept of memory and its connectivity to CPU*	*Xilinx Virtex 5 IDE*	*Adding to platform FPGA systems*	*Parallelism within FGPA hardware cores within FPGA designs*
	SLO-2	*Introduction to other digital interfaces*	*External memory access*	*Xilinx Virtex 5 IDE*	*Assembling custom compute cores*	*Parallelism within FGPA hardware cores within FPGA designs*
S-7	SLO-1	*Sensors and sensing principles. Optical, capacitive sensors*	*Memory access priority, Direct Memory Access*	*Slices and CLBs*	*Software design: root file system, cross-developmental tools*	*Managing bandwidth: Balancing*
	SLO-2	*Magnetic, RF sensors*	*Different DMA modes*	*Various slices in Virtex 5*	*Monitors and bootloaders*	*Managing bandwidth: Balancing*
S-8	SLO-1	*Other sensors*	*Clocking system: Internal master oscillator*	*Bit stream*	*Monitors and bootloaders*	*Khan process network*
	SLO-2	*Interfacing techniques*	*IMO, and sleep/wake up modes*	*Programming FPGA*	*Connecting the hardware to the base system.*	*Khan process network*
S 9 -10	SLO-1	*Practice: Embedded sensors and sensing*	*Practice: PSoC 8051 simulation program in C*	*Practice: Sample programming FPGA – I*	*Practice :Hardware Integration*	*Practice: On-chip memory access, FIFOs*
	SLO-2	*Practice: Embedded sensors and sensing*	*Practice: PSoC 8051 simulation program in C*	*Practice: Sample programming FPGA - I*	*Practice :Hardware Integration*	*Practice: On-chip memory access, FIFOs*
S-11	SLO-1	*Processing: Mathematical views.*	*Clock distribution*	*Spectrometer example using Xilinx IDE*	*Overview of partitioning platform*	*Platform FPGA bandwidth techniques*
	SLO-2	*Processing: Mathematical views.*	*Internal low speed clock*	*Spectrometer example using Xilinx IDE*	*Analytical solution to partitioning*	*Platform FPGA bandwidth techniques*
S-12	SLO-1	*Micro controller subsystems*	*Types of reset*	*Sample IP core design for digital logic*	*Resource considerations*	*On-chip, off-chip memory*
	SLO-2	*Micro controller subsystems*	*Interrupts and interrupt lines*	*Sample IP core design for digital logic*	*Analytical approach*	*Memory access techniques*
S-13	SLO-1	*Programmable logic and mixed signal design fundamentals*	*Clock distribution*	*Sample IP core design for digital logic*	*Transfer of state*	*Off chip memory access: I/O, DMA.*
	SLO-2	*Programmable logic and mixed signal design fundamentals*	*Power management: Internal regulators*	*Sample IP core design for digital logic*	*Practical issues: profiling issues*	*Bus and bus controller*
S 14-15	SLO-1	*Practice: Programmable logic design*	*Practice: PSoC 8051 simulation program in C*	*Practice: Sample programming FPGA – II*	*Practice: Building base systems*	*Practice: Block RAM, local link interface*
	SLO-2	*Practice: Programmable logic design*	*Practice: PSoC 8051 simulation program in C*	*Practice: Sample programming FPGA – II*	*Practice: Building base systems*	*Practice: Block RAM, local link interface*

Learning Resources	1. *Robert Ashby, "Designers guide to the Cypress PSoC", Cypress Semiconductors, 2005.* 2. *Edward H. Currie and David Van Ess, " PSoC3/5 Reference Book", Cypress Semiconductor, 2010.*	3. *Sass and Schmidt, "Embedded system design with Platform FPGAs", Morgan Kaufmann, 2010.* 4. A.Arockia Bazil Raj FPGA based embedded system developers guide , “CRC press 1st edition 2018”

Learning Assessment											
	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
Level 2	Apply Analyze	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*
Level 3	Evaluate Create	*10%*	*10%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
	Total	100 %		100 %		100 %		100 %		-	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, Conf. Paper etc.,

Course Designers		
Experts from Industry	*Experts from Higher Technical Institutions*	*Internal Experts*
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Prof. V. Natarajan, Professor, ECE Dept,SRMIST*
2.Dr.Mariappan Vaithilingam, Engineering Leader Amazon, dr.v.m@ieee.org	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	

Course Code	18ECC351T	Course Name	COMPREHENSION	Course Category	C	Professional Core	L	T	P	C
							0	1	0	1

Pre-requisite Courses	*NIL*	Co-requisite Courses	*NIL*	Progressive Courses	*NIL*
Course Offering Department	*Electronics and Communication Engineering*	Data Book / Codes/Standards		*Nil*	

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-1 :	*Acquire skills to solve real world problems in Analog and Digital Electronics (Discrete & IC)*			
CLR-2 :	*Acquire skills to solve real world problems in Data structures and Object Oriented Programming*			
CLR-3 :	*Acquire skills to solve real world problems in Data structures and Object Oriented Programming*			
CLR-4 :	*Acquire skills to solve real world problems in Data structures and Object Oriented Programming*			
CLR-5 :	*Acquire skills to solve real world problems in FPGA Design based embedded systems*			
CLR-6 :	*Acquire skills to solve real world problems in Operating Systems and Embedded Hardware*			

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*			
CLO-1 :	*Practice and gain confidence and competence to solve problems in Analog and Digital Electronics (Discrete & IC)*	*3*	*85*	*80*
CLO-2 :	*Practice and gain confidence and competence to solve problems in Data structures and Object Oriented Programming*	*3*	*85*	*80*
CLO-3 :	*Practice and gain confidence and competence to solve problems in Computer architecture and Data base Management*	*3*	*85*	*80*
CLO-4 :	*Practice and gain confidence and competence to solve problems in Microprocessor, Microcontrollers and Interfacing*	*3*	*85*	*80*
CLO-5 :	*Practice and gain confidence and competence to solve problems in FPGA Design based embedded systems*	*3*	*85*	*80*
CLO-6 :	*Practice and gain confidence and competence to solve problems in Operating Systems and Embedded Hardware*	*3*	*85*	*80*

Program Learning Outcomes (PLO)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design,	Modern Tool Usage	Society & Culture	Environment &	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO - 3
CLO-1 :	*H*	*H*	*H*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*M*	*L*	*M*
CLO-2 :	*H*	*H*	*M*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*M*	*M*	*M*
CLO-3 :	*H*	*H*	*M*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*M*	*L*	*M*
CLO-4 :	*H*	*H*	*M*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*M*	*M*	*M*
CLO-5 :	*H*	*H*	*H*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*M*	*L*	*M*
CLO-6 :	*H*	*H*	*M*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*M*	*M*	*M*

Duration (hour)		3	3	3	3	3
S-1	SLO-1	*Tutorial on Semiconductor Devices*	*Tutorial on Signals and Systems*	*Tutorial on Data Structures*	*Tutorial on Microcontrollers & Interfacing*	*Tutorial on FPGA based embedded system design*
	SLO-2	*Problem Solving*	*Problem Solving*	*Problem Solving*	*Problem Solving*	*Problem Solving*
S-2	SLO-1	*Tutorial on Digital Electronics*	*Tutorial on Computer Systems*	*Tutorial on Object Oriented Programming*	*Tutorial on Computer Architecture*	*Model Test*
	SLO-2	*Problem Solving*	*Problem Solving*	*Problem Solving*	*Problem Solving*	*Model Test*
S-3	SLO-1	*Tutorial on Integrated Circuits*	*Tutorial on Computer System Design*	*Tutorial on Database Management*	*Tutorial on Operating Systems*	*Final Test*
	SLO-2	*Problem Solving*	*Problem Solving*	*Problem Solving*	*Problem Solving*	*Final Test*

Learning Resources	
	1. *Rahul Nigam, "Basic Electronics Interview Questions and Answers" Amazon Asia-Pacific Holdings Private Limited,ebook,2019*
	2. *Hwei Hsu , "Schaum's Outline of Signals and Systems, 3rd Edition (Schaum's Outlines)", 2013*
	3. *Arshad Iqbal, "Computer Fundamentals MCQs", ebook,Amazon Asia-Pacific Holdings Private Limited,2019*
	4. *Samantha Abraham, "MCQs in Computer Organization and Architecture", Amazon Asia-Pacific Holdings Private Limited, 2019*

Learning Assessment											
	Bloom's Level of Thinking	Continuous Learning Assessment (100% weightage)								Final Examination	
		CLA – 1 (20%)		CLA – 2 (30%)		CLA – 3 (30%)		CLA – 4 (20%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	*40%*	-	*30%*	-	*30%*	-	*30%*	-	-	-
	Understand										
Level 2	Apply	*40%*	-	*40%*	-	*40%*	-	*40%*	-	-	-
	Analyze										
Level 3	Evaluate	*20%*	-	*30%*	-	*30%*	-	*30%*	-	-	-
	Create										
	Total	100 %		100 %		100 %		100 %		-	

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2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Dr. Venkatesan, Sr. Scientist, NIOT, Chennai, venkat@niot.res.in*	