ACADEMIC CURRICULA

POST GRADUATE DEGREE PROGRAMMES

Master of Technology

(Choice Based Flexible Credit System)

Regulations 2021

Volume – 24
Syllabi for School of Electrical Engineering Programmes

Professional Core and Elective Courses

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Chengalpattu District 603203, Tamil Nadu, India

ACADEMIC CURRICULA

Embedded System Technology

Professional Core Courses

Regulations 2021

SRM INSTITUTE OF SCIENCE & TECHNOLOGY
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SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Chengalpattu District 603203, Tamil Nadu, India

Course Code	21ECC501J	Course Name	EMBEDDED SYSTEM ARCHITECTURE	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*define the ARM core architecture and its language structure and programming.*
CLR-2:	*outline the various I/O ports, peripherals and their configuration.*
CLR-3:	*organize the concepts of embedded system development like linkers and the linking process.*
CLR-4:	*interpret tasks, task operations and their synchronization*
CLR-5:	*identify the I/O peripherals of embedded systems and system clocks*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*recall Cortex M processor instruction set code in assembly and their use.*	2		3
CO-2:	*demonstrate the Cortex-M processor features for embedded applications.*	2		3
CO-3:	*interpret the concepts and requirements of RTOS, in general basic OS principles.*	2		3
CO-4:	*apply the implementation and use of tasks, task operations for embedded programs*		2	3
CO-5:	*distinguish the different IO peripherals and real-time clocks and system clocks*		2	3

Module-1 - Cortex-M processor Architecture	***15 Hour***
Cortex-M processor family, Advantages of the Cortex-M processors, Software development flow, Block diagram of the Cortex-M3 and Cortex-M4 processor, Architecture of Cortex-M processor, Programmer's model, Program status, Register, Memory system, Exceptions and interrupts, Debug. Reset and reset sequence, Assembly language syntax, Suffixes for Cortex-M Assembly Language, Instruction Set, Barrel shifter, Memory System, Connecting the processor to memory and peripherals, Memory system in a microcontroller *Practice: Basic practice of Cortex M microcontroller assembly language programs*	
Module-2 - Cortex-M Processor Features	***15 Hour***
Exceptions and Interrupts, Exception types, Interrupt management, Priority, Vector table and vector table relocation, Exception sequence, NVIC registers for interrupt control SCB registers for exception and interrupt control, Special registers for exception or interrupt masking, Exception sequences, Interrupt latency and exception handling optimization, Low power features, OS Support Features, Shadowed stack pointer, SVC exception, PendSV exception, Fault exceptions, Causes of faults. *Practice: Programming Cortex M processor for Interrupt processing*	
Module-3 - Embedded System Development	***15 Hour***
Basics Of Developing Embedded Systems, Linkers and the Linking Process, Executable and Linking Format, Mapping Executable Images into Target Embedded Systems, Mapping Executable Images, Embedded System Initialization, Target System Tools and Image Transfer, Target Boot Scenarios, Executing from ROM Using RAM for Data, Executing from RAM after Image Transfer from ROM, Executing from RAM after Image Transfer from Host, Target System Software Initialization Sequence, Real-Time Operating Systems, The Scheduler, Context switch, Scheduling Algorithms, Objects, Characteristics of an RTOS *Practice- Programming Cortex M processor for Serial communication*	
Module-4 – Peripheral Interfacing	***15 Hour***
UART Interface, Debugging hardware with Target board, SSI Interface, SSI programming with interrupt, Analog I/O, A/D converter interfacing, OS consideration of I/O, Solid state disk, Flash device driver, SD Card interface, Communication system with Ethernet. *Practice: Programming Cortex M processor for ADC, DAC interfacing*	

Module-5 – I/O Peripherals	***15 Hour***
Exceptions and Interrupts, Applications of Exceptions and Interrupts, Processing General Exceptions, The Nature of Spurious Interrupts, Timer and Timer Services Real-Time Clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routines, Implementing the Soft-Timer Handling Facility, Timing Wheels Soft Timers and Timer Related Operations, I/O Subsystem, Memory Management, Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory Management in Embedded Systems, Blocking vs. Non-Blocking Memory Functions, An Outside-In Approach to Decomposing Applications, Guidelines and Recommendations for Identifying Concurrency *Practice: Programming Cortex M processor for Timing and tasks*	

Learning Resources		
	1. *Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors," Third Edition, Newnes,2013.* 2. *Qing Li and Carolyn Yao, "Real-Time Concepts for Embedded Systems," CMP Books, 2003.*	3. *Jonathan Valvano, "Real time operating systems for ARM Cortex-M Microcontrollers, Embedded systems - Volume 3", 2017.* 4. *K.C. Wang, "Embedded and Real time operating systems", Springer, 2017.*

Learning Assessment								
	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	-	*20%*	*20%*	-
Level 2	*Understand*	*20%*	-	-	*20%*	*20%*	-
Level 3	*Apply*	*30%*	-	-	*30%*	*30%*	-
Level 4	*Analyze*	*30%*	-	-	*30%*	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. *Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com*	1. *Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	1. *Dr. J.Subhashini , SRMIST*
2. *Mr. Hariharan VS, Vice president-HR BP @ Edveon Technologies*	2. *Dr. R. Ramesh, Professor, EEE, Anna University, Chennai*	

Course Code	21ECC502J	Course Name	REAL TIME OPERATING SYSTEMS	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*summarize the basics of operating system*
CLR-2:	*acquire knowledge of process management*
CLR-3:	*outline the process synchronization and memory management*
CLR-4:	*infer scheduling algorithms*
CLR-5:	*inspect how Real Time operating system used in real time applications*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*recall the fundamentals of operating system*	*3*	*2*	*-*
CO-2:	*illustrate the process concepts and kernel structure*	*3*	*1*	*-*
CO-3:	*construct the process synchronization and memory management*	*2*	*3*	*-*
CO-4:	*analyze the design a scheduling algorithm*	*3*	*1*	*2*
CO-5:	*apply the knowledge to use and design RTOS*	*1*	*-*	*3*

Module-1 – Introduction to Real Time Operating System	***15 Hour***
Overview of Operating System, Fundamentals and keywords, structures, OS user view, system view, Interrupts, Storage structures, I/O structures, Single, Multi and clustered systems, Dual mode and multimode operation, Resource Management, Timers and I/O, virtualization and distributed systems, lists, stacks, Hash functions, computing environments, Building and Booting an operating system, operating system debugging, Queues, Trees. *Practice –Basics of Linux Operating System*	
Module-2 – Process Management	***15 Hour***
Process Management, Process scheduling, Message queues, Mailboxes, Pipes, Inter-Process Communication (IPC), IPC in shared memory message passing systems, threads and concurrency, Multithreading models, implicit threading, threading issues, Kernel Structure-Critical sections, tasks, task states, task scheduling, task control blocks, task management, time management, Device drivers. *Practice – System calls for Linux operating system and Shell programs*	
Module-3 – Process Synchronization and Memory Management	***15 Hour***
Synchronization tools, the critical section problem, Hardware support for synchronization, Mutex locks, Semaphores, semaphore usage and implementation, Monitors, implementation using semaphores, resuming processes within a monitor, Deadlocks, characterization, methods for handling, deadlock prevention, Deadlock avoidance, 'deadlock detection, Recovery from Deadlock, Memory management, main memory allocation, contiguous memory allocation, paging, structure of the page table, virtual memory, allocating kernel memory *Practice- Producer consumer problem using Semaphores, IPC using Shared Memory, Bankers Algorithm for Deadlock avoidance, Algorithm for deadlock detection, Memory allocation methods*	
Module-4 – Real Time Scheduling and Scheduling Algorithms	***15 Hour***
Uniprocessor scheduling , types of scheduling, pre-emptive and non-preemptive scheduling, dispatcher, scheduling algorithms-FCFS, Round robin scheduling, priority based scheduling, thread scheduling, multiprocessor scheduling, Real Time CPU scheduling, Rate monotonic scheduling, Earliest Deadline-First scheduling, POSIX Real-Time Scheduling, Fault tolerant scheduling, aperiodic scheduling, Schedulability problem: classification- schedulability test, Worst Case Execution Time (WCET), spring algorithm, Sporadic scheduling .	

Practice – CPU Scheduling Algorithms (Priority based scheduling, Round Robin Scheduling, First Come First Serve (FCFS) and shortest scheduling Algorithms)
Module-5 – RTOS and Case Studies ***15 Hour***
Introduction to POSIX, POSIX standards, Design of POSIX, RTOS-Tiny OS introduction, example application, Names and Program Structure, Basic Programming, component signatures, Interfaces, Component Implementation, Split phase interfaces, configurations, applications, Case Study-RTOS for Control Systems, Case Study-RTOS for Voice over IP *Practice - File organization techniques, Tiny OS*

Learning Resources	1. *Abraham Silberschatz, Peter Baer Galvin, Greg Gagne, Operating System Concepts, Tenth edition, Wiley, 2018* 2. *Jean J. Labrosse, The microC /OS-II The Real Time Kernel Optics, CMP Books, 2nd edition, 2011* 3. *C.M. Krishna and G.Shin, Real Time Systems, McGrraw-Hill International Edition, 2010(3rd Reprint)*	4. *Jim Cooling, "Real-Time Operating Systems Book 1: The Foundations", Lindtree Associates, 2018.* 5. *Donald A. Lewine, POSIX Programmer's Guide.1991.* 6. *Philip Levis, David Gay, Tiny OS Programming Cambridge University Press 2009*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 - Practice (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	-	*20%*	*20%*	-
Level 2	*Understand*	*30%*	-	-	*30%*	*30%*	-
Level 3	*Apply*	*30%*	-	-	*30%*	*30%*	-
Level 4	*Analyze*	*20%*	-	-	*20%*	*20%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. K.Vadivukkarasi, SRMIST*
2. Mr. Hariharan VS, Vice president-HR BP @ Edveon Technologies	*2. Dr. R. Ramesh, Professor EEE, Anna University, Guindy*	*2. Dr. A. RuhanBevi, SRMIST*

Course Code	21ECC503T	Course Name	EMBEDDED CONTROL SYSTEMS	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*identify the basic concept of embedded system.*
CLR-2:	*classify control system design for embedded applications.*
CLR-3:	*design optimal embedded models and learn the uncertainties.*
CLR-4:	*explain the basic controllers design and implementation.*
CLR-5:	*execute robust control and embedded control system for industrial applications.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*recall the architecture of embedded control system and controller area network.*	2		
CO-2:	*interpret linear and nonlinear control system models for embedded applications.*	2	3	
CO-3:	*analyze time domain and frequency domain systems and reduce uncertainties in system design.*	2	3	
CO-4:	*design various control elements by understanding pole-zero placement.*		2	3
CO-5:	*acquire knowledge in robust real time control systems with embedded safety precautions.*			3

Module-1 - Embedded System Basic Concepts	***9 Hour***
Introduction to embedded system, Embedded system model, Electric Power Level, Signal Processing Level, Communication Networks in Embedded Systems, Controller Area Network, CAN Communication Network, CAN Message Frames, CAN Message Frames, Error Detection and Signaling, CAN Controller Modes, CAN Implementations, Multi-tasking Embedded Control Systems, Introduction to RTOS, Planning Embedded System Development.	
Module-2 - Embedded Control System Design	***9 Hour***
Requirements for Control System Design, Identification of the System to Be Controlled, Control Device Specification, Control Device Design, Installation and Maintenance, Mathematical models for control, Models from Experimental Data, Linearization of Nonlinear Models, Control System's Characteristics, Disturbance Attenuation, Tracking, Sensitivity to Parameter Variations, Control System's Limitation, Relative stability, Performance Specifications for Linear Systems.	
Module-3 - System Identification and Model-Order Reduction	***9 Hour***
Model Building and Model Structures, Model Structures, Input Signal Design for System Identification Experiments, Requirements imposed on the input signal, Model Validation in Time Domain, Model Validation in Frequency Domain, Model-order reduction methods, Nominal Plant and Plant Uncertainties. Multiplicative Uncertainty Model, Additive Uncertainty Model, Practical Examples – System Identification, Brushless d.c. Drive's Identification, Identification of a Fuel Cell.	
Module- 4-Classical Controller Design	***9 Hour***
Controller Design Based on Pole-Zero Cancellation, Controller design deadbeat response, Controller Design Using the Root Locus Technique, Phase-Lead Controller Design Using the Root Locus, PID Controller Design, Ziegler-Nichols Tuning Formula, Chien- Hrones-Reswick Formula, Coefficient Diagram Method, Validation of the Control System, Representative Sample and Sample Size, Monte Carlo Simulation, Controller Design for Systems with Time Delays, Coefficient Diagram Method (CDM) for Systems with Time Delays, Handling Jitter in Networked Control System, Controller Design for Disturbance Rejection, Disturbance Observers, Two-Degree-of-Freedom Control Systems, Control System Design Verification and Validation.	
Module-5 – Fundamentals of Robust Control and Embedded Safety	***9 Hour***

Norms for Signals and Systems, Internal stability, Unstructured plant unstabilities, Robust Stability for different Uncertainty model, Performance and Robustness bound, Design for Robust bound, Performance Weighting Function Design for Tracking Control, Performance weighting function, Robust Controller Synthesis Problem, Controller Design Using Youla Parametrization, Controller Design Using Robust Control Toolbox, Controller Design with Constraint on the Control Signal, Robust Gain-Scheduled Control, Control Algorithm Implementation in Real-Time, Embedded Safety Loop Development, Risk Assessment and Safety Levels, Classification of Faults, Calculation of Probability of Failure on Demand.

Learning Resources	1. *A. Forrai, "Embedded control system design- A model based approach," Springer-Verlag, 2013* 2. *Adamski MA, Karatkevich A, Wegrzyn M. Design of embedded control systems. Berlin: Springer; 2005 Jun 1.*	3. *Marian Andrzej Adamski, Andrei Karatkevich, Marek Wegrzyn, "Embedded Control systems," Springer Science, 2006* 4. *Dorf RC. Systems, controls, embedded systems, energy, and machines. CRC press; 2017 Dec 19.*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Final Examination (40% weightage)	
		Formative CLA-1 Average of unit test (50%)		Life-Long Learning CLA-2 (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	*Remember*	*30%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*30%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*20%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*20%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1.Dr. M.K. Srilekha, SRMIST*
2. Hariharan VS, Vice president-HR BP @ Edveon Technologies	*2. Dr. R. Ramesh, Professor EEE, Anna University, Guindy*	*2. Dr. J. Subhashini, SRMIST*

Course Code	21ECC504J	Course Name	SoC ARCHITECTURE AND PROGRAMMING	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*realize the need and significance of system on chip architecture in embedded design*
CLR-2:	*learn the design of system on chip design based on different processor architecture*
CLR-3:	*study the interconnection and buses of system on chip*
CLR-4:	*familiarize the principle of low power design on system on chip using Zynq board*
CLR-5:	*analyse the simulation experiments with system on chip*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*develop the process building blocks of system on chip system design using Vivado*	*3*	*2*	*-*
CO-2:	*articulate the architectural structure of SoC design*	*3*	*2*	*-*
CO-3:	*elucidate the interconnection and hardware design of SoC design*	*-*	*2*	*3*
CO-4:	*design a low power system model for SoC using Zynq board*	*-*	*2*	*3*
CO-5:	*acquire knowledge peripheral and interrupts for SoC design*	*-*	*2*	*3*

Module-1 - Introduction to the System Approach	***15 Hour***
System Architecture, Components of the system, Hardware and Software, Processor Architectures, SIMD Architectures, Multiprocessors, Memory and Addressing. System level interconnection, SoC design, System Architecture and Complexity, Reconfiguration of SoC *Practice: Introductory lab on vivado design tool (IDE) with basic arithmetic and logical operations*	
Module-2 - Processors of System on Chip Design	***15 Hour***
Canonical SoC design, SoC Design Flow, Waterfall, Spiral, Top-Down, Bottom-Up, Types of Specifications, Processor Selection for SOC, Processor Architecture, Processor Micro Architecture, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors. *Practice: Sample design simulation, GPIO interfacing to LED using AXI*	
Module-3 - Interconnection Structures	***15 Hour***
SoC Interconnection Structures- Bus-based Structures, SOC Standard Buses, Analytic Bus Models, Network on Chip, Interconnection Structures, Topologies- routing- flow control- network components - router/switch, network interface, Links. *Practice: GPIO interfacing to LED with software and blinking rate change, Programs on Hardware Interrupt.*	
Module-4 - Introduction to Zynq	***15 Hour***
Zynq device, Designing with Zynq, Design flow, Vivado and design boards, Device comparisons, Zynq and FPGA, Zynq and Standard processor, Zynq with discrete FPGA, Application opportunities, Zed board and applications, Sample designs on Zynq. *Practice: Hardware interrupt counter with display in LED, AXI timer experiment*	
Module-5 – Zynq SoC Hardware and Design	***15 Hour***

Peripheral access, SoC overview, Interfacing and signals, implementation metrics and considerations, interconnects, Memory architecture DDR memory controller, Static memory interface, On Chip memory, Interrupts, Interrupts sources, PPI, SPI, SGI. *Practice: IP block simulation, Case study experiment.*

Learning Resources	1. *Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd, 2011* 2. *Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer* 3. *Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, "The Zynq Book", University of Strathclyde, Glasgow, Scotland, UK & Xilinx, Under Open-source license, 1st edition, 2014*	4. *"Vivado design suite user guide", Xilinx, 2021.* 5. *System on Chip (SOC) Architecture by Veena S. Chakravarthi, Springer, 2022.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	-	*10%*	*20%*	-
Level 2	*Understand*	*20%*	-	-	*10%*	*20%*	-
Level 3	*Apply*	*30%*	-	-	*30%*	*30%*	-
Level 4	*Analyze*	*20%*	-	-	*20%*	*30%*	-
Level 5	*Evaluate*	*10%*	-	-	*20%*	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	1. *Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	1. *Dr. A.Manikandan, SRMIST*
2.Ramesh R .Nair, IP functional validation Engineer Grade 08, Intel Corporation	*2. Dr. V. Bhanumathi, Associate Professor EEE, Anna University, Guindy*	2. *. Dr. S. Kayalvizhi, SRMIST*

Course Code	21ECC505J	Course Name	ARTIFICIAL INTELLIGENCE FOR EMBEDDED SYSTEMS	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*define aspects of machine learning*
CLR-2:	*implementing the probability and statistics with python*
CLR-3:	*developing the training model*
CLR-4:	*implementation of various training model*
CLR-5:	*creating an application*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understanding the concepts of machine learning*	2		3
CO-2:	*demonstrate python concepts for probability and statistics*	2		3
CO-3:	*learning the construction training model*	2		3
CO-4:	*implementation of wake word detection with help of the architecture*		2	3
CO-5:	*developing the model for given application*		2	3

Module-1 Introduction to Machine Learning	***15 Hour***
Machine Learning, Aspects of Machine Learning, Machine Learning Application, Linear Regression, Correlation, Regression Analysis of. Supervised and Unsupervised Learning, Supervised Learning Model, Un Supervised Learning Model, Semi Supervised Learning, comparison, Case Study. Reinforcement Learning: Reinforcement Learning model, Markov Decision Problem, Q-Learning, Temporal Decision Learning, Learning Automata, Case Study, Cluttering: k-means, Fuzzy, Hierarchical, Similarity. *Practice: Machine Learning for Supervised and Unsupervised Learning models*	
Module-2 Probability and Statistics with Introduction to Python	***15 Hour***
Introduction to Probability and Statistics, Need for Probability and Statistics, First Order Linear Model, Least Square Regression Line Model, Introduction to Scientific, Libraries in Python-NumPy, Introduction to Scientific Libraries in Scipy, Estimated Coefficients, Problems related to linear model, Importing dataset using Pandas, Altering dataset using Pandas, Selection Operator, Plotting Libraries, Introduction and basic analysis using Scikit- Learn, Introduction to Keras, Introduction to Tensor Flow. *Practice: Basic Mathematical and Scientific Operations using NumPy & SciPy, Analysis of a Dataset (CSV) using Pandas with plots, Basic Mathematical Operations using Keras and Tensor flow.*	
Module-3 The "Hello World" of Tiny ML	***15 Hour***
Building and Training a Model, Applications, Deploying to Microcontrollers, building on embedded Microcontroller model, training our model, Converting the model for Tensor Flow Lite, *SparkFun edge, ST Microelectronics.* *Practice: Model Deploying in Arduino Microcontrollers*	
Module-4 Wake-Word Detection	***15 Hour***
Application Architecture, Walking Through the test, listening for wake words, Deploying to Microcontrollers, Training the New model, Using the model in the project, Training with own Data. Person Detection: Building an Application, Training Model *Practice: Programming Arduino Tensor flow Lite applications*	

Module-5 Magic Wand	**15 Hour**
Magic Wand Building an Application, Training Model, TensorFlow Lite for Microcontrollers, Designing TinyML Applications. *Practice: Magic wand – Training a model*	

Learning Resources	1. *Wes McKinney, "Python for Data Analysis: Data Wrangling with Pandas, NumPy, and IPython", Second Edition, O'reilly Media, Inc., First Edition, 2018.* 2. *Machine Laerning: a practitioner's approach, Chandra S.S., Vinod, Hareendran S., Anand, PHI Learning pvt. ltd., 2021* 3. *TinyML_ Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers- Pete Warden, Daniel Situnayake -O'Reilly Media (2019)*	4. *https://www.coursera.org/learn/introduction-to-embedded-machine-learning#syllabus* 5. *https://sites.google.com/g.harvard.edu/tinyml/home* 6. *https://www.udemy.com/course/getting-started-with-embedded-ai-hands-on-experience//*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 -Practice (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	*-*	*-*	*20%*	*20%*	*-*
Level 2	*Understand*	*20%*	*-*	*-*	*20%*	*20%*	*-*
Level 3	*Apply*	*30%*	*-*	*-*	*30%*	*30%*	*-*
Level 4	*Analyze*	*30%*	*-*	*-*	*30%*	*30%*	*-*
Level 5	*Evaluate*	*-*	*-*	*-*	*-*	*-*	*-*
Level 6	*Create*	*-*	*-*	*-*	*-*	*-*	*-*
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. S.Murugaveni,,SRMIST*
2 Mr. .Ramesh R .Nair, IP functional validation Engineer Grade 08, Intel Corporation	*2. Dr. V. Bhanumathi, Associate Professor EEE, Anna University, Guindy*	*2. Dr.J.Subhashini, ,SRMIST*

ACADEMIC CURRICULA

Embedded System Technology

Professional Elective Courses

Regulations 2021

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Chengalpattu District 603203, Tamil Nadu, India

Course Code	21ECE501T	Course Name	EMBEDDED SYSTEM DESIGN AND STANDARDS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book/Codes/Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*define a comprehensive overview of embedded hardware*
CLR-2:	*explain computer architecture principles and on-chip bus interfaces*
CLR-3:	*interpret on-board bus interfacing and protocol standards in embedded system design*
CLR-4:	*apply knowledge of RTOS features and process management concepts*
CLR-5:	*demonstrate device driver programming skills*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*analyse the internal components of ARM processor and Cortex-M3 MCU*	*3*	*-*	*2*
CO-2:	*describe multiprocessor cache mapping techniques, cache coherence, and memory consistency models*	*3*	*2*	*-*
CO-3:	*implement on-board bus interfacing and wired bus standards for embedded design*	*2*	*-*	*3*
CO-4:	*analyse the RTOS process management models*	*3*	*-*	*2*
CO-5:	*interpret embedded device driver programming and protocol standards*	*3*	*2*	*-*

Module 1 -Embedded Hardware Overview	***9 Hour***
ARM Architecture, ARM Processor Modes. Scheduling, Interrupts and Exceptions Processing, Instruction set, Thumb Instruction set, ARM Assembly language Programming, Data Transfer Operations, Arithmetic Operations, GPIO Programming, Serial Port and Interrupt Programming, Timers Programming, Device Interfacing: Memory Interfacing, Branch Operations, Branch and Conditional Execution Operations, Function handling and arguments, Register. allocation, Instruction Scheduling	
Module-2 - Computer Architecture and Bus Interfacing	***9 Hour***
Memories: Cache memory architecture and organization, Memory hierarchy and cache, Memory Management Unit, Address Translation Mechanism, Cache mapping techniques, Load and store Operations in assembly level programming, Cache replacement policy, Cache write techniques, Cache trashing mechanism, Advanced Microcontroller Bus Architecture Standard: AHB and APB, Peripheral Bus Interfacing,, Designing Simple APB Peripherals, Stack handling in microprocessors, Stack Operations, Software Interrupt Handling	
Module-3 – - Bus Interfacing and Protocol Standards	***9 Hour***
Interfacing: Time-multiplexed data transfer, Two protocol control methods, Strobe/handshake compromise, Interrupts: Interrupt-driven I/O using fixed vectored interrupts processing, Direct memory access: Peripheral to memory transfer with DMA, Memory access without DMA, I/O Port Handling, Parallel I/O Programming, Arbitration using priority arbiter, Daisy-chain configuration . *Standards: UART, Serial Peripheral Interface, SPI Operations and Interfacing, Universal Serial Bus - interfacing, Inter-Integrated Circuits operation, Inter-Integrated Circuits interfacing, IEEE 802.11 Wi-Fi Standard, IEEE 802.15 Bluetooth Protocol, Bluetooth Protocol Architecture*	
Module-4 - Process Management	***9 Hour***
Tasks and task states, Task Scheduling in RTOS Priority Inversion, Priority Ceiling, Priority Inheritance, Shared-Data Problem, Interrupt Latency, Multitasking, Context Switching, Semaphore, Serial Port Programming in assembly language, Applications of Semaphores, Semaphore synchronization mechanisms, Process Communication, Process handling in OS, Uniprocessor Embedded System Kernel, Multi-processor Embedded System basics, Introduction to OpenMP, Tasking: The task and task stack access, task-wait Constructs, Exceptions and Interrupts	

Module-5- Device Driver Programming	***9 Hour***
Introduction to Linux Kernel and Porting, The Boot Process, Role of device Driver, Classes of Device and Modules, Module Basics, Steps to write the module, Implementing System Calls, System Call functions, Task priority, Tasking dependencies, Task Scheduling, Task context, stack and control blocks, Kernel Debugging, OS Debugging functions, Block Device Driver, Network Device Driver, USB Driver, USB Driver OS handling Multitasking in OS, Multitasking OpenMP, Linux Kernel module level programming, Device drivers: Case Study	

Learning Resources	1. *Vahid, Frank and Givargis, Tony, "Embedded system design: a unified hardware/software introduction", Vol. 52, 2002, Wiley New York.* 2. *Xiao, Perry, "Designing Embedded Systems and the Internet of Things (IoT) with the ARM mbed", 2018, Wiley Online Library.*	3. *Wang, "Embedded and Real-Time Operating Systems", Pages 401-475, Springer, 2017.* 4. *Mahout, Vincent, "Assembly language programming: ARM Cortex-M3,2013, John Wiley & Sons.* 5. *Linux Device Drivers Development: Develop customized drivers for embedded Linux" by John Madieu (2019, Packt Publishing)*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*30 %*	*-*	*40 %*	*-*	*30 %*	*-*
Level 2	*Understand*	*40 %*	*-*	*40 %*	*-*	*40 %*	*-*
Level 3	*Apply*	*30 %*	*-*	*20 %*	*-*	*30 %*	*-*
Level 4	*Analyze*	*-*	*-*	*-*	*-*	*-*	*-*
Level 5	*Evaluate*	*-*	*-*	*-*	*-*	*-*	*-*
Level 6	*Create*	*-*	*-*	*-*	*-*	*-*	*-*
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. V. Padmajothi, SRMIST*
2. Mr. Ramesh R .Nair, IP functional validation Engineer Grade 08, Intel Corporation	*2. Dr. V. Bhanumathi, Associate Professor EEE, Anna University, Guindy*	*2. Dr.S. Suhasini, SRMIST*

Course Code	21ECE502T	Course Name	COMMUNICATION PROTOCOLS FOR EMBEDDED SYSTEMS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*realize the electrical requirements, and master the signaling protocols of CAN.*
CLR-2:	*acquire expertise in CAN principles for effective physical layer design.*
CLR-3:	*assess and critique vehicular communication protocols for optimal network performance*
CLR-4:	*configure and apply communication protocols across diverse industrial contexts.*
CLR-5:	*analyze, compare, and proficiently implement multiplexed bus protocols in automotive scenarios.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*demonstrate a comprehensive understanding of Controller Area Network principles*			*3*
CO-2:	*apply the foundational principles of Controller Area Network alongside practical deployment of CAN physical standards*	*1*		*3*
CO-3:	*rationalize Vehicular Communication Protocols for critical analysis and assessment of communication systems within vehicular networks.*	*2*	*1*	*2*
CO-4:	*configure networks and apply communication protocols effectively in various industrial and automotive contexts.*	*3*		*1*
CO-5:	*analyze and apply multiplexed bus protocols effectively in diverse automotive communication scenarios*	*3*	*2*	*1*

Module-1 - Controller Area Network	***9 Hour***
Historical Context of CAN, Bus Access and Arbitration, CSMA/CD Vs CSMA/CA, problem of latency, Bitwise contention, Initial consequences, concept of elasticity of a system, Implication of the elasticity of a system, Error Processing and Management, positive and negative acknowledgements, Error management, Error messages, Error management strategy. ISO standardization, Definitions of the CAN Protocol: ISO 11898-1, ISO/OSI layers of the CAN bus, Properties of CAN, CAN 2.0A standard frame, Message transfer, The CAN bit, Data frame, Remote frame, Errors: Their Intrinsic Properties, Detection and Processing, CAN 2.0 B.	
Module-2 - CAN Physical Layer	***9 Hour***
CAN Bit - Nominal Bit Time - Signal Propagation - Bit Synchronization - Network Speed - Different media and coupling modes – High and Low Speed CAN- CAN Components - Application Layers and Development Tools for CAN.	
Module-3 - Vehicular Communication Protocols	***9 Hour***
Vehicular Ad Hoc Network (VANET) - Need of VANET - Components and Characteristics of VANET – Types of Communication in VANET - Dedicated short-range communication (DSRC). Internet of Vehicles (IoV) and Use Cases - Network Characteristics in IoV - Communication and Computing in IoV - V2X Communication Protocols. Protocol Design for Safety Message Broadcast - Communication in Safety Message Broadcast - Network Scenario - Features of Safety Message Broadcast, CIDC: A Distributed and Adaptive MAC Design - Performance Analysis - Performance Evaluation.	
Module-4 - Industrial Communication and Automotive Ethernet	***9 Hour***
Profibus, Network topologies - Network configuration - Active and Passive components - Testing of Profi bus. Basics of MODBUS – and its application. Automotive networking - Electrical requirements - Network layer protocols. TCP/IP, UDP - Ports and sockets - Audio/Video transport protocol - Measurement, calibration, diagnostics.	
Module-5 – Multiplexed Bus	***9 Hour***
FlexRay protocol - Frames - Topology - Synchronization - Architecture of a FlexRay node. LIN – Local Interconnect Network - Concept of the LIN 2.0 Protocol: Operating principle - Data link layer - Physical layer – Performance comparison - Cost and Market - Conformity of LIN.	

Learning Resources	1. *Mushu Li, Jie Gao, Xuemin (Sherman) Shen, Lian Zhao, "Intelligent Computing and Communication for the Internet of Vehicles" Springer, 2023* 2. *Sonali P. Botkar, Sachin P. Godse, Parikshit N. Mahalle, Gitanjali R. Shinde, "VANET : Challenges and Opportunities" CRC Press, 2021* 3. *Flex Ray Consortium, "FlexRay Communication system: Protocol specifications", FlexRay Consortium, 2010.*	4. *Siemens, "Profibus network manual", Simens manual, 2009.* 5. *Dominique Paret, "Multiplexed Networks for Embedded Systemsll", Wiley, 2007.* 6. *Modbus-IDA, "MODBUS application protocol specification", Modbus-IDA, 2006* 7. *SGS-Thompson, "Lin Application note AN1278", SGS - Thompson Ltd. 2002*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Final Examination (40% weightage)	
		Formative CLA-1 Average of unit test (50%)		Life-Long Learning CLA-2 (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Kartik Soundarrajan, Vice President, Quadgen Wireless Solutions pvt Ltd, Bengaluru, kartik.s@quadgenwireless.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	1. *Dr. Deepa T, SRMIST*
2. Mr. Ramesh R .Nair, IP functional validation Engineer Grade 08, Intel Corporation	*2. Dr. V. Bhanumathi, Associate Professor EEE, Anna University, Guindy*	2. *Dr. Giriprasad S, SRMIST*

Course Code	21ECE503T	Course Name	IoT SENSOR NODES WITH ARTIFICIAL INTELLIGENCE	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*introduce the Artificial Intelligence algorithms*
CLR-2:	*introduce the Machine Learning and Deep learning aspects and Architectures*
CLR-3:	*introduce the IoT aspects and Architectures*
CLR-4:	*conceptualize the need for IoT*
CLR-5:	*acquire knowledge on sensor nodes and Data acquisition in IoT systems and used cases*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*appreciate the uses of Artificial Intelligence*	*2*	*-*	*3*
CO-2:	*understand the Machine Learning and Deep Learning Architectures*	*2*	*1*	*1*
CO-3:	*understand the IoT Architectures*	*3*	*-*	*1*
CO-4:	*implement IoT application using hardware platform*	*3*	*-*	*1*
CO-5:	*develop applications using AI enabled /smart IoT sensor for day-to-day life activities*	*2*	*1*	*1*

Module-1 – Application of IoT	***9 Hour***
Introduction to IoT, Need for IoT, Sensing, Actuation, Communication Protocols, Need for Communication Protocols, Sensor Networks, Machine-to-Machine Communications, Interoperability in IoT, Introduction to Arduino Programming, Integration of Sensors with Arduino, Integration of Actuators with Arduino, Applications of IoT- Case Studies, Industrial Applications, Infrastructure Applications, Case Study, Military, Applications, Case Study, Weather Reporting system, IoT Weather Reporting system using Raspberry pi, Irrigation System, Smart Irrigation System Using IoT, Water Quality Management System (WQMS), IoT based (WQMS) system	
Module-2 – Protocols for IoT	***9 Hour***
Unit-2: *Implementation tools for IoT, Hardware for IoT, Arduino - Basics, Programming using Arduino, Raspberry Pi - Basics, Programming using Raspberry Pi, ESP8266 - Basics, Programming using ESP8266, Introduction of Beagle Board, Beagle board - Single Board Computer, Basic Programming, Study of Beagle Board-xM Development Board, Programming using Beagle board, Software for IoT, MQTT Protocol, Usage of MQTT Protocol, REST APIs, Usage of REST APIs, Cloud Services for IoT, Need for Cloud server, Arduino Programming, Case Study, Raspberry Pi Programming, Case Study.*	
Module-3 – Sensor nodes for IoT	***9 Hour***
Need for Sensors and Sensor nodes, Introduction to Sensor nodes, Sensors used in IoT, Position, Pressure Sensors, Proximity and Motion Sensors, Velocity, Displacement Sensors, Temperature and Humidity Sensors, Chemical, Gas sensors, IoT based Intelligent Traffic Management System, IoT based Humidity Monitoring, IoT based Temperature Monitoring, IoT based Smart Parking System Using RFID, Industrial Applications. IoT for Machine vision, Data acquisition Procedure, Data acquisition through connected IoT sensor nodes, Arduino as sensor nodes, Application using Arduino as sensor nodes, Raspberry Pi as sensor nodes, Application using Raspberry Pi as sensor nodes, Data processing On Cloud platforms, Case Study, Data processing on edge hardware, Case Study.	
Module-4 – AI for IoT	***9 Hour***
Introduction to Artificial Intelligence, Need for Artificial Intelligence, Human Brain and Artificial Intelligence, Difference between machine learning and artificial intelligence, History of Artificial Intelligence, Advantages of Artificial Intelligence, Turing Test, Physical Symbol Systems, Scope of Symbolic AI, Scope of Agents, State Space Search, Depth First Search, Heuristic Search, Best First Search	

Hill Climbing, Beam Search, Expert Systems, Rule Based Expert Systems, Inference Engine, Rete Algorithm, Plan Space Planning, Algorithm for Plan Space Planning, Graph plan, Algorithm Graph plan
Module-5 – ML for IoT ***9 Hour***
History of Machine Learning, History of Deep Learning, McCulloch Pitts Neuron, Thresholding Logic, Perceptron Learning Algorithm, Multilayer perceptron (MLPs), Representation Power of MLPs, Sigmoid Neurons, Gradient Descent, Feedforward Neural Networks, Feed Forward Neural Networks, Backpropagation Algorithm, Implementation of BPN, Principal Component Analysis, PCA- interpretations, Singular Value Decomposition, SVD- Interpretations, Convolutional Neural Networks, Architecture of LeNet, AlexNet, ZF-Net Architectures, Architecture of VGGNet, GoogLeNet Architecture, Architecture of ResNet Case Study on AI sensor: BHI260AP, Vision sensor, AI Workplace Occupancy Sensor, AI ToF People Counting Sensor.

Learning Resources	1. *Dr. Guillaume Girardin, Antoine Bonnabel, Dr. Eric Mounier, 'Technologies & Sensors for the Internet of Things Businesses & Market Trends 2014 - 2024', Yole Development Copyrights, First Edition, 2014.* 2. *AurélienGéron, "Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems", Second Edition, O'reillyMedia, Inc., First Edition, 2019.* 3. *David Forsyth and Jean Ponce, "Computer Vision: A Modern Approach", Pearson Education Limited, Second Edition, 2015* 4. *Peter Waher, "Learning Internet of Things", Packt Pub, UK, First Edition, 2015.*	5. *Adrian McEwen and Hakim Cassimally, "Designing the Internet of Things", John Wiley & Sons, 2014* 6. *https://nptel.ac.in/content/syllabus_pdf/106105166.pdf* 7. *https://www.bosch-sensortec.com/products/smart-sensor-systems/bhi260ap/* 8. *https://www.sony-semicon.com/en/technology/ivs/index.html* 9. *https://www.keyence.co.in/download/download/confirmation/?dlAssetId=AS_134458* 10. *https://resource.milesight-iot.com/milesight/document/vs121-datasheet-en.pdf* 11. *https://resource.milesight.com/milesight/iot/document/vs133-datasheet-en.pdf*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. S. Dhanalakshmi, SRMIST*
2.Mr. Ramesh R .Nair, IP functional validation Engineer Grade 08, Intel Corporation	*2. Dr. V. Bhanumathi, Associate Professor EEE, Anna University, Guindy*	*2. Dr. P. Eswaran, SRMIST*

Course Code	21ECE504J	Course Name	MEMS DEVICES AND APPLICATIONS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							2	0	2	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand the need and the importance of MEMS technology and their application*
CLR-2:	*get familiar with MEMS device fabrication techniques and manufacturing process*
CLR-3:	*study the principle and application of piezoresistive and capacitive sensor and actuators*
CLR-4:	*learn the principle and application of piezoelectric, magnetic and thermal sensor and actuators*
CLR-5:	*understand the RF MEMS devices principle and application and explore MEMS sensor and actuator specification and features through case study and manufactures data sheets*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*identify suitable MEMS devices for their application*	1	-	3
CO-2:	*select appropriate MEMS device fabrication techniques and manufacturing process*	2	2	3
CO-3:	*design piezoresistive and capacitive sensor and actuators*	2	2	3
CO-4:	*select appropriate MEMS piezoelectric, magnetic and thermal sensor and actuators*	2	2	3
CO-5:	*design RF MEMS devices for custom design and applications and identify suitable sensor or actuator for the embedded system design and product development.*	2	2	3

Module-1 - Introduction to Microsystems	***12 Hour***
Overview of microelectronics manufacture and Microsystems technology, MEMS -Scaling laws, multi-disciplinary nature of MEMS, MEMS Materials – Silicon and silicon compound, MEMS Materials – polymer, Applications of MEMS – Various Cases, Working principle of Microsystems - micro actuation techniques, micro sensors types, Micro valves – micro grippers, micro accelerometers *Practice: Exploring MEMS simulation CAD tool, Simple cantilever*	
Module-2 - Fabrication and Manufacturing Process	***12 Hour***
Fabrication: Substrates, single crystal, silicon wafer formation, Photolithography Etching (Dry and Wet), CVD, Physical vapor deposition-Deposition epitaxy, Manufacturing: Surface micromachining, Bulk Micromachining, LIGA process, SLIGA, Micro system packaging materials - die level, device level, system level, Packaging techniques – 2D and 3D, Die preparation, Surface bonding, Wire bonding, sealing *Practice: Capacitive Pressure Sensor & actuator*	
Module-3 - Application MEMS Devices and Applications - I	***12 Hour***
Principle and application: Piezoresistive principle, Piezoresistive pressure sensor, Capacitive sensor principle, Capacitive accelerometer, Capacitive sensor and actuator problem, Electrostatic projection display, Case study of smart sensor: LPS22HD ultra-compact piezoresistive absolute pressure sensor, BMI160 Inertial Measurement unit, DLP4500NIR digital micro mirror, Capacitive pressure sensor/Touch sensor, Capacitive accelerometer, DLP4500NIR digital micro mirror. *Practice: MEMS RF switch, Temperature sensor/Actuator*	
Module-4 - MEMS Devices and Applications -II	***12 Hour***
Principle and application: Piezo electric sensor, Piezo electric actuator, Magnetic actuator principle and case study, Thermal sensor, Thermal sensor – Problem solving, Thermal actuator, Thermal actuator – Problem solving, Case study of smart sensor: Piezoelectric Sounders/Piezoelectric Buzzers/Piezoelectric Ringers, PMM-3738-VM1000-R PUI Audio MEMS Microphones, Thermal Bend Actuated Inkjet with Pre-Heat Mode, MEMS Thermal Sensors, PMM-3738-VM1000-R PUI Audio MEMS Microphones. *Practice: Piezo electric sensor and actuator, Microfluidics devices*	

Module-5 – MEMS Devices and Applications -III	***12 Hour***
Principle and application: RF MEMS devices – Series Switches, RF MEMS devices –Shunt Switches, MEMS Oscillators, MEMS Filters, MEMS varactors tuners, Optical MEMS principle, Optical MEMS actuators, Case study of smart sensor: ADGM1304 wideband MEMS Switch with Integrated Driver, MEMS audio sensor, DSC63XX MEMS Oscillator, Infra-red sensor Principle and application: RF MEMS devices – Series Switches, DSC63XX MEMS Oscillator. *Practice: Comb drive actuator, MEMS filter*	

Learning Resources	1. *Chang Liu, "Foundations of MEMS", Second Edition, Pearson, 2012* 2. *Stephen D. Senturia, Microsystem Design. 2nd edition, Springer, 2004.* 3. *Tai-Ran Hsu, MEMS and MICROSYSTEMS DESIGN AND MANUFACTURE, McGraw Hill Education; 1 edition, 2017.* 4. *Gaberiel M. Rebiz, "RF MEMS Theory, Design and Technology", John Wiley & Sons, 2010.* 5. *Charles P. Poole and Frank J. Owens, "Introduction to Nanotechnology", John Wiley & Sons, 2009.* 6. *Julian W.Gardner and Vijay K Varadhan, "Microsensors, MEMS and Smart Devices", John Wiley & sons, 2013* 7. *Mohamed Gad – el – Hak, "MEMS Handbook", CRC Press, 2002.*	8. *Rai - Choudhury P. "MEMS and MOEMS Technology and Applications", PHI Learning Private Limited, 2009.* 9. *Sabrie Solomon, "Sensors Handbook," McGraw Hill, 1998.* 10. *Marc F Madou, "Fundamentals of Micro Fabrication", CRC Press, 2nd Edition, 2002.* 11. *Francis E.H. Tay and Choong. W.O, "Micro fluidics and Bio mems application", IEEE Press New York, 1997.* 12. *Trimmer William S., Ed., "Micromechanics and MEMS", IEEE Press New York, 1997.* 13. *Maluf, Nadim, "An introduction to Micro electro mechanical Systems Engineering", AR Tech house, Boston 2000.* 14. *Julian W.Gardner, Vijay K.Varadan, Osama O. AwadelKarim, "Micro sensors MEMS and Smart Devices", John Wiley& sons Ltd., 2001.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 - Practice (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	-	*10%*	*20%*	-
Level 2	*Understand*	*20%*	-	-	*20%*	*20%*	-
Level 3	*Apply*	*30%*	-	-	*25%*	*30%*	-
Level 4	*Analyze*	*30%*	-	-	*30%*	*30%*	-
Level 5	*Evaluate*	-	-	-	*15%*	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. P. Eswaran, SRMIST*
2. Mr.Hariharan VS, Vice president-HR BP @ Edveon Technologies	*2. Dr. R. Ramesh, Professor EEE, Anna University, Guindy*	

Course Code	21ECE505T	Course Name	SECURITY FOR EMBEDDED SYSTEMS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*study and understand encryption techniques*
CLR-2:	*implement and apply crypto protocols*
CLR-3:	*realize the authentication methods and attacks in the security of embedded systems*
CLR-4:	*study and analyze the building blocks of security and management engine*
CLR-5:	*analyze and use Intel's TPM and EPID technology for embedded system security*

Course Outcomes (CO):	**At the end of this course, learners will be able to:**	Programme Outcomes (PO)		
		1	**2**	**3**
CO-1:	*acquire knowledge of encryption methods*	3		
CO-2:	*infer and implement crypto protocols*	1	3	
CO-3:	*summarize authentication methods, attacks*	2	1	
CO-4:	*implement counter measures and use security management engines*	2		2
CO-5:	*interpret security issues related to embedded systems and use Intel's TPM and EPID technology*		1	3

Module-1 – Introduction to Secure Embedded Systems	***9 Hour***
Cryptography and side channel, Types of attacks on embedded devices, RFID, Wireless cards, PDAs, Mobiles, ATMs, Automobiles, FPGAs. Key, Randomness, Physically Unclonable functions, Key lifetime, Storage, Authentication and key types. Trusted Platform Module, NOC security, Using keys, Shared keys, KDC, Needham–Schroeder, Public key approaches, Mathematics of Crypto keys	
Module-2 – Security Protocols	***9 Hour***
Elliptic curve protocols: Terminology and definitions, High level elliptic curve computations, Mathematics behind Elliptic curves, The Curve Over a Field, Point computations, Performance Improvements Symmetric key protocols: The theory of cipher, Block cipher, DES, AES, TEA, Stream Cipher, RC4, GRAIN, Cipher modes of operation, Authenticated Modes for Encryption, Embedded Systems Implications	
Module-3 - Data integrity, Message authentication and Side Channel Attacks	***9 Hour***
Authentication function: Terminology and protocols, Structure of authentication function, SHA-2, Integrity trees, Side Channel Attacks on the Embedded System, Theory of the side channel, Side channel attacks in practice, EM probe, Sample analysis, Differential analysis, Correlation analysis, Differential frequency analysis	
Module-4 - Countermeasures and Reliable, Testable Secure Systems	***9 Hour***
Countermeasures: Misalignment and Masking counter measures: S-Box masking, Evaluating counter measures and higher order analysis, Address masking of S box, Counter measures for public key cryptography, Reliable testable secure systems. Reliable testable secure systems: Reliability and Fault Tolerance, SEU-Resistant FPGA Design, SEU-Resistant AES Design, Testable and FPGA Security	
Module -5 - Privacy at next level: Intel's Enhanced Privacy Identification (EPID) Technology	***9 Hour***
Privacy and EPID, EPID verification, Implementation of EPID, Application of EPID, Next generation EPID. Boot Integrity: Boot Attack, Jail Breaking, TPM, Field programmable fuses, Boot methods, Intel's Platform Trust technology, DRM schemes, End to end content protection, Closed door model, OTP provision.	

Learning Resources	1. *Kleidermacher D, Kleidermacher M. "Embedded systems security: practical methods for safe and secure software and systems development". Elsevier; 2012.* 2. *Xiaou Rouan, "Platform embedded technology Revealed: Safeguarding the future of computing with Intel security and management engine", Apress Open, 2014.*	3. *Konstantinos Markantonakis, Keith Mayes, editors. "Secure Smart Embedded Devices, Platforms and Applications". Springer, 2014* 4. *Motahhir S, Maleh Y, editors. "Security Engineering for Embedded and Cyber-Physical Systems". CRC Press; 2022.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Kartik Soundarrajan, Vice President, Quadgen Wireless Solutions pvt Ltd, Bengaluru, kartik.s@quadgenwireless.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. T. Deepa, SRMIST*
2.Mr. Ramesh R .Nair, IP functional validation Engineer Grade 08, Intel Corporation	*2. Dr. V. Bhanumathi, Associate Professor EEE, Anna University, Guindy*	*2. Dr. Arumbu V N, SRMIST*

Course Code	21ECE506T	Course Name	MULTIPROCESSORS REAL TIME SYSTEMS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*learn about the importance of multiprocessor and multicomputer architecture.*
CLR-2:	*educate on the Parallelism concepts in programming for high Performance.*
CLR-3:	*realize the various memory systems protocol optimizations used in multiprocessor system design.*
CLR-4:	*investigate the design of a snoop-based multiprocessor system.*
CLR-5:	*examine the scalable multiprocessors with examples.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*describe architectural features of advanced processors used in developing multiprocessor real time system.*	*2*	*3*	-
CO-2:	*demonstrate parallelism concept in hardware/software.*	*3*	-	*2*
CO-3:	*select appropriate memory for multiprocessor and its challenges.*	*3*	--	*2*
CO-4:	*examine the snoop-based multiprocessor in the system design.*	*3*	-	*2*
CO-5:	*analyze the concept of scalable multiprocessors*	*3*	-	*2*

Module-1-Introduction to Multiprocessors	***9 Hour***
Multiprocessors and Multicomputer, Multi vector and SIMD computers, Architectural Development Tracks, Processors and Memory Hierarchy, Advanced Processor Technology, Superscalar and vector Processor, Memory Hierarchy technology, Virtual memory technology.	
Module-2- Parallel Programs	***9 Hour***
Introduction-The Parallelization Process, Instruction-Level Parallelism: Concepts and Challenges, Basic Compiler Techniques for Exposing ILP, Overcoming Data Hazards with Dynamic Scheduling, Dynamic Scheduling: Examples and the Algorithm, Thread-Level Parallelism-Centralized Shared-Memory Architectures, Performance of Symmetric Shared-Memory Multiprocessors, Distributed Shared-Memory and Directory, Based Coherence, Case Study 1: Single-Chip Multicore Multiprocessor, Case Study 2: Simple Directory-Based Coherence	
Module-3- Shared Memory Multiprocessors	***9 Hour***
Cache Coherence, Memory Consistency, Design Space for Snooping Protocols, A 3-state (MSI) Write-back Invalidation Protocol, A 4-state (MESI) Write-Back Invalidation Protocol, A 4-state (Dragon) Write-back Update Protocol, Assessing Protocol Design Tradeoffs, Workloads, Impact of Protocol Optimizations, Tradeoffs in Cache Block Size-, Update-based vs. Invalidation, based Protocols-Synchronization	
Module-4- Snoop-Based Multiprocessor Design	***9 Hour***
Introduction, Correctness Requirements, Base Design: Single-level Caches with an Atomic Bus, Multi-level Cache Hierarchies, Split-transaction Bus, Case Studies: SGI Challenge and Sun Enterprise SMPs-Extending Cache Coherence.	
Module-5- Scalable Multiprocessors	***9 Hour***
Scalability, Realizing Programming Models, Physical DMA- Case Study: nCUBE/2, User-level Access-Case Study: Thinking Machines CM-5, Dedicated Message Processing- Case Study: Intel Paragon, Shared Physical Address Space- Case study: Cray T3D, Clusters and Networks of Workstations- Case Study: Myrinet SBus Lanai	

Learning Resources	1. *Hennessy, J.L. Y Patterson, D.A., 2019. Computer Architecture: A Quantitative Approach. Sixth Edition. Cambridge,* 2. *Culler, D.E., Singh, J.P. Y Gupta, Anoop., 1999. Parallel Computer Architecture: A Hardware/Software Approach. San Francisco: Morgan Kaufmann Publishers.* 3. *Phillip A. Laplante, "Real-Time Systems Design and Analysis" John Wiley &Amp;; Sons, 4 Edition, 2015.*	4. *Sanjoy Baruah, Marko Bertogna, Giorgio Buttazzo, Multiprocessor Scheduling for Real-Time Systems, Springer ,2015.* 5. *Gianni Conte, Dante Corso,Multi -Microprocessor system for real Time Applications, Springer Dordrecht,2012*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	1. *Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. S. Kayalvizhi, SRMIST*
2. Mr.Hariharan VS, Vice president-HR BP @ Edveon Technologies	2. *2. Dr. R. Ramesh, Professor EEE, Anna University, Guindy*	*2. Dr. C. Vimala, SRMIST*

Course Code	21ECE507J	Course Name	PROGRAMMING WITH FPGA	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							2	0	2	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*demonstrate the basic concepts of FPGA architecture*
CLR-2:	*understand and relate the concept of PSoC design*
CLR-3:	*describe the FPGA configuration and IP design*
CLR-4:	*design an embedded processor using hardware accelerated design*
CLR-5:	*develop coding for various application using FPGA tools*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*Acquire knowledge on FPGA architecture and practice on HDL language*	*3*		
CO-2:	*Understand and design with PSoC architectures*	*2*		*3*
CO-3:	*Construct systems with Platform FPGAs*	*3*		*2*
CO-4:	*Develop the embedded hardware accelerated design for real time applications*	*3*	*2*	
CO-5:	*Implement the various applications using SysGen and Vivado tool for practice*		*2*	*3*

Module-1 - FPGA Architectures	***12 Hour***
FPGA Introduction- FPGA Internal architectures- Fine, medium, and coarse-grained architectures- CLB, LAB &Slices-Logic Implementation using MUX and LUT- Programmable Interconnections-Anti-fuse, SRAM-Fine, EEPROM-Embedded multipliers, Adders, MAC-Embedded processor cores-clock tree and clock manager-general purpose I/O, Hard IP, Soft IP and Firm IP-FPGA Implementation process for Digital logics *Practice: VHDL and Verilog programs on arithmetic and logic design, Programmable logic design .*	
Module-2 - PSoC	***12 Hour***
PSoC architecture overview - PSoC3 architecture details and 8051 instructions - PSoC C language, Interrupt priority and nesting- The concept of memory and its connectivity to CPU, External memory access - Memory access priority, Direct Memory Access, Different DMA modes - Clocking system: Internal master oscillator, IMO, and sleep/wake up modes - Clock distribution - Types of reset - Interrupts and interrupt lines - Power management: Internal regulators *Practice: PSoC 8051 simulation program in C language*	
Module-3 - FPGA Configuration	***12 Hour***
Design challenges, life cycle, Metrics: measures of success - PLD basics, FPGA configurations - Xilinx Virtex 5 IDE - Slices and CLBs, Slices in Virtex 5 - Bit stream, Programming FPGA - Spectrometer example using Xilinx IDE - Sample IP core design for digital logic *Practice: Programs with FPGA Target boards*	
Module-4 - Hardware Accelerated Designs	***12 Hour***
A simple embedded processor-soft core processor on an FPGA –Real time clock and Interface protocol Programming-Inter-Integrated circuit Interface Programming-UART- Serial peripheral interface programming *Practice: Creating IP core and Interface Protocol Programming*	
Module-5 - SysGen Interfacing and Implementation	***12 Hour***

Use and Interfacing methods of some Blocksets-System design and Implementation using SysGen tool. Zynq 7 series architecture-Use Vivado design flow to build an Embedded System-Adding IP cores in PL *Practice: Vivado Tool Practice*

Learning Resources	1. *Raj, A. Arockia Bazil," FPGA-Based Embedded System Developer's Guide" Taylor & Francis, CRC Press, 2018.* 2. *Clive Maxfield,"FPGAs world class designs, Newnes 2009* 3. *Sass and Schmidt, "Embedded system design with Platform FPGAs", Morgan Kaufmann, 2010.*	4. *Edward H. Currie and David Van Ess, "PSoC3/5 Reference Book", Cypress Semiconductor, 2010.* 5. *https://www.xilinx.com/support/university.html* 6. *Jim Ledin, "Architecting High-Performance Embedded Systems", Packt Publishing Ltd, 2021*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Final Examination (40% weightage)	
		Formative CLA-1 Average of unit test (45%)		Life-Long Learning CLA-2 -Practice (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	*Remember*	*20%*	-	-	*20%*	*20%*	-
Level 2	*Understand*	*20%*	-	-	*20%*	*20%*	-
Level 3	*Apply*	*30%*	-	-	*30%*	*30%*	-
Level 4	*Analyze*	*30%*	-	-	*30%*	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. V.Padmajothi, SRMIST*
2. Mr. Ramesh R.Nair, IP functional validation Engineer Grade 08, Intel Corporation	*2. Dr.V.Bhanumathi, Associate Professor EEE, Anna University, Guindy*	*2. Dr. Sukanya Ghoshi, SRMIST*

Course Code	21ECE508T	Course Name	EMBEDDED SYSTEM FOR POWER DRIVES	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*recall the principle and operation of power electronics devices and convertor*
CLR-2:	*explore the architecture of single and multicore MCU used in E-Mobility*
CLR-3:	*understand the feature of the embedded controller used in PV application*
CLR-4:	*discover the ASIC embedded controller used Electric vehicle application*
CLR-5:	*analyze the application of FPGA and SoC in E-Mobility*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*select the suitable power electronics devices and convertor based on the application*	*3*	*-*	*2*
CO-2:	*optimize the selection of MCU based on functional requirement*	*3*	*-*	*2*
CO-3:	*evaluate performance of embedded controller used in PV application*	*3*	*1*	*2*
CO-4:	*choose appropriate ASIC controller based on functional requirement*	*3*	*1*	*2*
CO-5:	*demonstrate customized FPGA and SoC architecture*	*3*	*1*	*2*

Module-1 - Power Electronics Devices and Convertors	***9 Hour***
Power Diodes, BJT, MOSFET, IGBT - Basic structure & Operation, VI characteristics, turn on/off process, RBSOA/FBSOA curves, On state losses, switching characteristics, Resistive and clamped inductive switching, turn on/off transients, Switching losses, device protection - over current/ short circuit protection, Component selection, Basic Thermal consideration on Power semiconductor devices. Latest trends in Semiconductor technology — SiC, GaN and its advantages. *HV Traction inverter system architecture, Basics of Induction and PMSM machines, Three Phase Inverters -Three Phase Square Wave /Stepped Wave Inverters. Three Phase SPWM Inverters. Choice of Carrier Frequency in Three Phase SPWM Inverters*	
Module-2 – Advanced Embedded Controllers	***9 Hour***
Choosing MCU's for Automotive Applications, Atmel — SMART ARM based MCU, ST- SPC5 32-bit Automotive MCU, NXP -Automotive MCU, Automotive microcontrollers for Electric Powertrain Control, Analog and digital interface, Overview of Single core processor Architecture and its limitations, Architectural Innovations, Need for Multi-core Processor and its Limitations, Classification Multicores, Multicore system software stack, GPUs as Parallel computers — architecture of a modern GPU, Overview of real-time operating systems and their role in embedded systems development. Understand concepts like task scheduling, synchronization, and memory protection	
Module-3 – ASIC Embedded Controllers for Photovoltaic Application	***9 Hour***
TMS320F2806x Real-Time Microcontrollers, Features, C200 microcontrollers, Functional block diagram, memory map, register map, DRV8305 Three Phase Gate Driver, Schematic diagram, Specifications, Functional Block Diagram, Programming, AN1338 dsPIC – Grid connected solar inverter architecture, Hardware and software design, Application, Case study - SPV1040, LT8490, PIC24, dsPIC33	
Module-4 – ASIC Embedded Controllers for E-vehicle Application	***9 Hour***
Hybrid electric architecture, Traction Inverter System Architecture, Traction Inverter Drive Stage, Protection Features, Prevention Circuits - Over-Current and Desaturation Detection, Power Switch Gate Voltage Monitoring, Isolated Analog-to-PWM Channel Case Study –Data sheet of controller: DS14558, DS72XX, L9963E, STSPIN948, STSPIN840	
Module-5 – Reconfigurable Architecture for Embedded Power Drives	***9 Hour***

Supported Automotive grade FPGAs and SoCs – Architecture, DC and Switching Characteristics, Cyclone 10 LP Devices, ECP5 and ECP5-5G Family, Motor Control Designs with an Integrated FPGA Design Flow, FPGA-Based Control for Electric Vehicle and Hybrid Electric Vehicle Power Electronics Case Studies

Learning Resources		
	1. *Kathiresh, M., G. R. Kanagachidambaresan, and Sheldon S. Williamson. E- Mobility. Springer International Publishing, 2022.* 2. *Kathiresh, M., and R. Neelaveni. Automotive Embedded Systems. Springer International Publishing, 2021.* 3. *Navet, Nicolas, and Françoise Simonot-Lion, eds. Automotive embedded systems handbook. CRC press, 2017* 4. *Marwedel, Peter. Embedded system design: embedded systems foundations of cyber-physical systems, and the internet of things. Springer Nature, 2021* 5. *P.C.Sen, Power Electronics, Tata McGraw Hill, 2003.* 6. *Dr. P S Bimbhra, Power Electronics, Khanna Publishers, Sth Edition, 2012.* 7. *R Krishnan, Electric Motor Drives, Modeling, Analysis, and Control, Pearson Education,2001.* 8. *Enamul Md Haque, Permanent Magnet Synchronous Motor Drives: Analysis, Modeling and Control, 2009* 9. *https://www.analog.com/media/en/technical-documentation/data-sheets/8490fa.pdf*	10. *https://www.ti.com/lit/ug/tiduej8b/tiduej8b.pdf?ts=1714877908560&ref_url=https%253A%252F%252Fwww.google.com%252F* 11. *https://ww1.microchip.com/downloads/en/appnotes/pv_appnotes.pdf* 12. *https://www.ti.com/lit/ds/sprs698j/sprs698j.pdf.* 13. *https://www.ti.com/lit/an/slua963b/slua963b.pdf.https://www.st.com/resource/en/datasheet/stspin948.pdf* 14. *https://www.st.com/resource/en/datasheet/stspin840.pdf* 15. *https://www.st.com/resource/en/datasheet/stspin32f0.pdf* 16. *https://www.st.com/resource/en/datasheet/l9963e.pdf* 17. *https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/wp/wp-01162-motor-control-toolflow.pdf* 18. *https://www.latticesemi.com/en/Blog/2022/08/30/16/28/FPGAs-Helping-Cars-Get-Smarter* 19. *https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/wp/wp-01210-electric-vehicles.pdf*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Examination (40% weightage)	
		Formative CLA-1 Average of unit test (50%)		Life-Long Learning CLA-2 (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	*Remember*	*30%*	-	*30%*	-	*20%*	-
Level 2	*Understand*	*30%*	-	*30%*	-	*20%*	-
Level 3	*Apply*	*20%*	-	*20%*	-	*30%*	-
Level 4	*Analyze*	*20%*	-	*20%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. P. Eswaran, SRMIST,*
2. Mr.Hariharan VS, Vice president-HR BP @ Edveon Technologies	*2. Dr. R. Ramesh, Professor EEE, Anna University, Guindy*	*2.Dr. A.Manikandan, SRMIST*

Course Code	21ECE601J	Course Name	COMPUTER VISION FOR EMBEDDED SYSTEMS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							2	0	2	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*review the fundamentals of digital image processing*
CLR-2:	*provide a in depth knowledge in image enhancement*
CLR-3:	*describe various segmentation techniques and image features*
CLR-4:	*discuss the importance of supervised and unsupervised classification techniques*
CLR-5:	*introduce basic concepts in video and real-time image processing*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*strengthen the fundamentals and to know the standards used in digital image processing*	*3*	*-*	*-*
CO-2:	*understand the use of histogram and various filters in image enhancement.*	*2*	*-*	*1*
CO-3:	*know segmentation techniques and understand the concept of feature extraction*	*2*	*2*	*2*
CO-4:	*classify images with supervised or unsupervised learning techniques*	*1*	*3*	*2*
CO-5:	*illustrate the mechanism behind MPEG compression and methods to reduce computational load of video algorithm*	*1*	*3*	*3*

Module-1 – Introduction to Computer Vision	***12 Hour***
Digital Image Processing – Various Fields that use Image Processing – Fundamentals Steps in Digital Image Processing – Components of an Image Processing System. Applications of Computer Vision – Recent Research in Computer Vision. Introduction to Computer Vision and Basic Concepts of Image Formation: Introduction and Goals – Image Formation and Radiometry – Geometric Transformation – Geometric Camera Models – Image Reconstruction from a Series of Projections. *Lab: Image transformation (scaling, translation, rotation), Colour space conversion, Image transform (DCT)*	
Module-2 – Image Enhancement	***9 Hour***
Spatial Domain: Gray level Transformations, Histogram, Histogram Modeling, equalization, Spatial filtering smoothing, sharpening, Filtering in frequency domain (Ideal LPF, HPF), Filtering in frequency domain (LPF, HPF), Median Filters, Homomorphic Filtering *Lab: Gray level transformation, Histogram manipulation, Filtering operation- spatial*	
Module-3 – Image Segmentation and Feature Extraction	***15 Hour***
Image Processing Concepts: Fundamentals – Image Transforms – Image Filtering – Colour Image Processing – Mathematical Morphology – Image Segmentation. Image Descriptors and Features: Texture Descriptors – Colour Features – Edge Detection – Object Boundary and Shape Representation – Interest or Cornet Point Detectors – Histogram Oriented Gradients – Scale Invariant Feature Transform. *Lab: Frequency domain filtering operation, Edge detection filters, Boundary description of images*	
Module-4 – Image Classification	***10 Hour***
Unsupervised learning, Clustering, PCA, K means clustering, Supervised learning, KNN learning, Bayes classifier, Support Vector Machine (SVM), detecting features using SVM and HoG features *Lab: K means clustering, SVM classifier, Face detection using Haar feature*	

Module-5 – Digital Video and Real Time Image Processing	***14 Hour***
Pixel-based model- Shadow Detection-Surveillance system- Region-based model- Principles of object tracking-Case Study. Case study- Machine Vision Enabled - Tactical Smart Scope (Application of AI in Defense), Human Pose Estimation (Application of AI in Robotics), Python in Web Development (Application of AI in Web Dev), Insights Dashboards (Application of AI in Retail Application) *Lab: Apply 2D DFT, DCT and DWT transform for an image and compare the results, Feature extraction and classification for medical image, Implement an Image Classifier using CNN in Tensor Flow / Keras.*	

Learning Resources	1. *SandipanDey, Hands-On Image Processing with Python: Expert techniques for advanced image analysis and effective interpretation of image data, Packt Publishing Ltd, 2018* 2. *"Digital Image Processing", 4th Edition (Global Edition), Rafael C Gonzalez and Richard E Woods, Pearson Education Limited, 2018.*	3. *"Mastering OpenCV 4 with Python", Alberto Fernández Villán, Packt Publishing, 2019.* 4. *"Computer Vision and Image Processing - Fundamentals and Applications", Manas Kamal Bhuyan, CRC Press, 2020.* 5. *"Practical Python and Open CV: Case Studies", 3rd Edition, Adrian Rosebrock, PyImage Search, 2016.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 -Practice (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	-	*20%*	*20%*	
Level 2	*Understand*	*30%*	-	-	*30%*	*30%*	
Level 3	*Apply*	*30%*	-	-	*30%*	*20%*	
Level 4	*Analyze*	*20%*	-	-	*20%*	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Kartik Soundarrajan, Vice President, Quadgen Wireless Solutions pvt Ltd, Bengaluru, kartik.s@quadgenwireless.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. S. Dhanalakshmi, SRMIST*
2.Mr. Hariharan VS, Vice president-HR BP @ Edveon Technologies	*2. Dr. R. Ramesh, Professor EEE, Anna University, Guindy*	*2..Dr.S.Latha, SRMIST, Chennai*

Course Code	21ECE602T	Course Name	AUTOMOTIVE EMBEDDED SYSTEMS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co- requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1:	*learn automotive embedded systems basic concepts*
CLR-2:	*understand embedded systems design for automotive applications*
CLR-3:	*design optimal embedded communication models*
CLR-4:	*understand the basics dependable automotive networks*
CLR-5:	*develop software for automotive embedded systems and gain knowledge on verification and testing.*

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	*Programme Outcomes (PO)*		
		1	*2*	*3*
CO-1:	*know and understand the basics of automotive embedded systems*	*1*	-	*3*
CO-2:	*able to design different system embedded systems design for automotive applications*	*1*	-	*3*
CO-3:	*design optimal embedded communication models*	*1*	*1*	*3*
CO-4:	*know and understand the dependable automotive networks*	*3*	-	*1*
CO-5:	*design and develop different software for automotive embedded systems and know the testing procedure*	*3*	-	*1*

Module-1 - Automotive Architectures	***9 Hour***
Introduction and General Context, Power Train Domain, Chassis Domain, Body Domain, Multimedia Telematic, HMI, Active/Passive Safety, Diagnostic, In-Vehicle Networks and Protocols, Operating Systems, Middleware Architecture Description Languages for Automotive Applications, Certification Issue of Safety-Critical In-Vehicle, Main Objectives of AUTOSAR, Working Methods, AUTOSAR Concept, Layered Software Architecture, BSW and RTE Description of the Methodology, AUTOSAR Models, Templates and Exchange Format, Congestion Problem, Energy and Emissions, Wireless Network Technologies, Intelligent Control Applications, Latest Driving Assistance, Fail-Safe Automotive Transportation Systems, Fail-Safe Automotive Transportation Systems, Intelligent Auto-diagnostic, Intelligent Auto-diagnostic, Fail-Safe Automotive Transportation Systems, Fail-Safe Automotive Transportation Systems, Intelligent Auto-diagnostic, Intelligent Auto-diagnostic, Automated Road Vehicles and Road Network, Automated Road Management and Deployment Paths.	
Module-2 - Embedded Communications	***9 Hour***
Characteristics and Constraints, From Point-to-Point to Multiplexed, Communications, Car Domains and Evolution, Different Networks for Different Requirements, Event-Triggered versus Time-Triggered, In-Car Embedded Networks, Installation and Maintenance, Low-Cost Automotive Networks, Rationale for a Middleware, Open Issues for Automotive, Communication Systems, Optimized Networking Architectures, System Engineering, Event-Driven versus Time-Driven, Communication Objectives of FlexRay, History of FlexRay, Frame Format, Communication Cycle, Static Segment, Dynamic Segment, Protocol Architecture, Protocol Wakeup and Startup, Protocol Architecture, Protocol Wakeup and Startup, Protocol Architecture, Protocol Wakeup and Startup, Clock Synchronization, Fault-Tolerance Mechanisms, FlexRay Implementation, Impact on Development, Verification of FlexRay, Verification of FlexRay.	
Module-3 - Dependable Automotive CAN Networks	***9 Hour***
Main Requirements of Automotive, Networking, Networking Technologies, CAN Features and Limitations, Management of Transient Channel Faults in CAN, Impairments to Data Consistency, And Solutions to Data CAN, CANcentrate and ReCANcentrate, Basics CANELy FTT System Architecture, Dual-Phase, Elementary Cycle, SRDB, Main Temporal Parameters within the EC, Fault-Tolerance Features, Accessing the Communication, Services, Control System Transactions, Control System Transactions, FlexCAN Architecture, FlexCAN Architecture, FlexCAN Applications, FlexCAN Applications, TTCAN,Fault-Tolerant Time-Triggered, Communication Using CAN, TCAN, TCAN ServerCAN, ServerCAN, Fault-Tolerant Clock, Synchronization Over CAN	
Module-4 - Embedded Software and Development Processes	***9 Hour***

Basic Concepts, Characteristics and Needs of AE, Software Product Lines, Feature Modeling as a Form of Variability Modeling, Phase-Lead Controller Design Using Root Locus, Feature Modeling for Automotive Domain, Coordination of Small- to Medium-Sized Product Lines, Difficulties Related to Artifact-Local Variability, Representing Variability in ECU, Reuse of Software, Requirements for the Reuse, of Software, Development of Modularized, Automotive Software Components, Systems with Time Delays – Smith Predictor, Function Repository Function Repository, Development of an In-Vehicle Embedded System, Development of an In-Vehicle Embedded System, Development Organization and Information Exchange, Development Organization and Information Exchange, Quality, Safety, and Reuse of Product Line Architectures, Analysis Synthesis and Prototyping, General Aspects on an Automotive ADL, General Aspects on an Automotive ADL, SysML, Architecture and Analysis Description Language, SysML, Architecture and Analysis Description Language.
Module-5 – Verification and Testing ***9 Hour***
Dynamic Testing, Current Practice, Structuring the Testing Process, Model versus Code-Based Testing, Test activities, Test activities, Functional Test Design, Functional Test Design, Structural Test Design, Structural Test Design, Exemplary Test Execution Techniques for Automotive Control Software, Exemplary Test Execution Techniques for Automotive Control Software, Exemplary Test Evaluation Techniques for Automotive Control Software, Exemplary Test Evaluation Techniques for Automotive Control Software, Exemplary Test Evaluation Techniques for Automotive Control Software, Exemplary Test Evaluation Techniques for Automotive Control Software, Test planning, Test planning, Testing in a model-based development process, Testing in a model-based development process, Test planning, Test planning, Selection of test object, Selection of test object.

Learning Resources	1. *Nicolas Navet, Francoise Simonot-Lion, 'Automotive embedded systems handbook', Edition 1, CRC press 2009.* 2. *Kathiresh M, Neelaveni R" Automotive embedded systems-Key Technologies, Innovations and Applications", Springer, 2021.* 3. *Richard Zurawski "Embedded Systems Design and Verification" CRC Press 2018*	4. *Markus Maurer, Hermann Winner" Automotive system Engineering" Springer 2013* 5. *https://www.kpit.com/insights/insights-system-engineering* 6. *Miroslw staron "Automotive Software Architectures: An Introduction" Second Edition, Springer 2021*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Final Examination (40% weightage)	
		Formative CLA-1 Average of unit test (50%)		Life-Long Learning CLA-2 (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Kartik Soundarrajan, Vice President, Quadgen Wireless Solutions pvt Ltd, Bengaluru, kartik.s@quadgenwireless.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1.Dr. P. Eswaran, SRMIST*
2. Mr.Hariharan VS, Vice president-HR BP @ Edveon Technologies	*2. Dr. R. Ramesh, Professor EEE, Anna University, Guindy*	

Course Code	21ECE603J	Course Name	RECONFIGURABLE COMPUTING	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							2	0	2	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*familiarize with the fundamental concepts of reconfigurable Computing*
CLR-2:	*approaches to manage the reconfiguration process to minimize reconfiguration Overhead*
CLR-3:	*introduce the concepts of key mapping steps for reconfigurable FPGA targets*
CLR-4:	*ability to understand the computational architectures of FPGA*
CLR-5:	*understand the utilization of reconfigurable systems for solving challenging computational problems*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*comprehend the fundamental concepts of Reconfigurable Computing*	2	-	-
CO-2:	*acquire knowledge on reconfiguration process management for hardware acceleration*	2	-	-
CO-3:	*perceive knowledge on the integral mapping designs in the context of Architecture Re-configurability*	3	2	-
CO-4:	*gain knowledge on the computational architectures of FPGA*	2	-	2
CO-5:	*exploration of FPGA Reconfigurable applications*	-	-	2

Module-1 - Introduction to Reconfigurable Computing	***12 Hour***
FPGA Design Cycle, Embedded Computer Organization and Methodology of System on Chip System in FPGA Devices, Fine-Grained Reconfigurable Devices, Coarse-Grained Reconfigurable Devices, Design Challenges and Differences of GPP, DSP, ASIC and FPGA based System on Chip Platforms, Application Profiling and Partitioning, FPGAs vs. Multi- Core Processor Architectures, Programming FPGA Applications in VHDL, Limitations of VHDL *Practice: Digital design using FPGAs, Simulation and synthesis using Vivado software and Xilinx*	
Module-2 - Reconfiguration Management	***12 Hour***
Configuration Architectures- Single Context and Multi Context, Configuration Grouping, Configuration Caching, Configuration Scheduling, Configuration Security, Software-based Relocation and Defragmentation, Context Switching, Reducing Configuration Transfer Time- Configuration Compression and Data Reuse, Configuration Security, Operating System Support for Reconfigurable Computing *Practice: Deriving critical path and estimating path delay- analyzing RTL and technology schematic of combinational and sequential circuits*	
Module-3 - Mapping Designs to Reconfigurable Platforms	***12 Hour***
Technology Mapping- Structural Mapping Algorithms- Area-Oriented, Performance-Driven, Power-Aware, Integrated Mapping Algorithms- Simultaneous Logic Synthesis, Integrated Retiming, Placement-Driven, Mapping Algorithms for Heterogeneous Resources- Mapping to Complex Logic Blocks, Mapping Logic to Embedded Memory Blocks, FPGA Placement Problem, Clustering, Partition-based and Analytic Placement *Practice: Study of proposed algorithms to combine logic synthesis with covering to overcome the limitations of pure structural mapping*	
Module-4 - Application Development	***12 Hour***
Strengths and Weaknesses of FPGAs, Application Characteristics and Performance, General Implementation Strategies for FPGA-based Systems, Instance-Specific Design, Partial Evaluation, Fixed Point Number System, Word length Optimization, Distributed Arithmetic- DA Implementation, Mapping DA onto FPGAs, CORDIC Algorithm, Optimized Fixed-Point Arithmetic Circuits in Custom hardware *Practice: Floating Point Multiplier and their types*	
Module-5 – FPGA Applications	***12 Hour***

SPIHT Algorithm- SPIHT Coding Engine, Design Considerations and Modifications- Fixed Point Precision Analysis, Hardware Implementation- The SPHIT Coding Phase, Automatic Target Recognition Algorithms, Dynamically Reconfigurable Designs, Reconfigurable Static Design, The Implications of Floating Point for FPGAs, Floating Point Application *Practice: Matrix Multiply*

Learning Resources	1. *Naomi Bowman, "Reconfigurable Computing: Architecture, Logic and Applications", Clanrye International, 2019.* 2. *Iouliia Skliarova, Piedad Brox Jiménez, Mário Véstias, and Pedro C. Diniz, "Applied Reconfigurable Computing: Architectures, Tools, and Applications," Springer Nature, 2024.* 3. *Christophe Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications," Springer, 2007.*	4. *S. Hauck and A. DeHon, "Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation," Ed., Elsevier, 2008.* 5. *Pao-Ann Hsiung, Marco D. Santambrogio, and Chun-Hsian Huang, "Reconfigurable System Design and Verification", CRC Press, 2009.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2- Practice (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	-	*20%*	*20%*	-
Level 2	*Understand*	*20%*	-	-	*20%*	*20%*	-
Level 3	*Apply*	*30%*	-	-	*30%*	*30%*	-
Level 4	*Analyze*	*30%*	-	-	*30%*	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. George Jacob, Founder and CEO, Semicon Design Technologies, Bangalore, george@semicondesign.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1. Dr. Sukanya Ghosh, SRMIST*
2. Mr. Ramesh R. Nair, IP functional validation Engineer Grade 08, Intel Corporation	*2 . Dr. V. Bhanumathi, Associate Professor EEE, Anna University, Guindy*	*2. Dr. V. Padmajothi, SRMIST*

Course Code	21ECE604J	Course Name	EMBEDDED ROBOTICS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							2	0	2	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*overview of the fundamentals of RISC microcontrollers*
CLR-2:	*discuss the elements required for motion of robots*
CLR-3:	*get familiar with the concepts of transformation and manipulators*
CLR-4:	*introduce the sensors and algorithms for robot movement*
CLR-5:	*illustrate the need and application of embedded robotics*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*discuss about the RISC microcontrollers*	*3*	*2*	*-*
CO-2:	*interrelate the concepts on actuation and driver system*	*3*	*1*	*-*
CO-3:	*demonstrate the concepts of robot control manipulations*	*2*	*3*	*-*
CO-4:	*acquire knowledge on machine vision and artificial intelligence*	*3*	*1*	*-*
CO-5:	*evaluate the real time application of embedded robotics*	*1*	*-*	*3*

Module-1 – Introduction to RISC Microcontrollers	***12 Hour***
Von- Neumann and Harvard architectures, Introduction to 8051 family microcontrollers, 8051 architectures, Register banks and Special Function Registers, Block Diagram, Addressing Modes, Instruction Set, Timers, Counters, Stack Operation, Programming using PIC microcontroller. *Lab: Determination of maximum and minimum positions of links and verification of transformation -. gripper and world coordinate systems*	
Module-2 – Basics of Robotics and Robot Elements	***9 Hour***
Robot-Basic concepts, Need, Law, History, Anatomy, specifications, Robot configurations-cartesian, cylinder, polar and articulate, Robot wrist mechanism. End effectors-Classification, Types of Mechanical actuation, Gripper design, Robot drive system, Types, Position and velocity feedback devices-Robot joints and links-Types, Motion interpolation *Lab: Estimation of accuracy, repeatability and resolution and Robot programming and simulation of pick up and place*	
Module-3 – Robot Kinematics and Control	***15 Hour***
Robot kinematics – Basics of direct and inverse kinematics, Robot trajectories, 2D and 3D Transformation-Scaling, Rotation, Translation Homogeneous transformation. Control of robot manipulators – Point to point, Continuous Path Control, Robot programming *Lab: Robot programming and simulation for colour and shape identification*	
Module-4 – Robot Sensors	***10 Hour***
Sensors in robot – Touch sensors-Tactile sensor – Proximity and range sensors. Force sensor-Light sensors, Pressure sensors, Introduction to Machine Vision and Artificial Intelligence. Collison Fronts Algorithm: Introduction, skeleton of objects. Gradients, propagation, Definitions, propagation algorithm, Thinning Algorithm, Skeleton lengths of top most objects. *Lab: Robot programing for machining (cutting and welding) and for writing practice*	
Module-5 – Robot Vision Applications	***14 Hour***

Overview of Robotics, Pattern recognition and robots, Use of Embedded Systems in Robotics, Robots and Computer Vision. Case study-Automated Navigation guidance by vision system – vision based depalletizing - line tracking - Automatic part Recognition. Image processing techniques implementation through Image Processing software-MATLAB / OPENCV *Lab: Robot programming for any industrial process (packing and assembly) and for multi - process*

Learning Resources	1. *Dr. Jisu Elsa Jacob, Manjunath N, Robotics Simplified: An Illustrative Guide to Learn Fundamentals of Robotics, Including Kinematics, Motion Control, and Trajectory Planning, Paperback, 2022* 2. *John J. Craig, "Introduction to Robotics: Mechanics and Control", Fourth Edition, Pearson, 2018.* 3. *S. B. Niku, Introduction to Robotics – Analysis, Control, Applications, 3rd edition, John Wiley & Sons Ltd., (2020)*	4. *N.P. Bali and Manish Goyal, A textbook of Engineering Mathematics, Laxmi Publications, New Delhi, 10th edition,2016.* 5. *Anis Koubaa, "Robot Operating System (ROS) The Complete Reference", First Volume, Springer, 2016. 5. K.S. F*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 - Practice (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	-	*30*	*20%*	-
Level 2	*Understand*	*30%*	-	-	*30*	*30%*	-
Level 3	*Apply*	*20%*	-	-	*20*	*20%*	-
Level 4	*Analyze*	*30%*	-	-	*20*	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mr. Kartik Soundarrajan, Vice President, Quadgen Wireless Solutions pvt Ltd, Bengaluru, kartik.s@quadgenwireless.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1 Dr. S.Dhanalakshmi, SRMIST*
2. Mr. Hariharan VS, Vice president-HR BP @ Edveon Technologies	*2. Dr. R. Ramesh, Professor EEE, Anna University, Guindy*	*2 Dr. K. Harisudha, SRMIST*

Course Code	21ECE605T	Course Name	SENSORS OF MEDICAL THINGS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*outline the fundamentals of internet of things*
CLR-2:	*explain the need of wearable sensors in health monitoring*
CLR-3:	*get familiar with the concepts of remote health monitoring*
CLR-4:	*analyze the current and future trends of internet of medical things*
CLR-5:	*explore the need and application of IoT in medicine*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*identify the principles, benefits, developments and challenges of Internet of Things*	*3*	*-*	*2*
CO-2:	*gain knowledge on placement, design and implementation of wearable sensors*	*2*	*-*	*1*
CO-3:	*utilize the concepts of remote healthcare monitoring, its evaluation, advantages and limitations*	*3*	*-*	*2*
CO-4:	*acquire knowledge on current and future trends of IoMT*	*-*	*2*	*3*
CO-5:	*evaluate the real time application of IoT in Medicine*	*2*	*3*	*-*

Module-1 - Paradigms in the Internet of Things	***9 Hour***
IoT Characteristics, Architectures for IoT, Sensors, Actuators, and Data Storage, Communication, Protocols, Interface Properties, IoT in Healthcare: Benefits, Developments and Challenges, Examples of IoT-Based Healthcare Devices.	
Module-2 - Wearable Sensors for Health Monitoring	***9 Hour***
Classification of Wearable Sensors, Placement of Wearable Sensor, Biosensors in Healthcare, Wireless Technology for Data Transmission, Interfacing of Sensor in BAN, Power Consumption of Wearable Nodes, Implantable Devices, Common Characteristics of Medical Sensors, Sensor Evaluation Metrics, Design and Implementation of an Example System.	
Module-3 - Remote Healthcare Monitoring	***9 Hour***
Remote Patient Healthcare, Real-Time Analysis, Methodology and Analysis, Microcontroller, Physical Sensors, Software Description, Experimental Evaluation, Advantage and Limitations of Remote Patient Health Monitoring.	
Module-4 - Internet of Medical Things	***9 Hour***
Use of Robotics in Medicine, Data-Driven Medicine, Image Management and Video Surveillance applied in Medicine, Cyber security: The Need for Security in Medical Systems, Legislation Applied to IOMT in Medicine.	
Module-5 – Applications of IoT in Medical Field	***9 Hour***
Case study: Robotics in healthcare, Application of implantable electronics in medicine, Remote health monitoring, Big data mining, Block chain technology in health care.	

Learning Resources	1. *Singh, Krishna Kant, Mohamed Elhoseny, Akansha Singh, and Ahmed A. Elngar, eds. Machine learning and the internet of medical things in healthcare. Academic Press, 2021.* 2. *Cardona, Manuel, Vijender Kumar Solanki, and Cecilia E. García Cena, eds. "Internet of Medical Things: Paradigm of Wearable Devices", CRC Press, 2021.* 3. *Hassanien, Aboul Ella, Nilanjan Dey, and Surekha Borra, eds. "Medical Big Data and internet of medical things: Advances, challenges and applications", CRC Press, 2019.*	4. *Kyung, Chong-Min, Hiroto Yasuura, Yongpan Liu, and Youn-Long Lin. "Smart sensors and systems." Cham, Switzerland: Springer, 2017.* 5. *Yasuura, Hiroto, Chong-Min Kyung, Yongpan Liu, and Youn-Long Lin, eds. Smart sensors at the IoT frontier. Cham, Switzerland: Springer International Publishing, 2017.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*15%*	-	*15%*	-	*15%*	-
Level 2	*Understand*	*25%*	-	*20%*	-	*25%*	-
Level 3	*Apply*	*30%*	-	*25%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*25%*	-	*30%*	-
Level 5	*Evaluate*	-	-	*10%*	-	-	-
Level 6	*Create*	-	-	*5%*	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Kartik Soundarrajan, Vice President, Quadgen Wireless Solutions pvt Ltd, Bengaluru, kartik.s@quadgenwireless.com	*1. Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1.Dr. S. Dhanalakshmi, SRMIST*
2. Mr. Hariharan VS, Vice president-HR BP @ Edveon Technologies	*2. Dr. Parthasarathy R, Assistant Professor, ECE, NIT Trichy. parthasarathy@nitt.edu*	*2. Dr. R. Jansi & Dr. Sayantani Bhattacharya, SRMIST*

Course Code	21ECE606T	Course Name	CLOUD TECHNOLOGY	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand the basic standards and characteristics of cloud computing technology*
CLR-2:	*learn the architecture and modeling of cloud technology*
CLR-3:	*identify and formulate management requirements relating to the configuration and performance of virtual environments.*
CLR-4:	*evaluate information storage management design in a cloud environment*
CLR-5:	*gain knowledge on cloud applications of different service providers*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*exhibit knowledge of the basics of cloud computing*	*1*	*2*	*3*
CO-2:	*understand the concept of cloud architecture and modelling*	2	3	-
CO-3:	*evaluate the virtualization environment*	-	2	3
CO-4:	*analyze the cloud storage management and services*	-	2	3
CO-5:	*examine the cloud tools and applications*	3	2	-

Module-1- Introduction to Cloud Computing	***9 Hour***
Cloud Computing Basics - Characteristics of Cloud Computing, Nature of the Cloud, Seven-Step Model, Types of cloud - Public and Private Cloud, Cloud Infrastructure, Cloud Application Architecture, Cloud Service Models, Cloud Deployment Models, Cloud Computing Technology - Cloud Lifecycle Model, Role of Cloud Modelling and Architecture, Reference Model for Cloud Computing, Cloud Industry Standard.	
Module-2- Cloud Architecture and Modelling	***9 Hour***
Cloud Computing Logical Architecture, Developing Holistic Cloud Computing Reference Model, Cloud System Architecture, Cloud Deployment Model, Cloud Computing: Basic Principles, Model for Federated Cloud Computing, Cloud Ecosystem Model, Cloud Governance.	
Module-3- Virtualization	***9 Hour***
Definition of Virtualization, Adopting Virtualization, Types of Virtualizations, Virtualization Architecture and Software, Virtual Clustering, Virtualization Application, Pitfalls of Virtualization, Virtualization in Grid, Virtualization in Cloud, Virtualization and Cloud Security, Anatomy of Cloud Infrastructure, Virtual Infrastructures, CPU Virtualization, Network and Storage Virtualization.	
Module-4- Cloud Data Storage and Services	***9 Hour***
Data Storage - Data Storage Management, File Systems, Cloud Data Stores, Grids in Data Storage, Cloud Storage - Data Management for Cloud Storage, Provisioning Cloud Storage, Data-intensive Technologies for Cloud Computing, Services – Services and applications by type, Cloud Types and Services, Software as a Service (SaaS), Platform as a Service (PaaS), Infrastructure as a Service (IaaS), Other Clouds Services.	
Module-5- Tools and Applications	***9 Hour***
High-Performance Parallel Computing with Cloud and Cloud Technologies, HADOOP, Tools – VMWare, Eucalyptus, CloudSim, OpenNebula, Nimbus, Applications, case studies on: Microsoft Cloud Services, Google Cloud Applications, Amazon Cloud Services.	

Learning Resources	1. *Srinivasan, A.; Suresh, J (2014), "Cloud computing: a practical approach for learning and implementation", Pearson India Education Services Pvt. Ltd.* 2. *Barrie Sosinsky (2011), "Cloud Computing Bible" Wiley Publishing Inc.* 3. *John W. Rittinghouse and James F. Ransome (2010), "Cloud Computing, Implementation, Management, and Security", CRC Press.* 4. *Borko Furht, Armando Escalante (2010), "Handbook of Cloud Computing", Springer.*	5. *Michael Kavis, (2014) "Architecting the Cloud: Design Decisions for Cloud Computing Service Models (SaaS, PaaS, AND IaaS)", John Wiley & Sons.* 6. *Sunil Kumar Manvi, Gopal K. Shyam (2021) "Cloud Computing: Concepts and Technologies", CRC Press, 1st edition.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*10%*	-	*10%*	-
Level 2	*Understand*	*20%*	-	*10%*	-	*10%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*20%*	-	*20%*	-	*20%*	-
Level 5	*Evaluate*	*10%*	-	*20%*	-	*20%*	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
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