SRM Institute of Science and Technology

(Deemed to be University u/s 3 of UGC Act, 1956)

College of Engineering and Technology

School of Bio Engineering

Department of Chemical Engineering

MINOR IN SEMICONDUCTOR PROCESS ENGINEERING

Foundation Courses (F)					
Course Code	**Foundation Courses- Title**	**Hours/ Week**			**C**
		L	**T**	**P**	
21MCH131F	Introduction to Semiconductor Fabrication Technology	3	0	0	3
21MCH132F	Chemical Engineering Principles in Chip Processing and Semiconductors	3	0	0	3
21MCH133F	Deposition Process Kinetics and Technology	3	0	0	3
21MCH134F	Thin Film Deposition Techniques	3	0	0	3
	Total Learning Credits				**12**
Elective Courses (E)					
Course Code	**Elective Courses -Title (Any 2)**	**Hours/ Week**			**C**
		L	**T**	**P**	
21MCH231E	Advanced materials and characterization in semiconductor manufacturing	3	0	0	3
21MCH232E[3]	Lean Manufacturing Practices of Semiconductors	3	0	0	3
21MCH233E	Quality Control in Chip Manufacturing	3	0	0	3
	Total Learning Credits				**6**

[3] – Blended mode (online)

Course Code	21MCH131F	Course Name	INTRODUCTION TO SEMICONDUCTOR FABRICATION TECHNOLOGY	Course Category	F	Foundation	L	T	P	C
							3	0	0	3

Pre-requisite Courses		Co-requisite Courses		Progressive Courses	
Course Offering Department	Chemical Engineering	Data Book / Codes/Standards			

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	Gain a comprehensive understanding of semiconductor materials, covering the initial phases of semiconductor manufacturing.
CLR-2 :	Grasp the diverse methods employed to build the layered structures of integrated circuits.and the wafer fabrication process.
CLR-3 :	Understand how circuit designs are transferred onto the wafer and how material is selectively removed to create the desired structures.
CLR-4 :	Know the final stages of manufacturing that ensure the device's functionality, durability, and connectivity.
CLR-5 :	Highlights the critical factors that influence the economic viability and performance of semiconductor products.

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	Program Outcomes (PO)											
		1	2	3	4	5	6	7	8	9	10	11	12
		Engineering Knowledge	Problem Analysis	Design/development of solutions	Conduct investigations of complex problems	Modern Tool Usage	The engineer and society	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning
CO-1 :	Learn the key principles of semiconductor materials relevant to device fabrication and the stages of the wafer fabrication process.	3		2									
CO-2 :	Describe various thin film deposition and etching techniques used in semiconductor manufacturing.	3		2									
CO-3 :	Analyze the lithography and patterning processes for device fabrication.		3	2									
CO-4 :	Comprehend the doping, layer deposition, and etching concepts.	2		3									
CO-5 :	Discuss the importance of testing and packaging technologies for semiconductor devices.	1						3					

***Module 1:* Overview of Semiconductor Industry, Materials, and Chemicals** **9 hours**

Origin and growth of semiconductor Industry technology (micro and nano level), Stages of solid-state devices preparation, Invention of the transistor, Basic of Semiconductors and their types - semiconductor materials and their properties -states and properties of matter – Chemical purity and safety issues.

***Module* 2: Silicon wafer preparation** **9 Hours**

Moore's law, Crystal growth techniques: Czochralski (CZ) and Float Zone (FZ) methods – Wafer terminologies, Basic wafer – fabrication operations-example, Outline of Wafer preparation: slicing, lapping, polishing, cleaning, wafer sort, packaging – Contamination control, contamination sources, and Need of the clean room & its elements. Surface cleaning and drying processes.

***Module* 3: Wafer Surface Preparation And Lithography**	**9 hours**
Factors affecting the successful wafer yield – Oxidation process for SiO_2 layer formation, oxidation Process flow – Photo resist chemistry, Ten-Step Patterning Process—Surface Preparation to Exposure, Optical and Non-optical lithography: Principles, resolution, depth of focus. Photoresists: types, properties, processing. Exposure systems: contact, proximity, projection (stepper, scanner), Resolution enhancement techniques (RETs): phase-shifting masks (PSMs), optical proximity correction (OPC), Non-optical lithography: Electron beam lithography (EBL), X-ray lithography, Deep ultraviolet (DUV) lithography, Extreme ultraviolet (EUV) lithography	
***Module* 4: Doping And Layer Deposition Processes**	**9 hours**
Diffusion: Fick's laws, diffusion mechanisms, solid-state diffusion and ion-implantation doping – Over view of deposition system, Physical Vapor Deposition (PVD): Thermal evaporation, Sputtering (DC, RF, magnetron) - Chemical Vapor Deposition (CVD): Basics of CVD: reaction kinetics, transport phenomena, Low-Pressure CVD (LPCVD), Plasma-Enhanced CVD (PECVD), Metal-Organic CVD (MOCVD), Epitaxy: Vapor-phase epitaxy (VPE); Molecular beam epitaxy (MBE); Atomic Layer Deposition (ALD), Etching	
***Module* 5: Interconnection And Packaging**	**9 hours**
Metallization: Aluminum and copper metallization, Sputtering, evaporation, and electroplating, Damascene process, Dielectric materials: Silicon dioxide, low-k dielectrics, Deposition techniques, Multilevel interconnects. Packaging: Die bonding; Wire bonding; Flip-chip bonding; Packaging materials and technologies. Emerging trends: New materials: Ge, III-V compounds, 2D materials, Nanotechnology in semiconductor fabrication, 3D IC fabrication	

Learning Resources	1. *Quirk, Michael, and Julian Serda. Semiconductor manufacturing technology. Vol. 1. Upper Saddle River, NJ: Prentice Hall, 2001.* 2. *Plummer, James D. Silicon VLSI technology: fundamentals, practice, and modeling. Pearson Education India, 2009.* 3. *May, Gary S. Fundamentals of semiconductor fabrication. Wiley, 2004.*	4. *Peter Van Zant, "Microchip Fabrication: A Practical Guide to Semiconductor Processing", McGraw-Hill Professional, Sixth Edition, 2014.* 5. *Campbell, Stephen A. The science and engineering of microelectronic fabrication. Oxford University Press, (2001).* 6. *James D. Plummer, Michael D. Deal, Peter B. Griffin, "Silicon VLSI Technology: Fundamentals, Practice and Modeling", Prentice Hall India Private Limited, 2000*

	Bloom's Level of Thinking	**Continuous Learning Assessment (CLA) - By the Course Faculty**				**By The CoE**	
		Formative CLA-I Average of unit test (50%)		**Life Long Learning** CLA-II- Practice (10%)		**Summative** Final Examination (40% weightage)	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	10	-	10	-		-
Level 2	Understand	20	-	20	-		-
Level 3	Apply	30	-	30	-		-
Level 4	Analyze	30	-	30	-		-
Level 5	Evaluate	10	-	10	-	-	-
Level 6	Create	-	-	-	-	-	-
	Total						

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Mr. N. Nagarajan, Vice President Engineering, EPCOGEN Pvt Ltd	*Dr. S. Sundaramoorthy, Professor, Puducherry Technological University*	*Dr. K. Selvam*

Course Code	21MCH132F	Course Name	CHEMICAL ENGINEERING PRINCIPLES IN CHIP PROCESSING AND SEMICONDUCTORS	Course Category	F	Foundation Course	L	T	P	C
							3	0	0	3

Pre-requisite Courses	NIL	Co-requisite Courses	NIL	Progressive Courses	*NIL*
Course Offering Department	*Chemical Engineering*	Data Book / Codes/Standards	*NIL*		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	Understand the types and properties of semiconductors
CLR-2 :	Understand the applications of fluid mechanics
CLR-3 :	Assimilate the importance of unit processes in semiconductor industry
CLR-4 :	Understand process monitoring strategies
CLR-5 :	Understand gases and chemicals abatement methods

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	Program Outcomes (PO)											
		1	2	3	4	5	6	7	8	9	10	11	12
		Engineering Knowledge	Problem Analysis	Design/development of solutions	Conduct investigations of complex problems	Modern Tool Usage	The engineer and society	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning
CO-1 :	Explain the raw materials and process steps in semiconductor manufacturing	1		2									
CO-2 :	Elucidate the applications of fluid mechanics	3		2									
CO-3 :	Describe the types of unit processes in semiconductor processing	3		2									
CO-4 :	Explain the methods of process monitoring	1		2									
CO-5 :	Describe the gases and chemicals abatement	2		1									

Module 1: Materials for Chips and Semiconductors **9 Hours**

Role of chemical engineering in semiconductor manufacture, Basic properties, types and applications of semiconductors, raw materials for semiconductor and chips manufacturing, properties of silicon, germanium, gallium arsenide and indium phosphide, extraction of silicon from sand, carbon reduction process, refining operations for high purity silicon, crystal growth - Czochralski Method

Module 2: Fluid mechanics applications **9 Hours**

Fluid properties and classification, basic equations of fluid flow, laminar flow and turbulent flow of fluids in channels, flow of liquids in thin layers, Fluid flow in micro-channels, Capillary and surface tension driven flow, applications in etching, doping, deposition and wafer cleaning process, Fluid metering devices and control valves in semiconductor fabrication, Cleanroom design

Module 3: Unit Processes **9 Hours**

Wafer Slicing and Polishing, cleaning operations and preparation of wafer, thin film deposition methods – CVD, PVD methods, lithography technique and etching process, diffusion and ion implantation, metal deposition and metallization process

Module 4: Process Monitoring **9 Hours**

Wafer State Measurements, Interferometry, Ellipsometry, Particle/Defect Inspection, Cleanroom Air Monitoring, Product Monitoring, Grinding, stress relief and dicing operations, Thermal Operations, temperature, pressure and gas flow, Residual Gas Analysis in plasma operations

Module 5: packing and Testing **9 Hours**

Wafer dicing – mechanical sawing, laser cutting, plasma dicing, Wafer-level packaging (WLP), purposes of wafer testing, types of tests, tools and techniques for wafer testing Speciality gas and Clean Dry Air (CDA) system. Speciality gas dispense and distribution, clean dry air, waste gas abatement systems, fundamentals, principles, major components and considerations, per-fluorocarbon compounds (PFC) abatement theory and strategies, catalytic abatement process, elements of chemical and slurry handling systems, fluid handling components and fluid measurement devices

Learning Resources	1) *Fundamentals of Semiconductor Manufacturing and Process Control, Gary S. May and Costas J. Spanos, IEEE Wiley – Inter science, John Wiley & Sons, inc., publication* 2) *Semiconductor Manufacturing Handbook, Hwaiyu Geng, McGraw-Hill company, 2005.* 3) *Unit Operations of Chemical Engineering, Warren L. McCabe, Julian C. Smith, Peter Harriott, fifth edition, McGraw-Hill Chemical Engineering Series*

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) - By the Course Faculty				By The CoE	
		Formative CLA-I Average of unit test (50%)		Life Long Learning CLA-II- Practice (10%)		Summative Final Examination (40% weightage)	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	40%	-	30%	-	30%	-
Level 2	Understand	40%	-	40%	-	40%	-
Level 3	Apply	20%	-	30%	-	30%	-
Level 4	Analyze		-		-		-
Level 5	Evaluate		-		-	-	-
Level 6	Create	-	-	-	-	-	-
	Total	100%		100%		100%	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Mr. N. Nagarajan, Vice President Engineering, EPCOGEN Pvt Ltd	*Dr. S. Sundaramoorthy, Professor, Puducherry Technological University*	*Dr. M. Magesh Kumar, SRMIST*

Course Code	21MCH133F	Course Name	DEPOSITION PROCESS KINETICS AND TECHNOLOGY	Course Category	F	*Foundation*	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*NIL*	Co-requisite Courses	*Nil*	Progressive Courses	
Course Offering Department	*Chemical Engineering*	Data Book / Codes/Standards			

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	Understand the principles of vacuum systems
CLR-2 :	Master vacuum-based thin-film deposition methods
CLR-3 :	Gain expertise in chemical reaction-based thin-film growth processes
CLR-4 :	Explore the influence of thermodynamics and kinetics on thin-film growth parameters
CLR-5 :	Learn techniques for analyzing thin-film properties and applying them in fields

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	Program Outcomes (PO)											
		1	2	3	4	5	6	7	8	9	10	11	12
		Engineering Knowledge	Problem Analysis	Design/development of solutions	Conduct investigations of complex problems	Modern Tool Usage	The engineer and society	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning
CO-1 :	Ability to design and operate vacuum systems for deposition processes			*3*		*1*							
CO-2 :	Skills to select and optimize PVD methods for metallic/oxide thin films	*1*	*2*										
CO-3 :	Competence in analyzing CVD reaction pathways and reactor design		*2*	*2*									
CO-4 :	Ability to model deposition kinetics for tailored film properties		*2*	*3*									
CO-5 :	Proficiency in thin film-based sensors	*1*	*2*										

***Module* 1: Vacuum Technology and Gas Kinetics** **9 Hours**

Kinetic theory of gases: Maxwell-Boltzmann distribution, molecular impingement flux, mean free path, Vacuum systems: Pump types (rotary, diffusion, turbomolecular), pressure measurement (Pirani, Penning gauges), conductance calculations, and Knudsen equation and gas transport mechanisms

***Module* 2: Thermodynamics of Physical Vapor Deposition (PVD) Techniques** **9 Hours**

Evaporation: Thermodynamics, evaporation rates, alloy/compound sources, deposition monitoring, Sputtering: DC/RF magnetron sputtering, target materials, plasma dynamics, Line-of-sight deposition, conformal coverage, and film structure development

***Module* 3: Kinetics of Chemical Vapor Deposition (CVD) Techniques** **9 Hours**

CVD thermodynamics and kinetics: Reaction equilibria, surface processes, diffusion-limited deposition. Techniques: Thermal CVD, plasma-enhanced CVD (PECVD), aerosol-assisted CVD, Epitaxy: Lattice mismatch, growth monitoring, composition control

Module 4: Thin Film Growth Kinetics **9 Hours**

Nucleation and growth: Adsorption, surface diffusion, stress development, Thermodynamic vs. kinetic control: Structure-property relationships, In-situ characterization: Thickness monitoring, stress measurement

Module 5: Thin Film-based sensors **9 Hours**

Fabrication of thin film-based sensors, Humidity sensors, Toxic gas sensors, VOC sensors, experiments on humidity sensing and VOC sensing

Learning Resources	1. *David M. Hata, Elena V. Brewer, and Nancy J. Louwagie, Introduction to Vacuum Technology, Milne Open Textbooks, 2023.*	4. *Anthony C Jones and Michael L Hitchman, Chemical Vapor Deposition Precursors, Processes and Applications, RSC Publishing, 2009.*

	2. *Xiu-Tian Yan, and Yongdong Xu, Chemical Vapor Deposition: An Integrated Engineering Design for Advanced Materials, Springer, 2012.* 3. *John E. Mahan, Physical Vapor Deposition of Thin Films, Wiley-Interscience, 1st edition, 2000.*	*5. Donald M Mattox, Handbook of Physical Vapor Deposition (PVD) Processing, Elsevier, 2nd Edition, 2000.* *6. P. Ciureanu, and S. Middelhoek, Thin Film Resistive Sensors, CRC Press, First edition, 1992.*

	Bloom's Level of Thinking	**Continuous Learning Assessment (CLA) - By the Course Faculty**				**By The CoE**	
		Formative CLA-I Average of unit test (50%)		**Life Long Learning** CLA-II- Practice (10%)		**Summative** Final Examination (40% weightage)	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30%	-	30%	-	30%	-
Level 2	Understand	30%	-	30%	-	30%	-
Level 3	Apply	20%	-	20%	-	20%	-
Level 4	Analyze	20%	-	20%	-	20%	-
Level 5	Evaluate		-		-	-	-
Level 6	Create	-	-	-	-	-	-
	Total						

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Mr. N. Nagarajan, Vice President Engineering, EPCOGEN Pvt Ltd	*Dr. S. Sundaramoorthy, Professor, Puducherry Technological University*	*K.Anbalagan,SRMIST*

Course Code	21MCH134F	Course Name	THIN FILM DEPOSITION TECHNIQUES	Course Category	F	Foundation	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*-Nil-*	Co-requisite Courses	*-Nil-*	Progressive Courses	*-Nil-*
Course Offering Department	*Chemical Engineering*	Data Book / Codes/Standards			

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*	Program Outcomes (PO)											
		1	2	3	4	5	6	7	8	9	10	11	12
		Engineering Knowledge	Problem Analysis	Design/development of solutions	Conduct investigations of complex problems	Modern Tool Usage	The engineer and	Environment &	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning
CLR-1 :	Understand the role and types of thin films in semiconductor devices												
CLR-2 :	Describe and compare various PVD techniques												
CLR-3 :	Understand the working principles and variants of CVD												
CLR-4 :	Explain the fundamentals of epitaxial film growth												
CLR-5 :	Select appropriate characterization methods for thin films												
Course Outcomes (CO):	*At the end of this course, learners will be able to:*												
CO-1 :	Identify and differentiate deposition techniques based on mechanism and applications	*2*				*3*							
CO-2 :	Analyze the influence of deposition parameters on film characteristics			*2*		*3*							
CO-3 :	Evaluate suitability of CVD and ALD for semiconductor process steps			*2*		*2*							
CO-4 :	Apply epitaxial techniques to high-performance device fabrication	*1*		*2*									
CO-5 :	Relate thin film properties to device performance and reliability	*1*		*2*									

Module - 1: Fundamentals of Thin Film Growth and Deposition Principles **9 Hours**

Introduction to Thin Films: Definition, Applications in Semiconductors—Nucleation Theory and Surface Diffusion—Film Thickness Control and Uniformity Considerations—Vacuum Technology Basics: Pumping systems, Gauges, Pressure regimes—Deposition System Design: Chambers, Substrate holders, Gas delivery—Substrate Preparation and Surface Conditioning—Classification of Deposition Techniques.

Module -2: Physical Vapor Deposition (PVD) **9 Hours**

Fundamentals of PVD and Thin Film Evaporation—Thermal Evaporation Techniques and Source Materials—Electron Beam Evaporation: Working and Applications—Sputtering Process: DC and RF Sputtering—Magnetron Sputtering and Reactive Sputtering—High-Power Impulse Magnetron Sputtering (HiPIMS)—Ion Beam Assisted Deposition and Ion Plating—Process Parameters: Pressure, Power, Substrate Bias, Temperature—Applications of PVD in Metallization and Barrier Layers.

Module -3: Chemical Vapor Deposition (CVD) **9 Hours**

Overview of CVD and Reaction Chemistry—Thermal CVD and Low Pressure CVD (LPCVD)—Plasma-Enhanced CVD (PECVD): Mechanisms and Reactor Design—Metal Organic CVD (MOCVD): Precursor Chemistry and Applications
Module -4: Atomic Layer Deposition (ALD) **9 Hours** *Atomic Layer Deposition (ALD): Self-Limiting Growth Concept—ALD Process Examples: High-κ Dielectrics, Conformal Layers in Vias—Area-Selective ALD and Spatial ALD—Precursor Design and Delivery Systems in ALD—Process Challenges: Step coverage, Film Conformality, and Throughput.*
Module -5: Epitaxial Growth and Advanced Deposition Techniques **9 Hours** *Introduction to Epitaxy: Crystalline Quality and Applications—Vapor Phase Epitaxy (VPE) and Selective Epitaxia(SEG)—Molecular Beam Epitaxy (MBE): UHV Conditions, Effusion Cells—MOCVD for Compound Semiconductors (e.g., GaN, GaAs)—Growth of Heterostructures and Quantum Wells—Emerging Techniques: Pulsed Laser Deposition (PLD), Cluster Beam Deposition.*

Learning Resources	*1. R.F. Bunshah, "Handbook of Deposition Technologies for Films and Coatings", Elsevier, 2nd Edition, 1994.* *2. Gary S. May & Simon M. Sze, "Fundamentals of Semiconductor Fabrication", Wiley, 2003.*	*3. John A. Venables, "Introduction to Surface and Thin Film Processes", Cambridge, 2010.* *4. Yoshio Nishi (Ed.), "Handbook of Semiconductor Manufacturing Technology", CRC Press, 2007.*

	Bloom's Level of Thinking	**Continuous Learning Assessment (CLA) - By the Course Faculty**				**By The CoE**	
		Formative CLA-I Average of unit test (50%)		**Life Long Learning** CLA-II- Practice (10%)		**Summative** Final Examination (40% weightage)	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30%	-	30%	-	30%	-
Level 2	Understand	30%	-	30%	-	30%	-
Level 3	Apply	20%	-	20%	-	20%	-
Level 4	Analyze	20%	-	20%	-	20%	-
Level 5	Evaluate		-		-		-
Level 6	Create	-	-	-	-	-	-
	Total	100%		100%		100%	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Mr. N. Nagarajan, Vice President Engineering, EPCOGEN Pvt Ltd	*Dr. S. Sundaramoorthy, Professor, Puducherry Technological University*	*Dr. S. Anandhakumar*

Course Code	21MCH231E	Course Name	ADVANCED MATERIALS AND CHARACTERIZATION IN SEMICONDUCTOR MANUFACTURING	Course Category	E	Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*-Nil-*	Co-requisite Courses	*-Nil-*	Progressive Courses	*-Nil-*
Course Offering Department	*Chemical Engineering*	Data Book / Codes/Standards			

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	Understand basic materials properties critical to semiconductor performance
CLR-2 :	Familiarity with new material systems beyond traditional silicon
CLR-3 :	Gain insight into thin film growth and etching principles
CLR-4 :	Develop ability to select and apply appropriate characterization tools
CLR-5 :	Analyze reliability issues related to materials and processes

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	Program Outcomes (PO)											
		1	2	3	4	5	6	7	8	9	10	11	12
		Engineering	Problem Analysis	Design/development of	Conduct investigations of complex problems	Modern Tool Usage	The engineer and	Environment &	Ethics	Individual & Team	Communication	Project Mgt. & Finance	Life Long Learning
CO-1 :	Relate material properties to process requirements and integration	*1*				*2*							
CO-2 :	Understand material selection criteria for various device nodes			*2*		*3*							
CO-3 :	Understand process-microstructure-property relationships			*2*		*3*							
CO-4 :	Interpret material analysis results for process monitoring	*2*		*2*									
CO-5 :	Apply statistical and metrology tools for yield improvement	*1*		*2*									

Module - 1: Fundamentals of Semiconductor Materials and Process Integration **9 Hours**

Crystal structures and bonding in semiconductors—Doping and defects in crystalline semiconductors—Electrical, optical, and thermal properties of materials—Overview of semiconductor device process flow—Role of materials in process integration.

Module -2: Advanced Materials in Semiconductor Devices **9 Hours**

High-k and low-k dielectrics—Metal gate materials—III-V and 2D materials (GaN, InP, MoS_2, graphene)—Ferroelectric and phase-change materials—Emerging channel materials (e.g., Ge, SiGe, FinFETs, GAA).

Module -3: Thin Film Deposition and Etching Techniques *Physical and chemical vapor deposition (PVD, CVD, ALD)—Atomic layer deposition and epitaxy—Etching technologies: plasma etching, reactive ion etching (RIE)—Surface preparation and cleaning.*	**9 Hours**
Module -4: Materials Characterization Techniques *Film Thickness and Uniformity Measurements: Profilometry, Ellipsometry—Surface and Interface Analysis: XPS, AES, AFM—Structural Characterization: XRD, TEM, SEM—Electrical Properties: Four-Point Probe, Hall Effect—Optical Properties: UV-Vis-NIR Spectroscopy, Photoluminescence—Stress and Adhesion Testing in Thin Films in semiconductor fabs.*	**9 Hours**
Module -5: Reliability, Defect Analysis, and Process Control *Defect identification and failure analysis (FIB, EBIC, CL)—Reliability testing (BTI, TDDB, HCI)—Cleanroom protocols and contamination control—SPC, process windows, and yield analysis.*	**9 Hours**

Learning Resources	*1. E. Machlin, "Materials Science in Microelectronics", Elsevier, Vol. 1, 2005.* *2. Gary S. May and Simon M. Sze, "Fundamentals of Semiconductor Fabrication", Wiley, 2003.*	*3. Gary E. McGuire, "Characterization of Semiconductor Materials", William Andrew, 1st Edition, 1990.* *4. Hong Xiao, "Introduction to Semiconductor Manufacturing Technology", SPIE Press, 2012.*

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) - By the Course Faculty				By The CoE	
		Formative CLA-I Average of unit test (50%)		**Life Long Learning** CLA-II- Practice (10%)		**Summative** Final Examination (40% weightage)	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30%	-	30%	-	30%	-
Level 2	Understand	30%	-	30%	-	30%	-
Level 3	Apply	20%	-	20%	-	20%	-
Level 4	Analyze	20%	-	20%	-	20%	-
Level 5	Evaluate		-		-	-	-
Level 6	Create	-	-	-	-	-	-
	Total	100%		100%		100%	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Mr. N. Nagarajan, Vice President Engineering, EPCOGEN Pvt Ltd	*Dr. S. Sundaramoorthy, Professor, Puducherry Technological University*	*Dr. S. Anandhakumar*

Course Code	21MCH232E	Course Name	LEAN MANUFACTURING PRACTICES OF SEMICONDUCTORS	Course Category	E	Elective	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*-Nil-*	Co-requisite Courses	*-Nil-*	Progressive Courses	*-Nil-*
Course Offering Department	*Chemical Engineering*	Data Book / Codes/Standards			

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	Understand the tools and safety process in clean rooms
CLR-2 :	Understand the detailed setting up of clean rooms and contamination prevention strategy
CLR-3 :	To learn about the procedure of cleaning and etching of clean rooms
CLR-4 :	Understand the basics of semiconductor manufacturing technology
CLR-5 :	Illustration on modern semiconductor manufacturing technology

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	Program Outcomes (PO)											
		1	2	3	4	5	6	7	8	9	10	11	12
		Engineering Knowledge	Problem Analysis	Design/development of solutions	Conduct investigations of complex problems	Modern Tool Usage	The engineer and society	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning
CO-1 :	Demonstrate clean rooms, its protocols and tools used	2		3									
CO-2 :	Apply personnel practices, contamination management strategies for cleaning rooms.	1	3										
CO-3 :	Evaluate the process of dry and wet etching of wafers along with general cleaning procedures	3	3										
CO-4 :	Analyze and compare the conventional semiconductor manufacturing techniques			3			2						
CO-5 :	Evaluate modern semiconductor manufacturing technology for its merits and demerits.				1	2							

Module 1 : Introduction to Clean Rooms	**9 Hour**
Purpose of cleanrooms, Use of PPE for handling and storage of chemicals, Maintenance, Safety protocols, Overview of semiconductor manufacturing, Semiconductor material science-Ingot and wafer fabrication, Use of tools in cleanrooms.	
Module 2 Construction of Clean Rooms	**9 Hour**
Contamination Control Strategies and Chemical Management, Access Control, Personnel Practices, and Safety Procedures, Automation, Maintenance, and Quality Assurance of clean	

rooms, Classification of clean rooms
Module 3: The Chemistry of Cleaning and Etching **9 Hour**
Chemistry of wet cleaning-Introduction to Aqueous Cleaning, Cleaning by acids, The chemistry of wet etching- Silicon Dioxide Etching, Silicon Etching, Silicon Nitride Etching, Rinsing and drying, Overview of rising, Overview of drying, ***General cleaning and etching-*** *Lifetime analysis of dilute chemistry wafer cleaning – Single wafer cleaning*
Module 4 : Semiconductor Manufacturing Technology **9 Hour**
Photolithography- photoresist, pattern transfer- E beam lithography, Etching-wet and dry etching and doping-Diffusion and ion implantation, Physical and Chemical vapor deposition.
Module 5: Modern Semiconductor Manufacturing Technology **9 Hour**
Atomic layer deposition, Electrodeposition, Fundamental of chemical mechanical planarization, Wafer thinning and singulation- Thinning process and equipment, Laser technology, Packaging – Wafer bumping and redistribution technology.

Learning Resources	1. *R. E. Novak, J. Ruzyllo, Hattori, T, "Cleaning technology in semiconductor device manufacturing, Proceedings of sixth international conference", The Electrochemical Society USA. 2000.* 2. *Karen A. Reinhardt, Richard F. Reidy, "Handbook of Cleaning in Semiconductor Manufacturing: Fundamental and Applications", Wiley online library, 2010.*	3. *Hwaigu Geng, "Semiconductor manufacturing handbook", Second edition, McGraw-Hill Education, 2018.* 4. *Gary S May and Costas J Spanos, "Fundamentals of Semiconductor Manufacturing and Process control", Wiley Interscience,2006.*

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) - By the Course Faculty				By The CoE	
		Formative CLA-I Average of unit test (50%)		**Life Long Learning** CLA-II- Practice (10%)		**Summative** Final Examination (40% weightage)	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30%	-	30%	-	30%	-
Level 2	Understand	30%	-	30%	-	30%	-
Level 3	Apply	20%	-	20%	-	20%	-
Level 4	Analyze	20%	-	20%	-	20%	-
Level 5	Evaluate		-		-	-	-
Level 6	Create	-	-	-	-	-	-
	Total	100%		100%		100%	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Mr. N. Nagarajan, Vice President Engineering, EPCOGEN Pvt Ltd	*Dr. S. Sundaramoorthy, Professor, Puducherry Technological University*	*Dr G Keerthiga, SRMIST*

Course Code	21MCH233E	Course Name	QUALITY CONTROL IN CHIP MANUFACTURING	Course Category	E	ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Chemical Engineering*	Data Book / Codes / Standards	*Nil*		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	To build foundational understanding of quality control principles, their relevance in chip manufacturing, and their impact on yield and performance.
CLR-2 :	To enable students to understand the sources of contamination and techniques used to monitor and maintain control over semiconductor fabrication processes.
CLR-3 :	To provide knowledge of various inspection and metrology techniques critical to defect detection and process improvement in chip fabrication.
CLR-4 :	To train students in basic yield modeling, loss analysis, and understanding failure modes in semiconductor devices.
CLR-5 :	To introduce students to industry practices for continuous quality improvement and effective problem- solving methodologies.

Course Outcomes (CO):	*At the end of this course, learners will be able to:*	Program Outcomes (PO)											
		1	2	3	4	5	6	7	8	9	10	11	12
		Engineering Knowledge	Problem Analysis	Design/development of solutions	Conduct investigations of complex problems	Modern Tool Usage	The engineer and society	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning
CO-1 :	Explain the role and importance of quality control in semiconductor manufacturing and identify key parameters affecting product quality.	*1*		*2*									
CO-2 :	Describe and apply basic monitoring tools and interpret data for process control in semiconductor manufacturing.		*3*	*2*									
CO-3 :	Classify types of inspections used in fabs and evaluate their application for detecting manufacturing defects.	*2*		*2*									
CO-4 :	Analyze wafer yield data, identify failure modes, and propose corrective actions.			*2*		*2*							
CO-5 :	Apply quality tools and lean principles to identify process bottlenecks and suggest improvements in chip manufacturing.			*2*		*2*							

Module 1 :Introduction To Quality Control In Semiconductor Manufacturing	**9 Hour**
Overview of Semiconductor Manufacturing Processes, Need for Quality Control in Chip Fabrication, Historical Development of Quality in Microelectronics, Basic Quality Terminologies and Metrics, Yield, Defects, Process Variation and Control, Types of Defects in Semiconductor Manufacturing, Cleanroom Concepts, Quality Standards in Industry	
Module 2 :Contamination Control & Contamination Monitoring Techniques And Strategies	**9 Hour**
Fundamentals of Contamination Control, Sources of Contamination, Pertinent Standards, Electrostatic Discharge Methods, Fundamentals of ESD Control, ESD and Contamination Control, Concept of Statistical Process Control, Control Charts for Variables and Attributes, Process Capability Indices	
Module 3: Defect Detection and Inspection Methods	**9 Hour**

Introduction to Wafer Inspection Techniques, Optical Inspection Systems, Scanning Electron Microscopy (SEM) and E-Beam Tools, Atomic Force Microscopy (AFM) Basics, Metrology Tools: CD-SEM, Profilometers, Defect Classification and Root Cause Analysis, Inline and End-of-Line Inspection Strategies, Automatic Defect Classification Overview
Module 4 : Yield Analysis and Failure Modes **9 Hour**
Yield Models, Yield Loss Mechanisms and Pareto Analysis, Wafer Mapping and Bin Data Analysis, Failure Modes and Effects Analysis (FMEA), Reliability Testing Basics, Statistical Yield Prediction Techniques, Packaging Defects and Final Test Failures
Module 5: Quality Improvement Strategies in Semiconductor Industry **9 Hour**
Root Cause Analysis Tools, Lean Manufacturing Principles in Semiconductor Fabs, Six Sigma DMAIC Approach, Total Quality Management (TQM) in Fab Environments, Quality Audits and Continuous Improvement Cycles.

Learning Resources	1. *May, Gary S., and Costas J. Spanos. "Introduction to Semiconductor Manufacturing", John Wiley & Sons, 2006, ISBN: 0471784060.* 2. *Geng, Hwaiyu, Semiconductor Manufacturing Handbook, McGraw-Hill Education, New York, 2nd ed. (2018)* 3. *Roger W.Welker, R. Nagarajan, and Carl E. Newberg, "Contamination and ESD Control in High-Technology Manufacturing", IEEE Press, Wiley-Interscience, 2006*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA) Formative CLA-1 Average of unit test (50%)		Continuous Learning Assessment (CLA) Life-Long Learning CLA-2 (10%)		Summative Final Examination (40% weightage)	
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30%	-	25%	-	30%	-
Level 2	Understand	30%	-	25%	-	30%	-
Level 3	Apply	20%	-	25%	-	20%	-
Level 4	Analyze	20%	-	25%	-	20%	-
Level 5	Evaluate	-	-	-	-	-	-
Level 6	Create	-	-	-	-	-	-
	Total	100 %		100 %		100 %	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
Mr. N. Nagarajan, Vice President Engineering, EPCOGEN Pvt Ltd	*Dr. S. Sundaramoorthy, Professor, Puducherry Technological University*	*V. Ganesh, SRM IST*