ACADEMIC CURRICULA

POST GRADUATE DEGREE PROGRAMMES

Master of Technology

(Choice Based Flexible Credit System)

Regulations 2021

Volume – 24
Syllabi for School of Electrical Engineering Programmes

Professional Core and Elective Courses

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Chengalpattu District 603203, Tamil Nadu, India

ACADEMIC CURRICULA

VLSI Design

Professional Core Courses

Regulations 2021

SRM INSTITUTE OF SCIENCE & TECHNOLOGY
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SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Chengalpattu District 603203, Tamil Nadu, India

Course Code	21ECC530J	Course Name	ELECTRONIC DESIGN AUTOMATION FOR ASIC AND FPGA	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							2	0	2	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*introduce the basics of hardware description languages and simulation types.*
CLR-2:	*explain the concepts and CAD tools for simulation and synthesis of digital circuits*
CLR-3:	*create insights into the theoretical concepts of device modeling and simulation using TCAD tools.*
CLR-4:	*provide students with the knowledge, skills, and practical experience needed to work effectively with EDA tools and methodologies for analog and digital circuits.*
CLR-5:	*gives an idea about the tools and techniques for integrated circuit design and Implementation*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*describe the functionality of a circuit using languages like Verilog or VHDL.*	*3*	*2*	*-*
CO-2:	*translate high-level descriptions (HDL code) into a gate-level net list that represents the logic of the design with functional design and verification.*	*3*	*2*	*1*
CO-3:	*explain, the process of creating mathematical representations or models that describe the behaviour of electronic devices.*	*3*	*2*	*1*
CO-4:	*simulate and verify the functionality of analog, digital and mixed signal circuits,*	*3*	*2*	*2*
CO-5:	*implement Frontend and Back-end IC design using EDA tools for analog, Digital, Mixed Signal and RF integrated circuit.*	*3*	*2*	*2*

Module-1 – Simulation and Synthesis Using HDL	***12 Hour***
Simulation-Types of Simulation, Logic Systems, Working of Logic Simulation, Cell Models, Delay Models, State Timing Analysis, Formal Verification, Gate level modelling, Behavioral modelling, Data flow modelling, Switch-Level Simulation, Logic Synthesis, Synthesis in design process of Combinational and sequential circuits, Memory Synthesis, FSM Synthesis, Performance-Driven Synthesis *Practice on different modelling level of simulation and Synthesis of Digital logic circuits: Combinational and Sequential circuits*	
Module-2 – FPGA Design	***12 Hour***
FPGA Building blocks, FPGA based digital system design, Usage areas of FPGAs, Configuring and Programming of FPGA, FPGA design and debug cycle, Simulation vs. Debugging in Hardware. *Practice on digital system design projects using FPGAs.*	
Module-3 - Technology TCAD	***12 Hour***
Device Modelling — From Physics to Electrical Parameter Extraction, MOS Technology and Intrinsic Device Modelling, Intrinsic MOS Transistor and modelling techniques, Substrate Effects on MOS Transistors, Device Technology Alternatives, *Practice on Device Modelling and Simulation using TCAD: Diode, MOS transistor*	
Module-4 – Analog and Digital Circuit Design and Simulation	***12 Hour***
Analog and digital design flow, PSPICE Models for Transistors, Design and Analysis of Analog and Digital Circuits, A/D & D/A Sample and Hold Circuits, and Digital System Building Blocks. *Practice on Design and Analysis of Analog and Digital Circuits Using PSPICE.*	
Module-5 – EDA Tools for ASIC Implementation and Verification	***12 Hour***
ASIC design flow, EDA Tools for Analog and Digital, circuit design and implementation, Design Entry, Design Verification, Physical design and GDS-II file for fabrication. *Practice on implementation of analog, digital and RF circuits using EDA tools and obtain GDSII file.*	

Learning Resources	1. Robert B. Reese, Mitchell A. Thornton, "Introduction to Logic Synthesis using Verilog HDL", Springer, 2022 2. Cem Ünsalan, Bora Tar, Digital System Design with FPGA, Implementation using Verilog and VHDL", Mc Graw Hill, 2017. 3. J.Bhaskar, "A Verilog HDL Synthesis", BSP, 2003.	4. Louis Scheffer, Luciano Lavagno, Grant Martin," EDA for IC Implementation, Circuit Design and Process Technology", Taylor and Francis 2006. 5. M.J.S.Smith, "Application-Specific Integrated Circuits", Addison Wesley.1997 6. M.H.Rashid, "SPICE FOR Circuits and Electronics Using PSPICE", (2/E) Prentice Hall, 1992.

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Final Examination (40% weightage)	
		Formative CLA-1 Average of unit test (45%)		Life-Long Learning CLA-2 (15%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	20 %	-	-	20 %	30 %	-
Level 2	Understand	20 %	-	-	20 %	40 %	-
Level 3	Apply	30%	-	-	30%	30 %	-
Level 4	Analyze	30%	-	-	30%	-	-
Level 5	Evaluate	-	-	-	-	-	-
Level 6	Create	-	-	-	-	-	-
	Total	100 %		100 %		100 %	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Sethupathy Balakrishnan, Lead Application Engineer, Cadence Designs Systems	1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University	1. Dr. J. Manjula, SRMIST
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	

Course Code	21ECC531J	Course Name	DIGITAL SYSTEMS DESIGN USING HDL	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand behavioural and RTL modelling of digital circuits*
CLR-2:	*understand the basic CMOS circuit, characteristics, and performance*
CLR-3:	*learn the designing of combinational circuits using different CMOS logic*
CLR-4:	*learn the designing of sequential circuits and FSM*
CLR-5:	*get an idea about designing Datapath and memory systems and how to implement such design*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*apply Verilog HDL to model digital systems, utilizing various abstraction levels*	3	2	
CO-2:	*analyse the basic CMOS circuit, including characteristics and performance metrics, demonstrating comprehension.*	3	2	
CO-3:	*evaluate and synthesize the design of combinational circuits using different CMOS logic, showcasing application of knowledge.*	3	2	
CO-4:	*synthesize the circuit design of latches, flip-flops, and Finite State Machines (FSMs) based on comprehension and application.*		2	3
CO-5:	*apply various optimization methods in the design of data paths and memory systems, demonstrating synthesis at higher cognitive levels.*		2	3

Module-1 - Basic Concepts - Verilog	***15 Hour***
Basic concepts, Identifiers, Value set, Data types, Parameters, Operands, Operators, Modules and ports, Gate-level Modelling, Behavioural Modelling, Tri state gates, MOS Switches, Bidirectional switches, Switch level modelling, Combinational UDP, System task, System functions, Introduction to synthesis, Verilog HDL synthesis, Synthesis Design flow, System Verilog *Practice on : Design and simulate the combinational circuits, Design and Implementation using task and function, Design and Verify Circuit Using Switch Level Modelling.*	
Module-2 - Principle of MOS Transistor's and CMOS Inverter	***15 Hour***
MOS Transistors, Threshold Voltage, Characteristics of MOS Transistor, Derivation of Drain Current, Short Channel Effects, Transfer Characteristics of CMOS Inverter, Transfer Characteristics of CMOS Inverter, Design of Logic Gates Circuit Using NMOS load, Design of Logic Gates Using PMOS load, Design of Logic Gates Using CMOS, Design and Verify Sequential Circuits, Stick Diagrams, Stick Diagrams Example, Case Study: Optimization of a CMOS inverter for minimum power consumption and delay. *Practice on: Implement CMOS Inverter using NMOS, PMOS, and CMOS configurations, Implementation of logic gates using CMOS, Implementation of Boolean expression using CMOS*	
Module-3 - CMOS – Combinational Circuits	***15 Hour***
Static CMOS design, complementary CMOS, static properties, complementary CMOS design, power consumption in CMOS logic gates, dynamic or glitching transitions. Design techniques to reduce switching activity, ratioed logic-DC VSL - pass transistor logic, differential pass transistor logic, design using differential pass transistor logic, sizing of level restorer, Sizing in pass transistor-Dynamic CMOS design - Basic principles - Domino logic optimization of Domino logic. NPCMOS-logic style selection. Designing logic for reduced supply voltages, design and analyse low power circuit, Case Study: Design and analysis of a low-power CMOS combinational circuit for a specific application, considering different logic optimization techniques. *Practice on: Design and implement Booth Multiplier, Design and simulate FSM design, Implement and optimize a CMOS circuit using Domino logic*	
Module-4 - CMOS – Sequential Circuits	***15 Hour***
Timing Metrics for Sequential Circuit, Latches Vs Registers - Static Latches and Registers Biostability Principle, Multiplexer Based Latches, Master Slave Edge Triggered Registers, Non-ideal Clock Signals, Low Voltage Static Latches - Static SR Flip Flop, C2MOS Register, Dual Edge Registers, True Single Phase Clocked Registers, Pipelining to Optimize Sequential Circuit - Pipelining to Optimize	

Sequential Circuit, Choosing a Clocking Strategy - Problem Solving, Design Circuit Using Pipeline Concept, Case Studies: Implementation of a Pipelined Processor with emphasis on optimizing clock cycles. Design and analysis of a low-power sequential circuit using advanced clocking strategies. *Practice on: Design and Verify Pipelined Based Circuit Latch, Design and verify the static latches, Design and Implement FIR Filter/FIR Filter With Pipelining*
Module-5 – Datapath and Memory System Design ***15 Hour***
Adder – Carry Select Adder, Adder – Carry Save Adder, Multiplier – Baugh-Wooley, Multiplier – Wallace Tree, Booth Multiplier, Universal Shift Register, Barrel Shifter, Power and Speed Trade-off's in Datapath Structures, Memory – RAM Static RAM, Dynamic RAM, Serial Access Memory – ROM, Content Addressable Memory, Content Addressable Memory, Finite-State Machines, Types of Finite-State Machines, Case Studies: The Programmable Logic Array (PLA), A 4-bit SRAM. *Practice on: Design and Simulate Universal Shift Register, Design and Simulate Memory Circuits, Design a Traffic Light Controller for an Intersection with a Main Street, a Side Street, and a Pedestrian Crossing or a Vending Machine*

Learning Resources	1. *Samir palnitkar, "Verilog HDL", Pearson education, Second Edition,20O3.* 2. *Jan.M.Rabaey., Anitha Chandrakasan Borivoje Nikolic, "Digital Integrated Circuits", Second Edition* 3. *Michael D. Ciletti,Advanced Digital Design with Verilog HDL, Second Edition, Pearson,2011.*	4. *Neil H.E Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Addition Wesley, 1998.* 5. *Sung Mu Kang, Yusuf Leblebici "CMOS Digital Integrated Circuits", 3rd edition, Tata McGraw-Hill, 2002.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20 %*	-	-	*20 %*	*20 %*	-
Level 2	*Understand*	*20 %*	-	-	*20 %*	*20 %*	-
Level 3	*Apply*	*30 %*	-	-	*30 %*	*30 %*	-
Level 4	*Analyze*	*30 %*	-	-	*30 %*	*30 %*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	100 %		100 %		100 %	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. *Mr. Sethupathy Balakrishnan, Lead Application Engineer, Cadence Designs Systems*	1. *Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	1. *Dr. R. Prithiviraj SRMIST*
	2. *Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram*	2. *Dr. A. Maria Jossy, SRMIST*
		3. *Dr. E. Chitra, SRMIST*

Course Code	21ECC532T	Course Name	SOLID STATE DEVICES AND MODELING	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	1	0	4

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*identify the basic concept and application of quantum mechanics*
CLR-2:	*illustrate the basics of semiconductor in equilibrium and non-equilibrium*
CLR-3:	*analyze the physical effects in PN junction and metal-semiconductor junction*
CLR-4:	*explain the physics of MOS capacitor and working of MOSFETs*
CLR-5:	*illustrate the scaling and short channel effects in MOSFET compact modelling*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand the principle of Schrodinger's wave equation and analyze the concept of energy band diagram*	*3*	*2*	*-*
CO-2:	*apply quantum theory to semiconductor in equilibrium and non-equilibrium*	*3*	*2*	*-*
CO-3:	*apply physical effects in PN Junctions and metal-semiconductor junction*	*3*	*2*	*-*
CO-4:	*identify the basic concepts used in MOS capacitor and MOSFET*	*3*	*-*	*3*
CO-5:	*apply the concepts of scaling and short channel effects in MOSFET Modelling*	*3*	*2*	*-*

Module-1 - Introduction to Quantum Mechanics	***12 Hour***
Principles of Quantum Mechanics: Energy Quanta, Schrodinger's Wave Equation, Physical Meaning of the Wave Function, Applications of Schrodinger's Wave Equation: Electron in Free Space, The Infinite Potential Well, The Finite Potential Well, Allowed and Forbidden Energy Bands, The E-k-Space Diagram, The Energy Band and the Band Model, Drift Current, Electron Effective Mass, Concept of the Hole, Metals, Insulators, and Semiconductors, Direct and Indirect Band Gap Semiconductors.	
Module-2 - Semiconductor in Equilibrium and Non-equilibrium	***12 Hour***
Density of States Function, The Fermi–Dirac Probability Function, Charge Carriers in Semiconductors, Thermal Equilibrium Distribution of Electrons and Holes, The Intrinsic Carrier Concentration & The Intrinsic Fermi-Level Position, The Extrinsic Semiconductor: Equilibrium Distribution of Electrons and Holes, The n_0p_0, Product, Fermi-Dirac integral, Position of Fermi Energy Level, Degenerate and Nondegenerate Semiconductors, Charge Neutrality: Compensated Semiconductors, Complete Ionization and Freeze-Out, Drift and Diffusion Process, Carrier Generation and Recombination, Characteristics of Excess Carriers.	
Module-3 - The P-N and Metal Semiconductor Junction	***12 Hour***
Basic Structure of the PN Junction, Built-in Potential Barrier at zero bias, Electric Field at zero bias, Space charge width at zero bias, Reverse Applied Bias, Space Charge Width and Electric Field at reverse bias, Nonuniformly Doped Junctions: One-Sided Junctions, Linearly Graded Junction, PN Junction Current, Tunnelling Mechanism, Junction Breakdown: Zener Effect and The Avalanche Effect, The Schottky Barrier Diode, Metal-Semiconductor Ohmic Contact.	
Module-4 - Metal Insulator Semiconductor Devices	***12 Hour***
The Two-Terminal MOS Structure: Energy-Band Diagrams in Accumulation, Depletion and Inversion Regions, Depletion Layer Thickness, Threshold Voltage, Flat-Band Voltage, Capacitance-Voltage Characteristics for N-MOS and P-MOS, Ideal C-V Characteristics, Frequency Effects, The Basic MOSFET Operation: Depletion and Enhancement MOSFETs, Substrate Bias Effects, Subthreshold Conduction, Subthreshold slope	
Module-5 – MOS Compact Modelling	***12 Hour***

MOSFET Scaling, Moore Law, Short channel effects: Channel length modulation, Velocity saturation, Mobility degradation, Hot carrier effects, Punch through, Ballistic Transport, Square law Model; Level 1 in SPICE, Level 3 in SPICE, History of BSIM models, BSIM family of Compact device models, BSIM6 model, BSIM-CMG model, BSIM-IMG model, Quantum Transport models -: Tunneling, Schrodinger equation and free particle, potential step, potential barrier, Key issues in MOSFET modeling, Introduction to the TCAD Simulation Tool, Examples of TCAD Simulations

Learning Resources	1. *Donald Neamen, Dhrubesh Biswas, Semiconductor Physics and Devices, McGraw Hill, 4th ed, 2012.* 2. *S. M. Sze, Physics of Semiconductor Devices, John Wiley, 3rd ed, 2005.* 3. *Pallab Bhattacharya, Semiconductor Opto electronic Devices, 2nd ed, PHI, 2017.*	4. *Nandita Dasgupta and Amitav Dasgupta, Semiconductor Devices: Modelling and Technology Prentice-Hall of India Pvt.Ltd; 1st ed, 2004.* 5. *Dragica Vasileska, Stephen M. Goodnick, Gerhard Klimeck, Computational Electronics, Semiclassical and Quantum Device Modeling and Simulation, CRC Press, 1st ed, 2017.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. *Mr. Abhijeet Pathak, Western Digital, Bangalore, India.*	1. *Dr. Kumar Prasannajit Pradhan, IIITDM, Kancheepuram*	1. *Dr. Aditya Nath Bhatt, SRMIST*
	2. *Dr GP Mishra, NIT Raipur*	2. *Dr. Rajesh Agarwal, SRMIST*
		3. *Dr. Soumya Ranjan Routray, SRMIST*

Course Code	21ECC533J	Course Name	ANALOG CIRCUITS AND SYSTEM DESIGN	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	0	2	4

Pre-requisite Courses	Nil	Co- requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	understand the operation and design of different MOS amplifier circuits
CLR-2:	emphasize the basics of analog CMOS sub-circuits and its design
CLR-3:	characterize the basics of differential amplifiers and its design analysis
CLR-4:	gain knowledge of various operational amplifiers
CLR-5:	understand and analyse the different oscillator circuits to determine the frequency of oscillation and identify the various components of PLL and its operation

Course Outcomes (CO):	At the end of this course, learners will be able to:	Programme Outcomes (PO)		
		1	2	3
CO-1:	analyse and design of MOS amplifier circuits under various load and understand the frequency response	3	2	1
CO-2:	understand the operation of CMOS current mirrors, biasing circuits and filters	3	2	1
CO-3:	design basic differential amplifiers	3	2	1
CO-4:	understand the operation of Operational amplifiers	3	2	1
CO-5:	elucidate and design oscillator circuits to meet certain specifications and illustrate the function of PLL and its performance	3	2	1

Module-1 - CMOS Amplifier	15 Hour
Introduction to Analog Design Single stage amplifiers - Common source Amplifier with Resistive load and Diode connected load, Common source amplifier with source Degeneration, Source Follower, Common Gate amplifier, Noise analysis, Frequency response of amplifiers, Multistage Amplifiers- Cascode Amplifier, Folded Cascode amplifier, Noise analysis and frequency response of Cascode stage amplifier. Practice on Common source amplifiers with different loads, Source follower	
Module-2 - Current Mirror and Bandgap reference Sources	**15 Hour**
General Properties, Basic Current mirrors, Cascode current mirrors, Active Current Mirrors, Block Diagram of Band gap reference circuits, Supply Independent Biasing, Temperature independent Reference circuit, PTAT Current Generation, Constant $-G_m$ biasing. Practice on of Basic current mirror, Cascode Current mirror, Voltage Reference circuits	
Module-3 - Differential amplifier	**15 Hour**
DC transfer characteristics of source coupled pair, small signal analysis, Single-ended operation and Differential operation, Basic differential pair, Qualitative and Quantitative analysis of differential amplifier, Common-mode response, Differential pair with MOS loads, Frequency response of Differential amplifier, Noise in differential amplifier. Practice on different configurations of differential amplifiers	
Module-4 - Operational Amplifier	**15 Hour**
Performance parameters of op-amp, Block Diagram, One stage op-amp, Two Stage op-amp, Voltage gain of two stage op-amp, Input common range and output swing, Slew rate, Power supply rejection ratio, Gain Boosting, Frequency response of op-amp, Folded Cascode CMOS op-amp, Voltage gain and frequency response of Folded Cascode op-amp, Rail to rail input operation, Noise in op-amps. Practice on one stage and two stage operational amplifiers	
Module-5 – Oscillators and Phase Locked Loops	**15 Hour**

Ring oscillator, two stage and three stage ring oscillators, LC oscillators, Cross Coupled oscillator, Voltage controlled oscillators, Tuning range of VCOs, Basic PLL topology and characteristic parameters, Phase detector, Charge Pump PLL, Problem of lock acquisition, non-ideal effects in PLL, Jitter in PLLs, Transient response of PLL in the locked state, Applications of PLL: Frequency multiplication. Case Study: Design of Ring Oscillator for specific practical circuit, Design of VCO for a particular locking frequency *Practice on different types of Cross-coupled Oscillator, Colpitts Oscillators and PLL circuit*

Learning Resources	1. *Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog Integrated Circuits", 5th Edition, Willey International, 2009.* 2. *Allen, Holberg, "CMOS analog circuit design", 3rd Edition, Oxford University Press, 2012* 3. *Behzad Razavi, "Design of analog CMOS integrated circuits", 2nd Edition, McGraw Hill, 2017*	4. *Adel S. Sedra, Kenneth C. Smith, "Microelectronic Circuits" 7th Edition, Oxford University Press, 2015* 5. *Ndjountche, Tertulien," CMOS Analog Integrated Circuits: High-Speed and Power-Efficient Design", 2nd Edition, CRC Press, 2019.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	-	*20%*	*20%*	-
Level 2	*Understand*	*20%*	-	-	*20%*	*20%*	-
Level 3	*Apply*	*30%*	-	-	*30%*	*30%*	-
Level 4	*Analyze*	*30%*	-	-	*30%*	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. *Mr. Sethupathy Balakrishnan, Lead Application Engineer, Cadence Designs Systems.*	1. *Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	1. *Dr. K. Ferents Koni Jiavana, SRMIST*
	2. *Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram*	2. *Dr. J. Manjula, SRMIST*

Course Code	21ECC534J	Course Name	VLSI PHYSICAL DESIGN AUTOMATION	Course Category	C	PROFESSIONAL CORE	L	T	P	C
							3	0	2	4

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*learn the VLSI design flow, design styles and design rules along with the basics of graph theory*
CLR-2:	*discuss the methods of Partitioning and Clustering*
CLR-3:	*interpret the methods of placement and floor planning*
CLR-4:	*describe the methods of Routing and layout compaction*
CLR-5:	*estimate the physical design of FPGA and MCMS*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand the basic concepts of VLSI Physical Design Automation*	3	1	1
CO-2:	*expose to hierarchical modelling concepts and the necessary knowledge to perform partitioning and clustering algorithms.*	3	1	2
CO-3:	*design a compact IC using floor planning and placement methodologies*	2	1	3
CO-4:	*analyse the routing process to achieve the performance of the digital design*	3	1	2
CO-5:	*design and develop physical design algorithms in optimization of VLSI layout*	3	1	2

Module-1 Introduction to VLSI Physical Design Automation	***15 Hour***
Electronic Design Automation (EDA), VLSI design flow, VLSI design styles, physical design automation, Physical design optimization, Algorithms and complexity, Graph theory terminology- Graph search algorithms- Spanning tree algorithms- shortest path algorithms *Practice on design of functional verification of logic gates, Practice on design of combinational circuits*	
Module-2 Partitioning and Clustering	***15 Hour***
Basic Concepts- Partitioning, Kernighan-Lin, Fiduccia- Mattheyses, Basic Concepts- Clustering - Agglomerative Clustering - Rajaraman and Wong algorithm- Hyper edge coarsening - Modified Hyper edge coarsening - Practice problems in Clustering *Practice on functional verification of Sequential circuit using 90nm Technology using Cadence RTL Compiler (RC) tool.* *Practice on Implementation of KL Partition algorithm in 90nm Technology and analyze the implemented circuit and check for the changes in delays, setup and hold times*	
Module-3 - Compaction, Floor planning and Placement	***15 Hour***
Compaction and it's aspects in Physical design-1D and 2D compaction-Liao Wong algorithm-Floorplan based design methodologies- Introduction to Floor planning- Slicing and Non slicing floorplan-Polar graphs representation-Sequence-pair-Shape functions- Non-slicing methods: Introduction to Placement - Problem formulation and classification - Enhancement of Min- cut placement - Placement algorithm using Simulated annealing - Placement algorithm using Genetic algorithm *Practice on implementation of FM Partition algorithm in 90nm Technology analyze the implemented circuit and check for the changes in delays, setup and hold times* *Practice on analysis of a circuit in the power planning stage using 90nm Technology*	
Module-4 - Routing	***15 Hour***

Channel routing and terminologies: Global Routing- Problem Formulation- Classification of Global Routing- Maze routing algorithm- Lee's algorithm- Line Probe algorithms- Shortest Path algorithms: Steiner Tree based algorithms- Channel routing-Terminologies-Constraint graphs-Detailed Routing: Problem formulation- Classification of Detailed routing- Two-layer channel routing algorithms: Left Edge algorithm- Dogleg Routing algorithm-Clock tree routing- H-tree algorithm *Practice on Routing and placement Analysis* *Practice on pre-Placement analysis in EDA Environment*
Module-5 – Practical Design Issues and automation of simulation ***15 Hour***
Elmore Delay based routing constructions – Physical design techniques in simulation mechanisms- Delay model-Data structures in event driven simulation- Switch level techniques-Partitioning for simulation- Physical Design Automation of FPGAs-Physical design automation of MCMS. *Practice on generation of Clock Tree Synthesis (CTS) of a synchronous circuit using 90nm Technology* *Practice on deciding on a final optimum back-end design of a circuit using 90nm Technology* *Mini project*

Learning Resources	*1. Naveed Sherwani, Algorithms for VLSI physical design Automation, Kluwer Academic Publishers, 2010.* *2. Sung Kyu Lim, "Practice Problems in VLSI physical design Automation", Springer, 2008*	*3. Algorithms for VLSI Design Automation-Sabih Gerez-Wiley publishers, 2006.* *4. Sadiq M. Sait, Habib Youssef, "VLSI Physical design automation theory and Practice", World Scientific Publishing, 1999*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life-Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	*-*	*-*	*20%*	*20%*	*-*
Level 2	*Understand*	*20%*	*-*	*-*	*20%*	*20%*	*-*
Level 3	*Apply*	*30%*	*-*	*-*	*30%*	*30%*	*-*
Level 4	*Analyze*	*30%*	*-*	*-*	*30%*	*30%*	*-*
Level 5	*Evaluate*	*-*	*-*	*-*	*-*	*-*	*-*
Level 6	*Create*	*-*	*-*	*-*	*-*	*-*	*-*
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Dr. Sandeep Patil, CEO, EspinNanotech Solutions, IIT Kanpur	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. S.Roji Marjorie, SRMIST*
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	*2. Mr. M. Maria Dominic Savio, SRMIST*

ACADEMIC CURRICULA

VLSI Design

Professional Elective Courses

Regulations 2021

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Deemed to be University u/s 3 of UGC Act, 1956)

Kattankulathur, Chengalpattu District 603203, Tamil Nadu, India

Course Code	21ECE531T	Course Name	SIGNAL PROCESSING TECHNIQUES FOR VLSI	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand the basic computation item in VLSI Signal Processing.*
CLR-2:	*familiar with concepts of iteration Bound, Retiming, Folding*
CLR-3:	*understand the Design Efficient Pipelining filter design*
CLR-4:	*learn the concept of parallel processing of FIR filter for low power design*
CLR-5:	*understand the concept of Bit-level arithmetic architectures*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand VLSI design methodology for signal processing systems.*	3	2	-
CO-2:	*be familiar with VLSI algorithms and architectures of DSP.*	2	-	2
CO-3:	*be able to implement basic architectures for DSP using CAD tools.*	-	2	2
CO-4:	*design the pipelined and parallel FIR Filter*	2	-	3
CO-5:	*be familiar with low power design concepts of ASICs and high-speed design*	-	3	2

Module -1 Introduction to DSP System	***9 Hour***
Iteration Bound – data flow graph representations – loop bound – iteration bound – problems on iteration bound techniques - various mechanism for iteration bound computation – Longest path matrix – problems on LPM techniques – pipelining and parallel processing – Introduction pipelining of FIR Digital filter, parallel filter – pipelining processing for low power – parallel processing for low power – problems on low power pipelined and parallel process system. Introduction to retiming – problems on retiming mechanism.	
Module -2: Systolic Architecture and Algorithm Strength Reduction	***9 Hour***
Algorithm strength reduction in filter – Transforms – 2-parallel FIR Filter – 2-parallel Fast FIR Filter – DCT algorithm architecture transformation – parallel architecture for rank order filter - ODD-EVEN merge sorter architecture – parallel rank order filter introduction and design – problems related to ODD-EVEN merge sort filter – problem on rank order filter – problem on ODD-EVEN merge sort – Systolic architecture design – Introduction – FIR systolic array sample problems	
Module- 3- Fast Convolution	***9 Hour***
Fast convolution – Cook –Toom algorithm –problem – modified cook-toom algorithm – problems- pipeline and parallel recursive and adaptive filter – Inefficient/efficient interleaving architecture – parallel recursive structures - interleaving mechanism – look-ahead pipelining in FIR filter - problem on look-ahead techniques – problems on interleaving – problem on parallel recursive structure – application of look-ahead pipelining – clustered Look-ahead pipelining.	
Module -4 - Bit-Level Arithmetic	***9 Hour***
Scaling and round-off noise – scaling operation, round-off noise – state variable description of digital filters – scaling and round-off noise computation – Round-off noise in pipelined first –order filters. Problems on round-off noise computation – Bit-level Arithmetic Architectures- parallel multiplier sign extension – parallel carry-ripple array multiplier – parallel carry-save array multiplier tabular form and implementation – 4x4 bit Baugh Wooley carry save array multiplier and implementation. Operation description of parallel carry save – problems on bit-arithmetic – application study on carry save multiplication.	

Module-5 - High Performance Algorithm for ASIC	**9 Hour**
Numerical Strength Reduction – Sub Expression elimination – Multiple Constant Multiplications – Iterative Matching – Linear transformations-Low power Design Techniques – Introduction to wave pipelining – Asynchronous pipelining bundled data versus dual-rail protocol- wave Pipelining in detail – Asynchronous pipelining – introduction – Detail description on Asynchronous pipelining mechanism – Data vs Dual Rail Protocol – needs for low power VLSI chips, charging and discharging capacitance – CMOS leakage current – basic principles of low power design.	

Learning Resources	1. *Keshab.K. Parhi, "VLSI Digital Signal Processing Systems: Design and Implementation", Wiley, NY 1999* 2. *Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic publishers, 1988.* 3. *Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", 1988.*	4. *S. Y. Kung, H.J. White House T. Kailath, "VLSI and Modern Signal Processing", Prentice HALL,1985.* 5. *Jose E. France, Yannis Tsividis, "Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall,1994.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Dr. Sandeep Patil, CEO, EspinNanotech Solutions, IIT Kanpur	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. J. Selvakumar, SRMIST*
	2.Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	

Course Code	21ECE532T	Course Name	HARDWARE DESIGN AND SCRIPTING LANGUAGE	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand the basic features of System C.*
CLR-2:	*construct the different types of digital systems in System C*
CLR-3:	*utilize the basic constructs of System Verilog and Identify different types of System Verilog Advanced features.*
CLR-4:	*understand Assertions in System Verilog.*
CLR-5:	*construct basic programs in TCL.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand the basic concepts of System C*	1	-	1
CO-2:	*analyse Combinational and Sequential Circuits in System C*	2	2	2
CO-3:	*gain knowledge on the basic conventions in System Verilog and System Verilog advanced features.*	2	-	2
CO-4:	*utilize the Assertion feature in System Verilog*	3	3	2
CO-5:	*utilize various concepts in TCL*	3	2	2

Module-1 – System C	***9 Hour***
Introduction to System C, Design Methodology, Data types –Value holders, bit, arbitrary width logic type, Integer type, Resolved type, User-defined type, Modelling combinational logic - SC -module, Reading and writing port signals, Logical operators, Arithmetic operators, Relational operators, Programs using Operators, Vector Ranges, IF statement, Switch statement, Programs using IF, SWITCH Statements, Loops, methods, Structures, Delta delay, Programs on Adder, Multiplexer, Decoder, Encoder, Priority encoder, Modelling flip flops and latches.	
Module-2 - Advanced Features of System C	***9 Hour***
Modeling an FSM-Mealy FSM, Moore FSM, Universal shift register, Counters- Modulo N counter, Johnson counter, Gray code up-down counter, Writing a Test bench, Simulation control, SC-thread process, Dynamic sensitivity, Constructor arguments, Ports, Interfaces and Channels, Shared data members, Fixed point types, Module, Simulation Algorithm, Run time environment	
Module-3 - System Verilog	***9 Hour***
Literal values, Data types- String data type, User-defined types, Enumerations data type, Arrays –Dynamic Arrays, Associative arrays, Data declarations, Attributes, Operators-Assignment, Real, Streaming, conditional, Operator overloading, Procedural statements and Control, Flow Process, Tasks and Functions.	
Module-4 - Advanced Features of System Verilog	***9 Hour***
Classes -Objects, Methods, Static Methods, Casting, Chaining Constructors, Data hiding, Encapsulation, Parameterized classes, Polymorphism, Classes and structures, Random constraints and variables, Randomization methods, Assertions, Boolean expressions, Sequences, Case studies -System Verilog assertion API, System Verilog coverage API.	
Module-5 – Scripting Language	***9 Hour***
TCL Fundamentals, Strings and Pattern Matching, TCL Data Structures-TCL Lists, Arrays, Control Flow Commands, Procedures and Scope, Eval Commands	

Learning Resources	1. *J. Bhaskar, "A System C Primer ", Star Galaxy publications, 2010.* 2. *System Verilog for Verification: A Guide to Learning the Test Bench Language Features by Chris Spear and Greg Tumbush, Springer 3rd Edition, 2012.* 3. *David C. Black, Jack Donovan, Bill Bunton, Anna Keist, System C: From the Ground Up, Springer 2nd Edition, 2005.*	4. *System Verilog 3.1 a-Language Reference Manual (Accelera's Extensions to Verilog 2001),2004* 5. *Brent Welch," Practical Programming in TCL and TK," Pearson; 4th Edition, 2003*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
Mrs. A. Suganya, Sr. Scientist and Head, Hardware Security Research Group, SETS, Chennai	1. *Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1.Dr. Sudhanya P, SRMIST*
	2. *Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram*	*2.Mrs. N. Saraswathi, SRMIST*

Course Code	21ECE533T	Course Name	LOW-POWER VLSI DESIGN	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	Nil	Co- requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Electronics and Communication Engineering	Data Book / Codes / Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1:	familiarize with the fundamental concepts of Low Power VLSI
CLR-2:	perceive the knowledge of Probabilistic Power Analysis
CLR-3:	introduce the concepts of Circuit and Logic Level Synthesis for Low Power
CLR-4:	explore the concepts of Special Power Reduction Techniques
CLR-5:	understand the concepts of Architectural Level Approaches and Advanced Techniques

Course Outcomes (CO):	At the end of this course, learners will be able to:	Programme Outcomes (PO)		
		1	2	3
CO-1:	comprehend the fundamental concepts of Low Power VLSI	2	-	-
CO-2:	acquire knowledge on Probabilistic Power Analysis	2	-	-
CO-3:	circuit and Logic Level Optimization of Low Power	3	2	-
CO-4:	gain knowledge on Special Techniques for Power Reduction	2	-	-
CO-5:	develop skills to explore Architectural-Level Approaches and Advanced Techniques	2	3	-

Module-1 - Introduction to Low Power VLSI	9 Hour
Introduction - Needs for Low Power VLSI, Charging and Discharging Capacitance, Short Circuit Current in CMOS Circuit- Inverter, Variation with Output Load and Input Signal Slope, CMOS Leakage Current- Reverse Biased PN-Junction, Subthreshold Channel Leakage, Leakage Current in Digital Design, Static Current, Basic Principles of Low Power Design- Reducing Switching Voltage, Reducing Capacitance, Reducing Switching Frequency, Reducing Leakage and Static Current, Low Power Figure of Merits	
Module-2 - Probabilistic Power Analysis	**9 Hour**
Random Logic Signals, Characterization of Logic Signals, Continuous and Discrete Random Signals, Probability and Frequency, Word-level and Bit-level Statistics, Probabilistic Power Analysis Techniques- Propagation of Static Probability in Logic Circuits, Transition Density Signal Model, Propagation of Transition Density, Gate Level Power Analysis using Transition Density, Signal Entropy, Power Estimation using Entropy	
Module-3 Circuit Level and Logic Level Synthesis for Low Power	**9 Hour**
Transistor and Gate Sizing- Sizing an Inverter Chain, Sizing for Dynamic Power Reduction and Leakage Power Reduction, Equivalent Pin Ordering, Network Restructuring, Network Reorganization- Transistor Network Partitioning and Reorganization, Adjustable Device Threshold Voltage, Gate Reorganization, Gated Clock FSMs, State Encoding, FSM Partitioning, Bus Encoding- Gray Coding, One Hot Coding, Bus Inversion Coding, T0 Coding, Precomputation Logic- Condition, Alternate Precomputation Architectures, Design Issues in Precomputation Logic	
Module-4 - Special Techniques for Power Reduction	**9 Hour**
Power Reduction in Clock Networks- Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, CMOS Floating Node- Tristate Keeper Circuit, Blocking Gate, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM Cell, Memory Bank Partitioning, Case study: Design of a FIFO Buffer	
Module-5 – Architectural-Level Approaches and Advanced Techniques	**9 Hour**
Switching Activity Reduction- Guarded Evaluation, Bus Multiplexing, Glitch Reduction by Pipelining, Parallel Architecture with Voltage Reduction, Voltage Scaling for Low Power- Multilevel Voltage Scaling, Challenges in Multilevel Voltage Scaling, Dynamic Voltage and Frequency Scaling- Latency Overhead, Adiabatic Computation- Complementary Adiabatic Logic, Power Efficiency of Adiabatic Logic, Adiabatic Charging and Amplification, Pass Transistor Logic Synthesis	

Learning Resources	1. Yeap, Gary K. Practical Low Power Digital VLSI Design. Springer Science & Business Media, 2012. 2. Roy, Kaushik, and Sharat C. Prasad. Low-power CMOS VLSI Circuit Design. John Wiley & Sons, 2009.	3. Pal, Ajit. Low-Power VLSI Circuits and Systems. Springer, 2014 4. Piguet, Christian. Low-Power CMOS Circuits: Technology, Logic design and CAD Tools. CRC press, 2018.	

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Final Examination (40% weightage)	
		Formative CLA-1 Average of unit test (50%)		Life-Long Learning CLA-2 (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	20%	-	20%	-	20%	-
Level 2	Understand	20%	-	20%	-	20%	-
Level 3	Apply	30%	-	30%	-	30%	-
Level 4	Analyze	30%	-	30%	-	30%	-
Level 5	Evaluate	-	-	-	-	-	-
Level 6	Create	-	-	-	-	-	-
	Total	100 %		100 %		100 %	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mrs. A. Suganya, Sr. Scientist and Head, Hardware Security Research Group, SETS, Chennai	1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University	1. Dr. Sukanya Ghosh, SRMIST
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	2. Dr. P. Aruna Priya, SRMIST
		3. Dr. Soumyaranjan Routray, SRMIST

Course Code	21ECE534T	Course Name	RECONFIGURABLE COMPUTING SYSTEMS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*familiarize wide range of reconfigurable hardware*
CLR-2:	*introduce architecture that enables high performance computation as well as the supporting application mapping process.*
CLR-3:	*ability to understand the computational architectures for FPGA*
CLR-4:	*explore different Optical reconfigurable architectures.*
CLR-5:	*focuses on specific, important field-programmable gate array (FPGA) applications, presenting case studies of interesting uses of reconfigurable technology.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand the fundamentals of the reconfigurable computing and reconfigurable architectures.*	3		
CO-2:	*articulate the design issues involved in reconfigurable computing systems with a specific focus on Field Programmable Gate Arrays (FPGAs) both in theoretical and application levels*	3		
CO-3:	*understand both how to architect reconfigurable systems and how to utilize them for solving challenging computational problems.*	3		
CO-4:	*understand the models for optical systems, algorithms and techniques for high performance applications*	3		
CO-5:	*explore important field-programmable gate array (FPGA) reconfigurable applications through case studies*	3	2	2

Module-1 - Reconfigurable Computing Hardware	***9 Hour***
Logic- The computational fabric, Logic Elements , Programmability .Array and interconnect, Interconnect Structures ,Programmability, Extending Logic Elements, RAM, Flash Memory, Antifuse, Fine-grained, Coarse-grained, RPF integration into traditional computing, Independent Reconfigurable Coprocessor Architecture Processor , RPF Architectures, operating system support for reconfigurable computing, Abstracted Hardware Resources, Flexible Binding, Scheduling, Evolvable FPGA, Artificial Evolution, Evolvable Hardware Digital Platforms	
Module-2 - Mapping Designs into Reconfigurable Platforms	***9 Hour***
Mapping designs into reconfigurable platforms, Structural mapping algorithm, Area oriented, performance driven mapping, power-aware mapping, Integrated mapping algorithms, Simultaneous Logic Synthesis, Integrated Retiming, Placement-driven Mapping, algorithms for heterogeneous resources, Mapping to Complex Logic Blocks, Mapping Logic to Embedded Memory Blocks, Mapping to Macrocells, The FPGA placement, Clustering, simulated annealing, VPR Annealing Algorithms Related Annealing, Algorithms Simultaneous Placement and Routing with Annealing, analytical placement, partition based placement.	
Module-3 - Computational Architectures for FPGA	***9 Hour***
Precision analysis for fixed point computation, Fixed-point number system, Multiple-word length Paradigm, Word length optimization, Analytic Peak Estimation, Distributed arithmetic, DA implementation, Mapping process, Mapping DA onto FPGAs, An application of DA on an FPGA, FPGA implementation of CORDIC processors. Case study: optimized fixed-point arithmetic, Hardware accelerated algorithms, optimized fixed-point arithmetic circuits in custom hardware.	
Module-4 - Optical Reconfiguration Model	***9 Hour***
Optical reconfigurable models, Basic algorithm techniques, Permutation Routing, Binary Prefix Sums, Algorithms for Optical Models, Basic Results, Sorting and Selection, Multiple Addition, Matrix Multiplication, Bit stream Generation Export Hardware, Complexity of Optical Models, Simulating PRAMs Simulating PRAMs example, Equivalence of One-Dimensional Models Relating the PR-Mesh and the LR-Mesh, Relating Two-Dimensional Optical Models Run time reconfigurability, Run time reconfigurability Design and implementation, Run-Time Reconfiguration Basic Concepts, Generic and Specific Problem.	
Module-5 – Case Studies of FPGA Applications	***9 Hour***
SPIHT Image Compression, SPIHT algorithm, SPIHT Coding Engine, Wavelets and the Discrete Wavelet Transform, The SPIHT Coding Phase, The SPIHT Coding Evaluation, Automatic Target Recognition Systems, Automatic target recognition algorithms, ATR implementations, The Implications of Floating Point for FPGAs, General Implementation Considerations of Adder and their types of Adder, Multiplier	

Implementation. Case study: Floating-point unit module – Xilinx Virtex-II Pro (or) ZYNQ XC 7Z020-1CLG400C – 650 MHZ ARM Cortex A9 dual core Processor, Implementation of PYNQ-Z2 -Python languages and libraries

Learning Resources	1. *Scott Hauck and Andre` DeHon, "Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation", Morgan Kaufmann, 2008.* 2. *Clive Maxfield, "The Design Warrior's Guide to FPGAs: Devices, Tools and Flows", Newnes, Elsevier, 2006*	3. *Ramachandran Vaidhyanathan and Jerry. L. Trahan "Dynamic Reconfiguration: Architectures and Algorithms", Kluwer Academic publishers, 2003.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*40 %*	-	*40 %*	-	*30 %*	-
Level 2	*Understand*	*40 %*	-	*40 %*	-	*40 %*	-
Level 3	*Apply*	*20 %*	-	*20 %*	-	*30 %*	-
Level 4	*Analyze*	-	-	-	-	-	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. T S Karthik, SRMIST*
2. Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com	*2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram*	*2. Dr. P Aruna Priya, SRMIST*

Course Code	21ECE535T	Course Name	CRYPTOGRAPHY AND HARDWARE SECURITY IN VLSI	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	Data Book / Codes/Standards		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1 :	*apply mathematical techniques to cryptography*
CLR-2 :	*describe principles, techniques and algorithms with a strong desire to learn cryptography*
CLR-3 :	*understand the overview of hardware security algorithms in VLSI*
CLR-4 :	*explore the significance of hardware FPGA*
CLR-5 :	*analyse various attacks and counter measures*

Course Outcomes (CO):	***At the end of this course, learners will be able to***	Program Outcomes (PO)		
		1	**2**	**3**
CO-1 :	*understand the detailed mathematical concepts for cryptography.*	*3*	*3*	*1*
CO-2 :	*describe the general structure of Block cipher and steam cipher algorithms.*	*3*	*1*	-
CO-3 :	*analyze performance and hardware Implementation of Hash and RSA*	*3*	*3*	*2*
CO-4 :	*describe variety of state-of-the-art applications such as physically unclonable functions*	*3*	*1*	-
CO-5 :	*explore different types of Trojan and physical attacks.*	*3*	*2*	-

Module-1-Mathematics of Cryptography	***9 Hour***
Basic concepts in number theory and finite fields: Modular arithmetic- Euclidean Algorithm -Extended Euclidean Algorithm-Fermat's and Euler's Theorem-Groups, Rings and Fields-Finite fields of the form-Mapping between Binary and Composite Fields-Prime Number Generation-Pseudo random Sequence Generator- Linear Feedback shift registers.	
Module-2-Modern Cryptography	***9 Hour***
Security goals-Attacks and Services, Block Ciphers, Feistel cipher, Cipher block chaining mode, Cipher feedback mode, DES - AES algorithms and its key generation-RSA algorithm- Elliptic curve -Hash function--MAC-Steam Ciphers using LFSR	
Module-3-Hardware Implementation of Hash Function, RSA	***9 Hour***
Introduction to Cryptographic Hash Functions-The Merkle-Damgard model of hash functions-Construction of Hash Function-Application of Hash function-Hardware Implementation of Hash Functions-MD5-Pipeling-SHA-2 Performance analysis-SHA-3 Keccak Algorithms, RSA Implementation and security - Hardware implementation of 3-bit multiplier, Serial Parallel multiplier.	
Module-4-Security Based on Physical Unclonable Function and FPGA Implementation	***9 Hour***
Classification of PUF- Weak - ICID - SRAM Based PUFs- NOR& NAND circuit-Strong PUF-Features of strong PUF-Arbiter PUF-Analog PUFs-Glitch PUF architecture- Controlled PUF - FPGA synthesis flow-vulnerabilities-Side channel attack-Fault injection attack-FPGA Implementation of PUFs-Arbiter based PUF-Delay Based PUF.	
Module-5-Hardware Trojan and Physical Attacks and its Counter Measures	***9 Hour***

Taxonomy of Hardware Trojans- Classification-Phase of Insertion- Abstraction level of description-Activation mechanism-effects-Location-Hardware Trojan Detection-Introduction-Hardware Trojan detection in IC-Hardware Trojan detection approaches-Trojan Modelling-Combinational Modelling-Sequential Modelling-Design of MOLES Trojan- Side Channel Attacks-Countermeasures.

Learning Resources	1. *Stallings, W. (2020). Cryptography and network security, 8th edition Pearson Education India.* 2. *Katz, J., Menezes, A. J., Van Oorschot, P. C., & Vanstone, S. A. (1996). Handbook of applied cryptography. CRC press.*	3. *Tehranipoor, M., & Wang, C. (Eds.). (2011). Introduction to hardware security and trust. Springer Science & Business Media.* 4. *Mukhopadhyay, D., & Chakraborty, R. S. (2014). Hardware security: design, threats, and safeguards. Chapman and Hall/CRC.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mrs. A. Suganya, Sr. Scientist and Head, Hardware Security Research Group, SETS, Chennai	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. P. Radhika, SRM IST*
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	*2. Dr. M. Valarmathi, SRM IST*
		3. Dr. P. Aruna Priya, SRM IST

Course Code	21ECE536T	Course Name	INTEGRATED NANO-PHOTONICS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of taking this course is to:***
CLR-1:	*outline the fundamentals of Optics and Photonics*
CLR-2:	*understand the effect of nano-size on the optical properties of materials*
CLR-3:	*get familiar with the nanophotonic materials and devices*
CLR-4:	*understand the concept of metamaterial and metasurfaces*
CLR-5:	*explore the application of nano-photonics in various fields.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*define basic principles and concepts of optics and electromagnetic theory.*	3	2	-
CO-2:	*illustrate optical confinement and the effect of device size on its optical properties.*	3	2	-
CO-3:	*utilize the optics and quantum mechanics to understand the concept of nanophotonic.*	3	-	2
CO-4:	*acquire knowledge of metamaterial and metasurfaces.*	3	2	-
CO-5:	*analyse the nanophotonic devices for various applications.*	2	-	3

Module-1 - Introduction to Photonics	***9 Hour***
Basic principles of optics and light propagation, Electromagnetic theory and Maxwell's equations, Wave-particle duality of light, Reflection and refraction, Polarization of light, Interference, and diffraction of light, Coherence, Fresnel equations; Absorption, dispersion, and scattering of electromagnetic waves, diffraction limit – Breaking through the diffraction limit.	
Module-2 – Foundations for Nanophotonics	***9 Hour***
Photons and Electrons: Similarities and Differences, Confinement of photons and electrons, Tunneling, Localization under periodic potential, Nanoscale optical interactions, Nanoscale confinement of electronic interactions, Near-field optics, Modeling near-field nanoscopic interactions, Near-field study of quantum dots, Nano-scale enhancement of optical interactions, Principles of operations of nanophotonic devices using optical near fields.	
Module-3 – Nanophotonic Materials and Devices	***9 Hour***
Quantum Confined Materials: Quantum Wells, Quantum Wires, Quantum Dots, Quantum Rings, Manifestations of Quantum Confinement: Optical Properties, Nonlinear properties, Quantum confined Stark effect, Dielectric confinement effect, Metallic Nanoparticles and Nano-shells, Optical properties of Metallic Nanoparticles, Nanocomposite, Optical properties of Nanocomposites, Photonic Crystals: Basic concepts and features.	

Module-4 – Metamaterial and Metasurfaces	***9 Hour***
Metamaterials concept; Effective medium theories: Maxwell–Garnett theory, Bruggeman theory, Single and Double-Negative metamaterials; Applications: Perfect absorbers; Super lens, Hyperbolic metamaterials and Hyper lens; Tunable photonic metamaterial-based devices; Introduction to metasurfaces; Frequency selective surfaces; Guided mode resonances (GMR); Applications of metasurfaces and GMR based devices; Perfect control over transmission and reflection using metasurfaces	
Module-5 – Applications of Nanophotonic Devices	***9 Hour***
Nano-photonic Devices as Electronic Switches: AND Gate, NOT Gate; Nanocomposite as waveguides, Random Lasers, Quantum confined Lasers; Silicon Photonics: Directional Coupler (DC), Multi-Mode Interferometric Coupler (MMIC). Mach-Zehnder Interferometer (MZI) and Microring Resonator (MRR), Thermo-Optic and Electro-Optic Switches; Reconfigurable Filters and Tunable Delay Lines, Concept of Field Programmable Photonic Gate Array (FPPGA); Biotechnology: Semiconductor quantum Dots for bio-imaging and biosensing.	

Learning Resources	1. *Nanophotonics, Paras. N. Prasad, New Jersey, USA: John Wiley & Sons Inc.,2004.* 2. *Principles of Nanophotonics, Motoichi Ohtsu, Kiyoshi Kobayashi, Tadashi Kawazoe, Takashi Yatsui and Makoto Naruse, New York, USA: CRC Press-Taylor & Francis Group, 2008.* 3. *Fundamentals and Applications of Nanophotonics. by Joseph W. Haus (2016).* 4. *Introduction to Nanophotonics, Sergey V. Gaponenko, Cambridge University Press (2010).*	5. *Optics, A Ghatak, Tata McGraw-Hill (2009).* 6. *Nanophotonics, Hervé Rigneault, Jean-Michel Lourtioz, Claude Delalande, Ariel Levenson, Wiley-ISTE (2006).* 7. *Optical Metamaterials: Fundamentals and Applications, W. Cai and V. Shalaev Springer (2010)*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*15%*	-	*15%*	-	*15%*	-
Level 2	*Understand*	*25%*	-	*20%*	-	*25%*	-
Level 3	*Apply*	*30%*	-	*25%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*25%*	-	*30%*	-
Level 5	*Evaluate*	-	-	*10%*	-	-	-
Level 6	*Create*	-	-	*5%*	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. *Mr. Anuj Kumar, Bombardier Transportation, Ahmedabad, kumaranuj.anii@gmail.com*	1. *Dr. Meenakshi, Professor of ECE, CEG, Anna University, meena68@annauniv.edu*	*1.Dr. Sanjay Kumar Sahu, SRMIST*
2. *Mr. Hariharasudhan - Johnson Controls, Pune, hariharasudhan.v@jci.com*	*2*	*2. Dr. Sayantani Bhattacharya, SRMIST*

Course Code	21ECE537T	Course Name	TESTING OF VLSI CIRCUITS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes/Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1 :	*understand the level in the domain of VLSI Design and Test.*
CLR-2 :	*learn the concept of VLSI Testing for combinational circuits*
CLR-3 :	*gain Knowledge of Test generation for sequential circuits*
CLR-4 :	*introduce Testable memory design and IDDQ Testing*
CLR-5 :	*understand design for testability*

Course Outcomes (CO):	***At the end of this course, learners will be able to***	Program Outcomes (PO)		
		1	**2**	**3**
CO-1 :	*apply the knowledge in the domain of VLSI Design and Test*	*3*	-	*3*
CO-2 :	*develop Test generation for combinational circuit*	*3*	-	*3*
CO-3 :	*understand Test generation for sequential circuit and design testable sequential circuit*	*3*	-	*3*
CO-4 :	*summarize Testable memory design and IDDQ Testing method*	*3*	*2*	*3*
CO-5 :	*introduce the design for testability and the principle of BIST*	*3*	-	*3*

Module-1- Introduction to Testing	***9 Hour***
Introduction to testing, Role of testing in VLSI Design flow, testing at different Levels of abstraction, Types of testing, Fault Error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI Chip, DC and AC parametric tests, Fault modeling, Stuck-at fault, bridging fault, stuck on open fault in CMOS, fault equivalence, fault dominance and fault collapsing. Fault simulation, Types of fault simulation.	
Module-2- Test Generation for Combinational Circuit	***9 Hour***
Test generation basics, Test generation algorithms, path sensitization and example, Boolean difference and example, Significant Combinational ATPG Algorithm, D algorithm and based example, PODEM algorithm, comparing D and PODEM, Testable combinational logic circuit design, Reed –Muller Expansion Technique, Three-Level OR-AND-OR Design, Synthesize of Random Pattern Testable Combinational circuits, Path Delay Fault Testable Combinational Logic design, Testable PLA Design.	
Module-3- Test Generation for Sequential Circuits	***9 Hour***
Testing generation of sequential circuits, Testing of sequential circuits as iterative combinational circuits, state table verification, Test generation based on circuit structure, Design of testable sequential circuits, Controllability and Observability, Ad Hoc design rules for improving Testability, The scan-path Technique for Testable Sequential circuit design, Boundary scan-Motivation, System configuration with boundary scan, Testable sequential circuit design example, Test Sequence generation using State table. ATPG for synchronous circuit	
Module-4- Memory, IDDQ Testing	***9 Hour***
Testable memory design, Memory organization, RAM fault models, test algorithms for RAMs, GALPAT, walking 0s and 1s, March and Checkerboard Test, IDDQ testing-Motivation, Fault Detected by IDDQ test, IDDQ Testing Methods, limitations of IDDQ testing, Delay faults, Delay test Problem, Path Delay Test, Delay Test Methodologies, Practical considerations in Delay Testing, Cache RAM chip testing, Functional ROM Chip testing. Scan Chain Trace Rules- master, slave, shadow, copy, or extra. Built in self-Memory repair - BIRA, BISR, Efuse	

Module-5- Design for Testability	***9 Hour***
Basic principle of of Built-in Self-Test, Test pattern generation of Built-in Self-Test, Logic BIST, XLBIST Exhaustive Testing, Pseudo- Exhaustive pattern Generation, Pseudo-Random Pattern Generation, Deterministic Testing, Output response analysis, Transition count, Syndrome checking, signature analysis, BIST architectures, BILBO, Memory BIST CMOS Testing, testing of static CMOS circuit, Testing of dynamic CMOS circuit, Design for robust testability. *Testing standards-JTAG (IEEE 1149.1), iJTAG (IEEE 1687), IEEE 1500. On-chip Clock Controllers (OCC)*	

Learning Resources	*1.P. K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.* *2.Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test Principles and Architectures", Elsevier, 2017* *3. Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2017.*	*4. I.M.Abramovici,M.A.Breuer and A.D.Friedman,"Digital system and Testable design", Jaico Publishing House 2001* *5. Zainalabe Navabi, "Digital System Test and Testable Design: Using HDL Models and Architectures", Springer, 2010.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1.Dr. Sandeep Patil, CEO, EspinNanotech Solutions, IIT Kanpur	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. V. SARADA, SRMIST*
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	

Course Code	21ECE538T	Course Name	HIGH PERFORMANCE ASIC DESIGN	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*prepare the student to be an entry-level industrial standard ASIC or FPGA designer.*
CLR-2:	*give the student an understanding of basics of System on Chip and Platform based design.*
CLR-3:	*understand the basic FPGA Architecture*
CLR-4:	*analyze the partitioning and placement issues*
CLR-5:	*prepare the student to be an entry-level industrial standard ASIC or FPGA designer.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*be familiar with different FPGA Architecture and their interconnect mechanism*	3	2	-
CO-2:	*understand the significance of Partitioning and placement in ASIC Design*	2	-	3
CO-3:	*be familiar with optimization algorithms in ASIC*	3	-	1
CO-4:	*strong foundation in various routing algorithm*	2	2	-
CO-5:	*detail analysis of clock planning in ASIC*	1	-	2

Module-1- Introduction To ASIC	***9 Hour***
Types of ASICs -VLSI Design flow- Programmable ASICs design types-Antifuse, SRAM- EPROM based ASICs - ASIC Fusing based on EPROM -EEPROM based ASICs -FAMOS description- Programmable ASIC logic cells-ASIC I/O cells -Introduction to CPLD -Types of CPLD.	
Module-2-Programmable ASIC Logic Cells	***9 Hour***
Actel ACT Architecture -Actel Interconnect delay analysis -Xilinx LCA -Architecture -Xilinx EPLD Architecture-Xilinx LCA Interconnect- Xilinx EPLD Interconnect-Altera MAX 5000 - Architecture and interconnect-ASIC Design system: Introduction-Design Systems: Detailed analysis.	
Module-3-Optimization Methods	***9 Hour***
Trade off issues at System Level -Solutions to the issues at system level -Optimization about speed, area and power -Optimization trade-off factor -Asynchronous and low power system design-ASIC physical design issues.	
Module -4 -System Partitioning	***9 Hour***
System partitioning: Objectives -System partitioning Procedure-Objective of System Portioning - Partitioning methods- Measuring Connectivity -Problem on Constructive Partitioning -Constructive Partitioning - Iterative Partitioning Improvement -Problem on Iterative Partitioning Improvement -The Kernighan–Lin Algorithm -The Ratio-Cut Algorithm.	
Module-5-Routing	***9 Hour***
Introduction to Routing-Global and Local Routing- Introduction to Left Edge First Algorithm -bend minimization technique-over the cell (OTC) Routing -Transistor chaining -min-cut placement algorithm with problems- Clocking strategies -1D compaction	

Learning Resources	1. *Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.* 2. *Jose E. France, YannisTsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.* 3. *M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003*	4. *Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.* 5. *Sherwani, N.A., "Algorithm for VLSI Physical Design Automation", 2nd Ed., Kluwer. 1999*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mrs. A. Suganya, Sr. Scientist and Head, Hardware Security Research Group, SETS, Chennai	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. J. Selvakumar, SRMIST*
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	*2. Dr. R. Prithiviraj, SRMIST*

Course Code	21ECE539T	Course Name	QUANTUM COMPUTATION AND ALGORITHMS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*explore quantum computing and its underlying principles in quantum mechanics.*
CLR-2:	*analyze quantum circuits for computational tasks.*
CLR-3:	*utilize the open-source Qiskit platform for quantum programming.*
CLR-4:	*study the grover and deutsch-jozsa quantum algorithms for solving specific problems efficiently.*
CLR-5:	*investigate the practical applications of quantum concepts across various fields.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand fundamental concepts in quantum computing and quantum algorithms.*	3	2	3
CO-2:	*design and analyze quantum circuits for various computational tasks.*	3	2	3
CO-3:	*apply quantum computing principles to machine learning problems.*	3	2	3
CO-4:	*implement and optimize quantum algorithms for efficient problem-solving.*	3	2	3
CO-5:	*interpret variational circuits as machine learning models and apply them effectively.*	3	2	3

Module-1 - Quantum Computing Fundamentals	***9 Hour***
Introduction to Quantum Computing: Need for Quantum Computing and fundamental concepts - Vector spaces, Probability, Complex numbers, and mathematical preliminaries - Postulates of quantum mechanics - Bra-ket notations - Measurements, Composite systems, Quantum States and Entanglement: Bell's state, Entanglement - Bloch sphere, Pure and Mixed states	
Module-2 - Quantum Gates and Circuits	***9 Hour***
Quantum Gates and Superposition: Quantum superposition - Qubits: What is a Qubit? Mathematical Representation - Bloch Sphere and Quantum Gates - Entanglement and Multi-Qubit states - CNOT gate, Quantum Circuits and Complexity: Geometry of quantum states - Quantum gates, Quantum circuits - Quantum circuit design	
Module-3 - Quantum Algorithms	***9 Hour***
Quantum Circuit Analysis: Quantitative measures of circuits - Analysis of the quality of circuits - Circuit optimization. Quantum Algorithms: Introduction to Grover's algorithm - Detailed walkthrough on Grover's algorithm - Grover's search applied to an unstructured database - Quantum Teleportation, Shor's algorithm, Quantum Fourier Transform - Deutsch Algorithm, Deutsch-Jozsa algorithm	
Module-4 - Quantum Computing and Machine Learning	***9 Hour***
Introduction to Quantum Machine Learning - Parameterized quantum circuits (PQC) - Quantum Information Encoding - Training parameterized quantum circuits - Quantum Support Vector classification (QSVM)- Examples of Typical Machine Learning Problems - The Three Ingredients of a Learning Problem – Data -Model – Loss - Risk Minimisation in Supervised Learning - Minimising the Empirical Risk as a Proxy - Quantifying Generalisation – Optimisation - Training in Unsupervised Learning - Methods in Machine Learning - Linear Models - Neural Networks- Graphical Models - Kernel Methods	
Module-5 – Variational Circuits as Machine Learning Models	***9 Hour***
How to Interpret a Quantum Circuit as a Model - Deterministic Quantum Models- Probabilistic Quantum Models - An Example: Variational Quantum Classifier - An Example: Variational Generator- which Functions Do Variational Quantum Models Express? - Quantum Models as Linear Combinations of Periodic Functions - An Example: The Pauli-Rotation Encoding- Training Variational Quantum Models - Gradients of Quantum	

Computations - Parameter-Shift Rules - Barren Plateaus - Generative Training- Quantum Circuits and Neural Networks - Emulating Nonlinear Activations - Variational Circuits as Deep Linear Neural Networks - Time-Evolution Encoding as an Exponential Activation.

Learning Resources	*1.Quantum Computation and Quantum Information. M. A. Nielsen and I. L. Chuang, Cambridge University Press* *2.Quantum Computing ,Vishal Sahni, Tata McGraw-Hill Publishing Company Limited,2007.* *3. Mikio Nakahara and Tetsuo Ohmi,"Quantum Computing", CRC Press, 2008* *4. N. David Mermin,"Quantum Computer Science", Cambridge, 2007* *5. https://qiskit.org/* *6.An Introduction to Quantum Computing. P. Kaye, R. Laflamme, and M. Mosca, Oxford University Press, New York*	*7. Quantum Computer Science. N. David Mermin:, Cambridge University Press* *8. Quantum Cryptography. D. Unruh:, Available online: https://courses.cs.ut.ee/all/MTAT.07.024/2017_fall/uploads/* *9. NIST Post Quantum Cryptography, Available online: https://csrc.nist.gov/projects/post-quantum-cryptography/round-2-submissions* *10. Quantum Algorithms for Cryptographically Significant Boolean Functions - An IBMQ Experience. SAPV Tharrmashastha, D. Bera, A. Maitra and S. Maitra, Springer 2020.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*30%*	-	*30%*	-	*30%*	-
Level 2	*Understand*	*30%*	-	*30%*	-	*30%*	-
Level 3	*Apply*	*20%*	-	*20%*	-	*20%*	-
Level 4	*Analyze*	*10%*	-	*10%*	-	*10%*	-
Level 5	*Evaluate*	*10%*	-	*10%*	-	*10%*	-
Level 6	*Create*	-	-	-	-	-	-
	Total	100 %		100 %		100 %	

Course Designers

Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
1. Mrs. A. Suganya, Sr. Scientist and Head, Hardware Security Research Group, SETS, Chennai	1. *Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. R. Prithiviraj SRMIST*
	2. *Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram*	*2. Dr. Gayathri, SRMIST*

Course Code	21ECE631T	Course Name	MIXED SIGNAL IC DESIGN	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*21ECC533J, 21ECE531T*	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR)	***The purpose of taking this course is to:***
CLR-1	*understand the challenges involved in analog design and the necessity of Mixed Analog-Digital (MAD) chips.*
CLR-2	*explore the design and implementation of nonlinear analog circuits and understand their applications in mixed-signal IC design.*
CLR-3	*learn the principles and characteristics of continuous-time and discrete-time filters and understand their applications in signal processing.*
CLR-4	*explore different DAC and ADC architectures, along with their specifications and trade-offs.*
CLR-5	*comprehend the basic architecture and applications of PLLs in electronic systems.*

Course Outcomes (CO)	***At the end of this course, learners will be able to***	***Program Outcomes (PO)***		
		1	***2***	***3***
CO-1	*identify and articulate the advantages of MAD circuits over traditional analog circuits.*	*0*	*1*	*0*
CO-2	*design and analyze comparators and sample-and-hold circuits based on specific design requirements.*	*1*	*2*	*3*
CO-3	*design and analyze active RC filters, MOSFET-C filters, and Switched-Capacitor (SC) circuits.*	*2*	*2*	*3*
CO-4	*analyze quantization noise and design various DAC and ADC architectures, considering factors such as speed, accuracy, and power consumption.*	*3*	*2*	*3*
CO-5	*design PLL-based electronic oscillators and frequency synthesizers for different applications; integrate BIST structures into PLL designs, enhancing their reliability and testability.*	*3*	*2*	*3*

Module-1: Introduction to Analog and Mixed Signal Design	***3 Hour***
Challenges in analog design, Need for Mixed Analog-Digital (MAD) chips, Mixed-Signal processing blocks, Advantages of MAD circuits on the same chip, Applications of MAD chips, Obstacles in the design of MAD chips, Mixed-signal IC design flow, Mixed-signal layout issues, A MAD chip including a built-in self-test structure.	
Module-2: Nonlinear Analog Components	***12 Hour***
Comparators: Comparator specifications, op-amp comparator, charge-injection errors, latched comparators, CMOS comparators, BiCMOS comparators, Bipolar comparators, Sample-and-Hold (S/H) circuits: S/H basics, MOS S/H circuits, CMOS S/H circuits, BiCMOS S/H circuits, Translinear Circuits: Translinear gain cell, Translinear multiplier	
Module-3I: Integrated Analog Filters	***12 Hour***
Continuous-Time Filters: 1st order and 2nd order filters, Transconductance-C filters, Active RC filters, MOSFET-C filters, Discrete-Time Filters: Basic concepts of discrete-time signals and filters, Switched-Capacitor (SC) circuits - Basic building blocks, basic operation and analysis, 1st order filters, biquad filters, ladder filters, charge injection, SC gain circuits, Amplitude modulator, FWR, peak detector, VCO, sinusoidal oscillator, S/H circuits based on SC circuit	
Module-4: Data Converters	***12 Hour***
Data Converter Fundamentals: Analog vs Discrete-time signals, converting analog signals to digital signals, ideal Digital-to-Analog Converter (DAC), ideal Analog-to-Digital Converter (ADC), Sample-and-Hold (S/H) characteristics, quantization noise, signed codes, DAC specifications, ADC specifications, Mixed-signal layout issues.	

DAC Architectures: Decoder-based DACs, Binary-scaled DACs, Thermometer-code DACs, Hybrid DACs, ADC Architectures: Integrating ADC, Successive-Approximation ADC, Cyclic ADC, Pipelined ADC, Flash ADC, Two-step ADC, Interpolating ADC, Folding ADC, Time-interleaved ADC
Module-5: Phase-Locked Loops (PLL) ***6 Hour***
Basic PLL architecture, Application of PLL as electronic oscillators and frequency synthesizer, Delay-locked loop, PLL with BIST structure

Learning Resources	1. *Tony Chan Carusone, David A. Johns, Kenneth W. Martin, "Analog Integrated Circuit Design", Wiley, 2012.* 2. *Tertulien Ndjountche, "CMOS Analog Integrated Circuits: High-Speed and Power-Efficient Design", CRC Press, 2011.* 3. *Jacob Baker, "CMOS Mixed-Signal circuit design", IEEE Press, 2009.* 4. *Razavi, "Principles of data conversion system design", Wiley IEEE Press, 1st Edition, 1994.* 5. *Franco Maloberti, "Data Converters", Springer, 2007.*	6. *Vineeta P. Gejji, "Analog and Mixed Model VLSI Design", PHI, 2011.* 7. *Willy M. C. Sansen, "Analog Design Essentials", Springer, 2006.* 8. *Arjuna Marzuki, "CMOS Analog and Mixed-Signal Circuit Design", CRC Press, 2020.* 9. *Gregorian, Temes, "Analog MOS Integrated Circuit for signal processing", John Wiley and Sons, 1986.* 10. *Rolf Schaumann, Haiqiao Xiao, Mac E. Van Valkenburg, "Analog Filter Design", Oxford University Press, Second Edition, Re-print, 2013.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit tests (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	30%	-	30%	-	30%	-
Level 4	*Analyze*	30%	-	30%	-	30%	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Sethupathy Balakrishnan, Lead Application Engineer, Cadence Designs Systems	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. A.V.M. Manikandan, SRMIST*
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	*2. Dr. T. Vijayan, SRMIST*

Course Code	21ECE632T	Course Name	RADIO FREQUENCY VLSI	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*20ECC533J*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand the basic architectures of RF systems and its characteristic parameters, Impedance matching techniques.*
CLR-2:	*construct the different types of filters.*
CLR-3:	*utilize the basics of High frequency amplifier design, the operation of Mixers, oscillators, PLL and Frequency synthesizers*
CLR-4:	*identify different types of Power amplifiers*
CLR-5:	*understand Various multiple access techniques and Construct LNA, Frequency synthesizer and power amplifier*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*construct impedance matching networks*	*3*	*3*	*2*
CO-2:	*implement the different types of filters.*	*3*	*3*	*2*
CO-3:	*describe High frequency amplifier design, the operation of Mixers, oscillators, PLL and Frequency synthesizers*	*3*	*3*	*2*
CO-4:	*characterize the different types of Power amplifiers*	*3*	*3*	*2*
CO-5:	*recognize Various multiple access techniques and Create LNA, Frequency synthesizer and power amplifier*	*3*	*3*	*2*

Module-1 - RF Systems	***9 Hour***
Basic architectures, Transmission media and reflections Maximum power transfer, Passive RLC Networks, Parallel RLC tank Circuit, Q factor, Series RLC networks, Problems solving on RLC networks, Interconnects and skin effect, Conditions for Impedance matching, Pi and T matching network, Problems solving on Matching network, Performance parameter of RF design, Gain Parameters, Non-linearity parameters, Noise figure, Phase Noise, Dynamic range, Performance tradeoffs in an RF circuit.	
Module-2 - : Filter Design & High Frequency Amplifier Design	***9 Hour***
Filter performance parameters and its types, Frequency and impedance scaling, Modern filter design, Derivation of normalized parameters, Low Pass, High Pass, Band Pass and Band Reject Filter Design, Microstrip based filter design, Effects of finite Q, High frequency Amplifier design, Shunt-series Amplifier, Bandwidth enhancement techniques, tuned amplifiers, Neutralization, Unilateralization, cascaded Amplifiers, Problems solving on RF amplifier design.	
Module-3 – Mixers and Oscillators	***9 Hour***
Introduction to RF active devices, Mixer fundamentals, Nonlinear systems as Linear mixers, Multiplier based mixers, Subsampling mixers, Oscillators - Problems with purely linear oscillators, Resonators, Tuned oscillator- Hartley, Colpitt, Clapp oscillator, Negative Resistance oscillators, Voltage controlled oscillators, Phase locked loops : Linearized PLL models, Phase detectors, Charge pumps, Loop filters, PLL design, Frequency synthesizer: Block diagram description, Integer-N synthesis, Fractional-N frequency synthesis, Applications of Frequency Synthesis ,Problem Solving on Oscillator and PLL.	
Module-4 - RF Power Amplifiers	***9 Hour***
General considerations and its performance metrics, Types of Power amplifiers, Class A, B, AB, C, D, E, F & Efficiency Derivation, Linearization Techniques and methods, Envelope feedback, Feed forward, Pre-Post distortion, Envelope elimination and restoration, Efficiency Boosting Techniques, Methods of Efficiency boosting, Adaptive bias, Doherty amplifier, RF Power amplifier design examples.	
Module-5 – Multiple Access Techniques & Case Studies	***9 Hour***

Introduction, Various multiple access Techniques, Wireless standards, Mobile RF communication, FDMA, TDMA, CDMA, Transceiver Architectures: General considerations, Receiver architecture, Transmitter Architecture, OOK Transceiver, Transceiver performance tests, Transceiver Design examples, CASE STUDIES: LNA Design, Mixer Design, Frequency Synthesizer, Power Amplifier.

Learning Resources	1. *Aleksandar Tasic, Wouter.A.Serdijn, John.R.Long, "Adaptive Low Power Circuits for Wireless Communication (Analog Circuits and Signal Processing)", Springer, 2nd Edition, 2010.* 2. *Chris Bowick, "RF Circuit design", Newnes (An imprint of Elsevier Science), 2nd Edition, 2007.* 3. *B.Razavi ,"RF Microelectronics" , Prentice-Hall ,2nd Edition, 2020.* 4. *Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2nd Edition, 2011.*	5. *Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 2nd Edition,2017.* 6. *Jia-sheng Hong, "Microstrip filters for RF/Microwave applications", Wiley, 2nd Edition, 2011.* 7. *Thomas.H. Lee, "The design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd Edition, 2004.*

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Final Examination (40% weightage)	
		Formative CLA-1 Average of unit test (50%)		Life-Long Learning CLA-2 (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100%*		*100%*		*100%*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Mrs. A. Suganya, Sr. Scientist and Head, Hardware Security Research Group, SETS, Chennai*	1. *Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	1. *Dr. J. Manjula, SRMIST*
	2. *Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram*	2. *Dr. D. Tharani, SRMSIT*

Course Code	21ECE633T	Course Name	MACHINE LEARNING IN VLSI	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*provide concise introduction to the fundamental concepts of machine learning*
CLR-2:	*introduce neural networks and its algorithm*
CLR-3:	*focus on the backend design challenges, including mask synthesis and physical verification*
CLR-4:	*study how machine learning can help in physical design*
CLR-5:	*address the energy efficient design of machine learning hardware*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand the basic definitions and concepts of machine learning*	3	2	-
CO-2:	*explore the applications of neural network algorithms*	3	2	-
CO-3:	*apply the machine learning in physical verification and mask synthesis*	-	2	3
CO-4:	*predict the machine learning model for physical design such as placement and routing*	-	2	3
CO-5:	*analyze the energy efficient machine learning hardware structures.*	-	2	3

Module-1 - Introduction to Machine Learning	***9 Hour***
Introduction, Types of Learning, Supervised learning: Classification and Regression, Unsupervised Learning: Clustering, Density Estimation, Reinforcement learning, Linear Regression, Types of Regression Models, Tutorial on regression, Decision Tree, Example for Decision Tree, Overfitting, Pruning, Principal components, Bayesian Learning, Bayesian Network	
Module-2 - Neural Network, Computational Learning Theory and Clustering	***9 Hour***
Neural Network Introduction, Perceptrons, Multilayer Neural Network, Back Propagation Algorithm, Deep Neural Networks, Training of neural networks, Introduction to computational learning theory, Sample Complexity, Finite hypothesis space, Infinite hypothesis space, Ensemble Learning, Bootstrap Method, Bootstrap Aggregation, Adaptive Boosting (AdaBoost) Algorithms, Gradient Boosting Algorithms, Clustering, Hierarchical, Model Based and Density Based Clustering, K-means Clustering	
Module-3 - Machine Learning in Physical Verification and Mask Synthesis	***9 Hour***
Machine learning taxonomy, VLSI CAD Abstraction levels, Machine Learning for Compact Lithographic Process: Introduction, Lithographic Patterning Process, Representation of Lithographic Patterning Process – Mask, Imaging, Resist & Etch Transfer Function, Machine Learning for Mask Synthesis: Machine Learning guided OPC, MLP Construction, ML-EPC, EPC Algorithm, CPM Task, CPM Training Experience, Performance metrics, Supervised learning of a CPM.	
Module-4 - Machine Learning Applications in IC Physical Design	***9 Hour***
Machine Learning for Manufacturing: Gaussian Process-Based Regression Models, and Routability-Driven Placement, Lithography Friendly Routing, Gaussian Process-Based Wafer-Level Correlation Modeling, Wafer-Level Statistical Correlations, Spatial Correlation Modeling of E-Test Measurement, Probe-Test Specification Measurements, Machine Learning Approaches for IC Manufacturing, Manufacturing Process, Evaluation Metric: Confusion Matrix, ROC Curves	

Module-5 – Energy Efficient Design of Advanced Machine Learning Hardware	***9 Hour***
Artificial Intelligence and Machine Learning, Neural Networks, Resource Requirements of State-of-the-Art Neural Networks, Software and Co-design Optimizations, Pruning, Weight Sharing, Compact Network Architectures, Hardware–Software Co-design, Hardware-Level Techniques, Deep CNN Accelerators, Memory-Efficient Architectures, Leveraging Sparsity in Neural Networks, Error Resilience Analysis, Efficient Machine Learning Architectures.	

Learning Resources	*1. Lorenzo Rosasco, (2017), Introductory Machine Learning Notes.* *2. Ethem Alpaydin, Introduction to Machine Learning, Second Edition.*	*3. Ibrahim (Abe) M. Elfadel, Duane S. Boning and Xin Li (2019), Machine Learning in VLSI Computer Aided Design*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. *Mrs. A. Suganya, Sr. Scientist and Head, Hardware Security Research Group, SETS, Chennai*	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. A. Manikandan, SRMIST*
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	

Course Code	21ECE634T	Course Name	FUNDAMENTALS OF SOLAR CELL	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*know the fundamentals of semiconductor materials for solar cells.*
CLR-2:	*understand the basics of solar cell design and parameters*
CLR-3:	*introduce the technologies for solar cell production with silicon material*
CLR-4:	*apply the solar cell technologies foe wafer-based silicon*
CLR-5:	*implement the silicon technologies for photovoltaic systems*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*define the principles and arrangements of silicon atoms and p-n junction under illumination*	3	2	-
CO-2:	*acquire knowledge on solar cell parameters for efficient design*	3	-	3
CO-3:	*analyse the growth process of metallurgical and electronic grade silicon*	3	2	-
CO-4:	*express the knowledge of solar cell technology for development of commercial solar cell*	3	-	2
CO-5:	*investigate the design and application of photovoltaic systems*	3	2	-

Module-1 - Fundamentals of Semiconductors	***9 Hour***
Semiconductor as solar cell materials; arrangement of atoms in space: types of unit cells and lattices in solar cell; P-N junction diode, equilibrium conditions: carrier movement, current densities and carrier concentration profiles; P-N junction in non-equilibrium: I-V relation quantitative analysis; P-N junction under illumination: solar cell: generation of photovoltaics, light generated current, I-V equation of solar cell, solar cell characteristics.	
Module-2 - Design of Solar Cell	***9 Hour***
Upper limits of cell parameters: short circuit current, open circuit voltage, Fill Factor, Efficiency; Losses in solar cell: model of a solar cell, effect of series and shunt resistance on efficiency, effect of solar radiation in efficiency, effect of temperature in efficiency; sola cell designs; Design of high Isc: requirement of high Isc, choice of junction depth and its orientation, minimization of optical losses, minimization of recombination; Analytical Techniques: solar simulators, I-V measurement, quantum efficiency measurement	
Module-3 - Solar Cell Technologies: Production of Si	***9 Hour***
Growth of solar PV industry and Si requirements; steps in producing Si wafers, production of metallurgical grade Si (MGS), production of electronic grade Si (EGS): high purity Si containing gases, obtaining solid poly-Si; production of Si wafers: monocrystalline Si ingots- CZ and FZ process; refining process for solar grade Si, possible route for conversion of MG-Si to SoG-Si, SI usage in solar PV	
Module-4 - Si Wafer-Based Solar Cell Technology	***9 Hour***
Development of commercial solar cell: improvement from use of CZ single crystal, diffused junction and anti-reflective coating; multi-crystalline Si and first terrestrial PV modules; process flow of commercial Si cell technology; processes used in solar cell technology: saw damage removal and surface texturing, P-N Junction formation – diffusion process, thin film layer for ARC and surface passivation, metal contacts- pattern defining and deposition; High efficiency solar cell: passivated emitter solar cell, buried contact and rear point contact solar cell, passivated emitter and rear contact.	
Module-5 – Photovoltaics System Design and Applications	***9 Hour***
Introduction to solar PV systems; Stand-alone PV system configurations: type-A, type-B, type-C and type-D regulated stand-alone system with DC load, Design methodology of PV systems: design of PV-powered DC fan without battery (type-A configuration), regulated stand-alone system with DC load using MPPT (type-B configuration), design of PV powered DC pump, design of stand-alone systems with battery and AC or DC load; hybrid PV systems; Grid connected PV system; Simple payback period.	

Learning Resources	1. *Chetan Singh Solanki, Solar Photovoltaic Technology and Systems: A Manual for Technicians, Trainers and Engineers, 320 pages, 2013, Prentice Hall India Learning Private Limited.* 2. *G. N. Tiwari, Arvind Tiwari, Shyam, Handbook of Solar Energy: Theory, Analysis and Applications, 1st edition, 764 pages, 2016, Springer.*	3. *S. P. Sukhatme, SOLAR ENERGY, 4rth edition, 568 pages, 2017, McGraw hill education.* 4. *Hans S. Rauschenbach, Solar Cell Array Design Handbook: The Principles and Technology of Photovoltaic Energy Conversion, 560 pages, 1980, Springer.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mr. Abhijeet Pathak, Western Digital, Bangalore, India.	*1. Prof. G. P. S. C. Mishra, NIT Raipur*	*1. Dr Soumyaranjan Routray, SRMIST*
	2. Dr. K.P. Pradhan, IIITDM, Kanchipuram	*2. Dr Rajesh Agarwal, SRMSIT*

Course Code	21ECE635T	Course Name	OPTIMIZATION TECHNIQUES IN NANOELECTRONICS	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*know the fundamentals of materials for nanoelectronics.*
CLR-2:	*understand the basics of growth, fabrication, and measurement techniques for nanostructures*
CLR-3:	*introduce the concepts of electron transport in semiconductors and nanostructures*
CLR-4:	*apply the electron properties of in traditional low-dimensional structure*
CLR-5:	*implement the concepts of different nanostructured devices*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*know the fundamentals of materials for nanoelectronics.*	*3*	*3*	-
CO-2:	*understand the basics of growth, fabrication, and measurement techniques for nanostructures*	*3*	*3*	-
CO-3:	*introduce the concepts of electron transport in semiconductors and nanostructures*	*3*	*3*	-
CO-4:	*apply the electron properties of in traditional low-dimensional structure*	*3*	-	*2*
CO-5:	*implement the concepts of different nanostructured devices*	*3*	*3*	-

Module-1: Materials for Nanoelectronics	***9 Hour***
Introduction, Semiconductors, Crystal lattices: bonding in crystals: Ionic crystals, Covalent crystals, Electron energy bands, Symmetry of crystals and properties of electron spectra, Direct-bandgap and indirect-bandgap semiconductors, Band structures of semiconductor alloys, Semiconductor heterostructures, Band offsets at heterojunctions, Graded semiconductors, Strained pseudomorphic heterostructures ,Lattice-matched heterostructures, Lattice-matched and pseudomorphic heterostructures, Organic semiconductors, Carbon nanomaterials: nanotubes and fullerenes.	
Module-2: Optimization of Growth, Fabrication, and Measurement Techniques for Nanostructures	***9 Hour***
Introduction, Bulk crystal and heterostructure growth: Single-crystal growth, Epitaxial growth, Molecular-beam epitaxy, Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices, Techniques for characterization of nanostructures, Spontaneous formation and ordering of nanostructures, Clusters and nanocrystals, Methods of nanotube growth, Chemical and biological methods for nanoscale fabrication, Fabrication of nano-electromechanical systems	
Module 3: Optimization the Electron Transport in Semiconductors and Nanostructures	***9 Hour***
Introduction, Time and length scales of the electrons in solids: Electron fundamental lengths in solids , Size of a device and electron spectrum quantization, Quantum and classical regimes of electron transport, Statistics of the electrons in solids and nanostructures: Classical statistics, Fermi statistics for electrons , ,The density of states of electrons in nanostructures, Electron transport in nanostructures: Classical dissipative transport, Dissipative transport in short structures, Hot electrons, Transient overshoot effects, Classical ballistic transport, Quantum ballistic transport: the Landauer formula.	
Module-4: Electrons in Traditional Low-Dimensional Structure	***9 Hour***
Introduction, Electrons in quantum wells: Single modulation-doped heterojunctions, Basic equations describing the physics of the electrons at an interface, Numerical analysis of a single heterojunction, Control of charge transfer, Electrons in quantum wires: Electron transport in quantum wires, Electrons in quantum dots: zero-dimensional system, macro atom, tunnelling of electrons through quantum levels.	
Module-5: Device Optimizations and Applications	***9 Hour***
Geometry and Dimension, Surface Modification, Integration, Resonant-tunneling diodes: The physics underlying the resonant-tunneling effect, Quantitative characteristics of the resonant-tunneling effect, Sequential tunnelling, Negative differential resistance under resonant tunneling, A resonant-tunneling diode as a microwave oscillator, Field-effect transistors, Single-electron-transfer devices, Potential-effect transistors , Light-emitting diodes and lasers , solar cells, Computational Models: finite element analysis, density functional theory.	

Learning Resources	1. *Vladimir V Mitin, Viatcheslav A. Kochelap, and Michael A. Stroscio. "Introduction to nanoelectronics: science, nanotechnology, engineering, and applications", Cambridge University Press, 2008.* 2. *Khurshed Ahmad Shah, Farooq Ahmad Khanday "Nanoscale Electronic Devices and Their Applications", CRC Press, 2021.* 3. *Rainer Waser (Ed.), "Nanoelectronics and Information Technology", Wiley-VCH, Third, Completely Revised and Enlarged Edition, 2012.*	4. *George W. Hanson, "Fundamentals of Nanoelectronics", Prentice Hall, 20073.Karl Goser, Peter GlÖsekötter,JanDienstuhl, "Nanoelectronics and Nanosystems", Springer, 2004* 5. *Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications", Cambridge University Press, 2012* 6. *Sulabha K. Kulkarni "Nanotechnology: Principles and Practices", Third Edition, Springer, 2015.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1.Mr. Abhijeet Pathak, Western Digital, Bangalore, India	*1. Prof. G. P. S. C. Mishra, NIT Raipur*	*1. Dr. Arijit Bardhan Roy SRMIST*
	2. Dr. K.P. Pradhan, IIITDM, Kanchipuram	*2. Dr. Rajesh Agarwal, SRMIST*

Course Code	21ECE636T	Course Name	ELECTRONICS PACKAGING, ASSEMBLY AND TESTING	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*identify electrical issues encountered and corrective actions taken during packaging*
CLR-2:	*study of single chip and multi- chip IC packaging*
CLR-3:	*analyze different types of electronic packaging, materials used and their properties*
CLR-4:	*identify the challenges faced at different levels of packaging and their solutions.*
CLR-5:	*design PCB using CAD tools and study of board assembly techniques*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand different electrical issues in packaging*	3	3	2
CO-2:	*design of chip level packaging*	3	2	-
CO-3:	*explore different electronic packaging types*	3	2	-
CO-4:	*analyze the challenges faced in packaging*	3	2	3
CO-5:	*design of PCB and understand board assembly techniques*	3	-	2

Module-1– Electrical Issues of Packaging	***9 Hour***
Signal Distribution, Power distribution, Electromagnetic Interference, Electrical Package design: Capacitance, Resistance and Inductance Interconnect, Transmission Lines, Clock Distribution, Noise Sources, Digital and RF Issues, Processing Technologies, Thin Film deposition, Patterning, Metal to Metal joining.	
Module -2 – IC Packaging	***9 Hour***
Introduction, Packaging Technologies: Single chip packaging: functions, types, materials processes, properties, characteristics, Multi chip packaging: types, design, comparison, Chip and Wire assembly: Die/Wire Assembly, Flip Chip Assembly, Wafer level Packaging, wafer level burn – in and test.	
Module 3- Advanced Packaging	***9 Hour***
Functions of an Electronic Packaging – Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends: Challenges, Materials for Microelectronic packaging: Material Properties, Ceramics, Polymers, Metals, Material for high density interconnect substrates.	
Module -4 – Packaging Challenges	***9 Hour***
Basic concepts, Thermal mismatch and fatigue – failures – thermo mechanically induced – electrically induced – chemically induced. Thermal Management: Heat transfer fundamentals, Solution- Device level, Package level, convection- heat sink, Electric field control, Enhanced cooling. *Practice: Developing a package for thermal management using COMSOL*	
Module -5 – Board Assembly and Testing	***9 Hour***

PCB design- components, standard fabrication, CAD tools for PCB design, Types of Boards. Board assembly- Surface mount technology, Through Hole technology, Process control and design consideration, Rules for Component Placement in PCB, Rules for Power supply and Ground, Connections layout. *Practice: PCB Layout Design of single digit pulse counter using PCB design tool*

Learning Resources	1. *Tummala, Rao R., Fundamentals of Microsystems Packaging, McGraw Hill, 2001* 2. *Howard Johnson, Martin Graham, High Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993* 3. *John H. lau, Semiconductor Advanced Packaging, Springer, 2021. doi.org/10.1007/978-981-16-1376-0.*	*4. Qin et.al. "Thermal management and packaging of wide and ultra-wide bandgap power devices: a review and perspective" 2023 J. Phys. D: Appl. Phys. 56 093001. 10.1088/1361-6463/acb4ff.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*15%*	*-*	*15%*	*-*	*15%*	*-*
Level 2	*Understand*	*25%*	*-*	*20%*	*-*	*25%*	*-*
Level 3	*Apply*	*30%*	*-*	*25%*	*-*	*30%*	*-*
Level 4	*Analyze*	*30%*	*-*	*25%*	*-*	*30%*	*-*
Level 5	*Evaluate*	*-*	*-*	*10%*	*-*	*-*	*-*
Level 6	*Create*	*-*	*-*	*5%*	*-*	*-*	*-*
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Dr. Sandeep Patil, CEO, EspinNanotech Solutions, IIT Kanpur	*1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University*	*1. Dr. Tulika Srivastava, SRMIST*
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	*2. Dr. P. Eswaran, SRMIST*

Course Code	21ECE637T	Course Name	QUANTUM CRYPTOGRAPHY	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*develop a solid understanding of encryption fundamentals, block ciphers like DES and AES, and key distribution mechanisms.*
CLR-2:	*master public key cryptosystems including RSA, hash functions, MAC algorithms, and digital signatures for data integrity and authentication.*
CLR-3:	*delve into quantum key distribution with protocols like BB84 and Ekert91 and understand strategies for countering eavesdropping in quantum communication.*
CLR-4:	*examine quantum computing's impact on cryptography, explore post-quantum techniques, and discuss their role in quantum-safe communication.*
CLR-5:	*explore on the mathematical based quantum cryptography.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*gain a comprehensive understanding of encryption basics, block ciphers, and key distribution for secure communication.*	*3*	*2*	*3*
CO-2:	*master RSA encryption, hashing, MAC algorithms, and digital signatures for data integrity and authentication.*	*3*	*2*	*3*
CO-3:	*apply quantum key distribution protocols, ensuring privacy and countering eavesdropping in quantum communication.*	*3*	*2*	*3*
CO-4:	*explore quantum computing's impact on cryptography.*	*3*	*2*	*3*
CO-5:	*implement techniques for quantum-safe communication and data protection.*	*3*	*2*	*3*

Module-1 - Foundations of Cryptography	***9 Hour***
Introduction to Encryption and Block Ciphers - Overview of encryption fundamentals - Introduction to block ciphers - Data Encryption Standard (DES) and its overview - Advanced Encryption Standard (AES) and its significance - Block cipher modes of operation- Public Key Encryption and Key Exchange - Principles of public key cryptosystems - RSA algorithm and its significance - Diffie-Hellman Key Exchange protocol	
Module-2 - Cryptographic Protocols and Security Mechanisms	***9 Hour***
Hashing and Message *Authentication Codes (MAC) - Introduction to hashing algorithms - Message Authentication Codes (MAC) - Digital signatures and their importance- Authentication Protocols and System Security - Overview of authentication protocols - Secure email protocols: PGP and S/MIME - Introduction to IP Security (IPsec) - Web security protocols: SSL/TLS - Intrusion detection and prevention systems*	
Module-3 - Quantum Key Distribution Protocols	***9 Hour***
Quantum Key Distribution - Significance of random keys - BB84 protocol: Assumptions, Protocol, Relaxing assumptions - Error correction and privacy amplification - Eavesdropping strategies - Entanglement-based QKD: BBM92 protocol, Ekert91 protocol.	
Module-4 – Modern Cryptography	***9 Hour***
Overview of contemporary cryptographic techniques - Quantum Computing Impact - Discussion on the potential threat of quantum computers – Code based cryptography - The security of computing syndromes as one-way function - Codes and structures	
Module-5 – Post Quantum Cryptography	***9 Hour***
Multivariant – Examples of Multivariate PKCs - Lattice based cryptography - Finding Short Vectors in Random q-ary Lattices - Hash Functions - Public Key Encryption Schemes - Use Cases in Quantum Cryptography – Quantum safe cryptography – Quantum random number generation – Quantum secure direct communication.	

Learning Resources	1. William Stallings, Cryptography and Network Security, 6th Edition, Pearson Education, March 2013. 2. Quantum Cryptography. D. Unruh:, Available online: https://courses.cs.ut.ee/all/MTAT.07.024/2017_fall/uploads/	3. NIST Post Quantum Cryptography, Available online: https://csrc.nist.gov/projects/post-quantum-cryptography/round-2-submissions 4. Quantum Algorithms for Cryptographically Significant Boolean Functions - An IBMQ Experience. SAPV Tharrmashastha, D. Bera, A. Maitra and S. Maitra, Springer 2020.

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (CLA)				Summative Final Examination (40% weightage)	
		Formative CLA-1 Average of unit test (50%)		Life-Long Learning CLA-2 (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	30%	-	30%	-	30%	-
Level 2	Understand	30%	-	30%	-	30%	-
Level 3	Apply	20%	-	20%	-	20%	-
Level 4	Analyze	10%	-	10%	-	10%	-
Level 5	Evaluate	10%	-	10%	-	10%	-
Level 6	Create	-	-	-	-	-	-
	Total	100 %		100 %		100 %	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Mrs. A. Suganya, Sr. Scientist and Head, Hardware Security Research Group, SETS, Chennai	1. Prof Meenakshi M, Dept of Electronics and Communication Engineering, College of Engineering Guindy, Anna University	1. Dr. R. Prithiviraj, SRMIST
	2. Prof. Binsu J Kailath, Dept of Electronics Engineering, IIITDM, Kancheepuram	2. Dr. Gayathri, SRMIST

Course Code	21ECE638T	Course Name	RELIABILITY ENGINEERING OF IC TECHNOLOGY	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							3	0	0	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Electronics and Communication Engineering*	**Data Book / Codes / Standards**		*Nil*	

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand the concept of Reliability technology of IC*
CLR-2:	*illustrate the degradation mechanism in Semiconductor Devices*
CLR-3:	*apply the mathematics of failure analysis models*
CLR-4:	*analyze the components reliability*
CLR-5:	*improve reliability by applying different techniques.*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand the theory of Reliability Engineering for IC*	*3*	*3*	-
CO-2:	*discuss the Reliability issues of Electronics Devices*	*3*	-	*3*
CO-3:	*design the Mathematical model for Failure Analysis*	*3*	*3*	-
CO-4:	*apply life testing for reliability test.*	*3*	-	*2*
CO-5:	*design the techniques for characterization and improvement of reliability of IC*	*3*	*3*	-

Module-1 - Introduction to Reliability Engineering	***9 Hour***
Reliability Engineering, Probabilistic Reliability, Repairable and Non-Repairable Items, Pattern of Failures, Evolution of IC technology, current IC device and packaging, Front-End IC Fabrication Operations, Evolution of IC reliability issues and their associated solutions, Failure Physics, Semiconductor Device Degradation and Failure, Bathtub Curve	
Module-2 – Reliability of Electronics Devices	***9 Hour***
Physics of failure – based models for: Mass transport-induced failures, MOSFET Instabilities and Malfunction, Reliability Problems in Memories, Electronic charge-induced failures (Dielectric breakdown, Hot carrier effects, Electrical over-stress and Electrostatic discharge), Environmental damage (moisture ingress, corrosion, radiation damage), Degradation of interconnects (solder creep and fatigue), defects in semiconductor, Processing defects, Yield: Definition and Scope	
Module-3 - Introduction to Quality Engineering	***9 Hour***
Introduction, definition of quality, basic concept of quality, statistics, definition of SQC, benefits and limitation of statistically quality control (SQC), Quality assurance, Quality cost-Variation in process- factors – process capability – process capability studies and simple problems – Theory of control chart- uses of control chart – Control chart for variables $\bar{X}$ chart, R chart and σ(S) chart	
Module-4 - IC Reliability Methodology	***9 Hour***
Component Reliability, Physical Significance of Physical Distribution functions, Lot by lot sampling – types – probability of acceptance in single, double, multiple sampling techniques – O.C. (Operating Characteristics) curves – producer's Risk and consumer's Risk. AQL (acceptable quality level), LTPD (lot tolerance percent defective), AOQL (Average out going quality limit) concepts-standard sampling plans for AQL (acceptable quality level) and LTPD- uses of standard sampling plans	
Module-5 – Failure Mechanisms and Failure Analysis of IC	***9 Hour***
Dominant failure mechanisms in IC today, Failure analysis of IC, Burn In as reliability Test: Infant mortality, Burn in Procedure, Static and Dynamic Burn In, accelerated life testing (ALT) and *highly accelerated life testing* (HALT), *Technology scaling and Burn In, Non-destructive methods: Optical, X-ray, Acoustic microscope, Electrical characterization, thermal microscope, electron microscope, Raman microscope, FTIR, Destructive methods: decapsulation, SEM and EDX, SIMS, Raman and FTIR, XPS, FIB*	

Learning Resources	1. *Montgomery, Douglas C. "Introduction to Statistical Quality Control", Hoboken, NJ: Wiley, 7th edition, 2013* 2. *Milton Ohring and Lucian Kasprzak. Reliability and failure of electronic materials and devices. 2nd Edition, Academic Press, 2014.*	3. *Patrick D. T. O'connor, and Andre Kleyner. Practical reliability engineering, 5th Edition, John Wiley & Sons, 2012.* 4. *Monohar Mahajan, "Statistical Quality Control", Dhanpat Rai & Sons, 2001.*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (50%)		*Life-Long Learning CLA-2 (10%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*20%*	-	*20%*	-	*20%*	-
Level 2	*Understand*	*20%*	-	*20%*	-	*20%*	-
Level 3	*Apply*	*30%*	-	*30%*	-	*30%*	-
Level 4	*Analyze*	*30%*	-	*30%*	-	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers

Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Dr. Sandeep Patil EspinNanotech Solutions, IIT Kanpur	*1. Dr. Cher Ming Tan, Chang Gung University, Taiwan*	1. *Dr Soumyaranjan Routray, SRMIST,*
		2. *Dr Rajesh Agarwal, SRMSIT*

Course Code	21NTE510J	Course Name	SEMICONDUCTOR MANUFACTURING TECHNIQUES	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							2	0	2	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Physics and Nanotechnology*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand the basics unit processes*
CLR-2:	*grasp the differences/limitations of different process techniques*
CLR-3:	*study the process mechanisms involved*
CLR-4:	*study the process Integration techniques and requires processes involved in final IC*
CLR-5:	*understand the importance of printed electronics*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*understand the selection of silicon wafers and growth techniques*	*3*	*3*	*2*
CO-2:	*apply suitable patterning for different device structures*	*3*	*3*	*3*
CO-3:	*apply the deposition and implantation techniques for device making*	*3*	*3*	*2*
CO-4:	*understand the process integration of a CMOS Technology*	*3*	*3*	*3*
CO-5	*apply printed process for device applications*	*2*	*3*	*2*

Module-1 - Production of Silicon, Epitaxy and Oxidation	***12 Hour***
Classification of grades of silicon, Production of electronic grade silicon, Czochralski growth technique, float zone growth technique, Silicon wafer shaping, Wafer manufacturing steps and inspection, Overview of types of epitaxy, Definition-epitaxy, Comparison of vapour phase epitaxy (VPE),liquid phase epitaxy (LPE) and molecular beam epitaxy (MBE), Working of MBE process, General epitaxy growth mechanism, Epitaxy growth kinetics and examples, Understanding silicon oxide properties, Thermal oxidation, Silicon oxide growth kinetics, Thin oxide growth *Practice: Wafer cleaning processes, Silicon Oxidation Process*	
Module-2 - Lithography and Etching Tools	***12 Hour***
Need and basics of lithography, Optical lithography, Optical lithography controls and mask making, Working concept and controls of e-beam lithography, Resolution of electron beam lithography, X-ray lithography, , Stamp based lithography, Nanoimprint lithography and applications, Etching of silicon, Types- wet and dry etching, Ways of plasma generation for etching processes, Sputter etching, Capacitively coupled plasma, Inductively coupled plasma, Classification of plasma using its density, High density plasma, Reactive ion etching, Deep reactive ion etching and bosh process *Practice: Patterning by photolithography process, Wet chemical etching of silicon dioxide and metal films*	
Module-3 - Deposition Techniques and Ion Implantation Process	***12 Hour***
Classification of material deposition techniques, Overview of physical and chemical deposition technique, Resistive heating evaporation, Electron beam heating evaporation, Pulsed laser evaporation, , Basics of sputtering, DC and magnetron sources for sputtering, Introduction to atomic layer deposition, Working principle of atomic layer deposition, Concepts of diffusion, Using Fick's diffusion in semiconductor doping, , Process of ion implantation, Ion implantation tool, Fundamentals of ion energy loss and stopping, Damage due to implantation, Ion distribution, junction control Carrier recovery using annealing process, *Practice: Deposition Al thin film on the oxidized silicon surface by thermal evaporation and e-beam evaporation, Ion beam implantation process and defect analysis using SRIM software*	

Module-4 - Isolation, Planarization and Process Integration	***12 Hour***
Requirements of device isolation, Types of isolation, Local Oxidation of Silicon (LOCOS) and shallow trench isolation (STI) processes for local isolation, Concept of self-alignment, MOS fabrication with self-alignment, Requirement of planarization, Local and global planarization using chemical-mechanical polishing, Concept of well formation with p and n doping, Fabrication process of CMOS inverter-Process Integration, Packaging of Integrated Circuits *Practice: Local anodic oxidation pattern by scanning probe microscopy, MOS capacitor (Study of CV, I-V characteristics)*	
Module-5 – Printed Electronics Technology	***12 Hour***
Overview of printing processes,, Advantages of printing, Requirements of printing, Printing tools, Types of fluids for ink, Properties of fluids in printing processes, , Working principle of flexographic printing (FP), Advantages and disadvantages of FP, Working principle of gravure printing (GP), Advantages and disadvantages of GP, Working principle of screen printing (SP), Advantages and disadvantages of SP, Working principle of inkjet printing (IP), Advantages and disadvantages of IP Examples of printed devices Comparison of printed devices with lithographically fabricated devices Concept of hybrid printed electronics, Future of printed low-cost electronics, *Practice: Screen printing process and analysis (Optical and Electrical)*	

Learning Resources	1. *Hans H. Gatzen, Volker Saile, Jürg Leuthold, "Micro and Nano Fabrication", Springer 2015* 2. *S. M. Sze, and S. Lee, "Semiconductor Devices Physics and Technology", Wiley, 2012*	3. *Giovanni Nisato, Donald Lupo, Simone Ganz, "Organic and Printed Electronics", CRC Press, 2016.* 4. *Sorab K. Gandhi, "VLSI Fabrication and Principles", McGraw Hill, 2005* 5. *Ulrich Hilleringmann, "Silicon Semiconductor Technology" © Springer Fachmedien Wiesbaden GmbH, 2023*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life Long Learning CLA-2 Practice (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*15%*	*-*		*15%*	*15%*	*-*
Level 2	*Understand*	*25%*	*-*		*25%*	*25%*	*-*
Level 3	*Apply*	*30%*	*-*		*30%*	*30%*	*-*
Level 4	*Analyze*	*30%*	*-*		*30%*	*30%*	*-*
Level 5	*Evaluate*	*-*	*-*	*-*	*-*	*-*	*-*
Level 6	*Create*	*-*	*-*	*-*	*-*	*-*	*-*
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Dr. Saravanan Somasundaram, EMMVEE Group, Bangalore mailto: shrisharavanan@yahoo.co.uk	*1. Prof. S. Balakumar, University of Madras, balakumar@unom.ac.in*	*1. Dr. A. Karthigeyan, SRMIST*
2. Dr. Shanmugasundaram Sakthivel, ARCI, Hyderabad, mailto:ssakthivel@arci.res.in	*2. Prof. V Subramanian, IIT Madras, manianvs@iitm.ac.in*	*2. Dr. Elangovan Elamurugu, SRMIST*

Course Code	21NTE511J	Course Name	CHARACTERIZATION OF SEMICONDUCTOR MATERIALS AND DEVICES	Course Category	E	PROFESSIONAL ELECTIVE	L	T	P	C
							2	0	2	3

Pre-requisite Courses	*Nil*	Co- requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Physics and Nanotechnology*	**Data Book / Codes / Standards**	*Nil*		

Course Learning Rationale (CLR):	***The purpose of learning this course is to:***
CLR-1:	*understand the basics of semiconductor characterization techniques*
CLR-2:	*analyze the given sample data of different materials characterization*
CLR-3:	*study the surface and microstructural properties*
CLR-4:	*study the device characterization*
CLR-5:	*understand the various techniques involved in semiconductor technology*

Course Outcomes (CO):	***At the end of this course, learners will be able to:***	***Programme Outcomes (PO)***		
		1	***2***	***3***
CO-1:	*apply knowledge of characterization techniques using E-beam an X-ray*	3	3	2
CO-2:	*perform morphological Characterization of different surfaces*	3	3	3
CO-3:	*apply the knowledge of suitable optical and electrical characterization techniques*	3	3	2
CO-4:	*analyze device characteristics and perform case studies*	3	3	2

Module-1 - Electron Beam and X-ray Characterization Techniques	***15 Hour***
Secondary Ion Mass Spectrometry (SIMS), Auger Electron Spectroscopy (AES), Low-Energy Electron Diffraction (LEED), X-Ray Diffraction (XRD), Energy-Dispersive X-Ray Spectroscopy (EDS), X-Ray Photoelectron Spectroscopy (XPS), X-Ray Fluorescence (XRF) *Practice: (Demonstrations and Data analysis) Analyze and Identifying different phases present in the samples from given XRD data. (XPS): Identifying various elements present in a given sample and concentration using a given XPS data*	
Module-2 - Morphology Characterization Techniques	***15 Hour***
Atomic Force Microscopy (AFM), Scanning Tunnelling Microscopy (STM). Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), Electron Beam Induced Current (EBIC) Microscopy *Practice: (Demonstration of SEM, TEM AFM/STM): Estimating the grain size/nanorod size for given SEM/TEM images using Image-J software. AFM: roughness determination, STM: Tunneling and surface morphology*	
Module-3 - Optical and Electrical Characterization Techniques	***15 Hour***
Ellipsometry, UV-Visible spectroscopy Fourier Transform Infrared Spectroscopy (FTIR), Photoluminescence (PL), Temperature-dependent Photoluminescence (PL), Raman Spectroscopy, Resistivity, Sheet Resistance and the Four Point Probe method, Hall Effect: Resistivity Measurements and majority carrier concentration, Deep Level Transient Spectroscopy (DLTS), C-V characterization: carrier concentration and interface state density measurements *Practice: Demonstration of PL and Raman spectroscopy Bandgap, Fermi Energy and Defects energy level extraction Hall Effect: carrier concentration, mobility measurement*	
Module-4 - Device Characterizations Case Studies	***15 Hour***
Device Characterizations case studies: MOSFET Characterizations: Threshold voltage, Sub threshold Swing, Interface states. Solar cell Characterizations: Spectral response, Fill factor, Efficiency. Photodetector characterizations: Responsivity, Spectral Response *Practice: Estimation of threshold voltage (VT), Sub-threshold swing (SS) and effective mobility of a MOSFET from CV data, Photodetector performance (Spectral response, Responsivity) extraction using experimentally available data. (Solar Cell): Fill factor and Efficiency of a Solar cell.*	

Learning Resources	1. *Dieter K. Schroder, "Semiconductor Material and Device Characterization" John Wiley & Sons, INC, 3rd Edition.2006* 2. *Surender Kumar Sharma, "Handbook of Materials Characterization" Springer International Publishing, 2018* 3. *Khalid Sultan, "Practical Guide to Materials Characterization: Techniques and Applications" Wiley online library, 2022* 4. *S. M. Sze"VLSI technology" McGraw Hill Education, Second edition. 2017*	5. *Yang Leng, "Materials Characterization: Introduction to Microscopic and Spectroscopic Methods" Wiley online library, 2013.* 6. *Manijeh Razeghi, Fundamentals of Solid-State Engineering, Springer Cham, 2019* 7. *Sateesh Kumar, "Advanced Materials Characterization Basic Principles, Novel Applications, and Future Directions" Routledge, Taylor & Francis, 2023*

Learning Assessment

	Bloom's Level of Thinking	*Continuous Learning Assessment (CLA)*				*Summative Final Examination (40% weightage)*	
		Formative CLA-1 Average of unit test (45%)		*Life Long Learning CLA-2 (15%)*			
		Theory	*Practice*	*Theory*	*Practice*	*Theory*	*Practice*
Level 1	*Remember*	*15%*	-		*15%*	*15%*	-
Level 2	*Understand*	*25%*	-		*25%*	*25%*	-
Level 3	*Apply*	*30%*	-		*30%*	*30%*	-
Level 4	*Analyze*	*30%*	-		*30%*	*30%*	-
Level 5	*Evaluate*	-	-	-	-	-	-
Level 6	*Create*	-	-	-	-	-	-
	Total	*100 %*		*100 %*		*100 %*	

Course Designers		
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts
1. Dr. Saravanan Somasundaram, EMMVEE Group, Bangalore mailto: shrisharavanan@yahoo.co.uk	*1. Prof. S. Balakumar, University of Madras, balakumar@unom.ac.in*	*1. Dr. A. Karthigeyan, SRMIST*
2. Dr. Shanmugasundaram Sakthivel, ARCI, Hyderabad, mailto:ssakthivel@arci.res.in	*2. Prof. V Subramanian, IIT Madras, manianvs@iitm.ac.in*	*2. Dr. Elangovan Elamurugu, SRMIST*

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