SRM UNIVERSITY
FACULTY OF ENGINEERING AND TECHNOLOGY

SCHOOL OF COMPUTING
DEPARTMENT OF CSE
COURSE PLAN

Course Code : 15CS202
Course Title : Digital System Design
Semester : III
Course Time : JULY – DEC 2016

Day	B slot/ B1		D slot/ B2	
	Hour	Timing	Hour	Timing
Day 1	--	--	--	--
Day 2	6,7	12.30-2.15 P.M	1,2	8.00-9.40 A.M
Day 3	--	--	--	--
Day 4	8	2.20-3.10A.M	3	9.45-10.35 A.M
Day 5	4	10.40-11.30A.M	9	3.15-4.05 A.M

Location : TECH PARK

Faculty Details

Sec.	Name	Office	Office hour	Mail id
Group 1	Dr.A.PANDIAN	Tech Park	Monday - Friday	pandian.a@ktr.srmuniv.ac.in
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PURPOSE	To understand the basics of Boolean algebra and the operation of logic components, combinational, sequential circuits and VHDL.							
INSTRUCTIONAL OBJECTIVES		**STUDENT OUTCOMES**						
At the end of the course, student will be able to								
1.	Apply the principles of Boolean algebra to manipulate and minimize logic expressions.	a						
2.	Apply two-level logic functions with AND, OR, NAND, NOR and XOR gates	a						
3.	Use K-maps and table method to minimize and optimize two-level logic functions up to	a	b					

	5 variables.							
4.	Design combinational circuits using decoders, ROM and transmission gates.	a	b					
5.	Design finite state machines using various types of flip-flops and combinational circuits with prescribed functionality	a	b					
6.	Use the VHDL language for representation of digital signals	a						

Session	Description of Topic	Contact hours	C-D-I-O	IOs	Reference
	UNIT I: Introduction to Number Systems and Boolean Algebra	**9**			
1.	Digital and Analog Basic Concepts, Some history of Digital Systems	1	C	1	1
2.	Introduction to number systems , Binary numbers , Number Base Conversion	1	C	1	1,2,3,4
3.	Complement Codes, Binary Arithmetic , Binary codes: BCD, Weighted codes -2421,8421,gray code	3	C	1	1,2,3,4
4.	Binary Logic functions, Boolean Algebra, Theorems and Properties of Boolean Algebra	4	C	1,2	1,2,3,4
	UNIT II: Minimization techniques in digital Logic	**9**			
5.	Canonical forms, Generation of Switching Equations from Truth Table	2	C	1,2	1,2,3,4
6.	K-map(Karnaugh map) 2 ,3,4 and 5 variables, K map with Don't care terms	3	C	3	1,2
7.	Quine Mc-Cluskey minimization technique, Quine Mc-Cluskey using Don't Care Terms	3	C	3	1,2
8.	Mixed logic Combinational circuits	1	C,D	4	1,2
	UNIT III: Design of Combinational Logic Circuits	**9**			
9.	Introduction to Combinational Circuits, Analysis and Design Procedure	1	C	4	1,2
10.	Binary Adder, Subtractor, Carry Look Ahead Generator, Decimal Adder, Binary Multiplier	4	C,D	4	1,2,3,4
11.	Decoder, Encoder, Priority Encoder, Digital Multiplexer, Magnitude Comparator	4	C,D	4	1,2,3,4
	UNIT IV: Synchronous Sequential Circuits	**10**			
12.	Flip-flops- SR,D,JK,T	2	C	5	1,2
13.	Analysis of Synchronous Sequential Circuit	1	C	5	1,2
14.	State Reduction and Assignment	1	D,I	5	1,2
15.	Design of Synchronous Sequential Circuit: Sequence Detector for D,JK,T flip-flops	2	D,I	5	1,2,3,4
16.	BCD Counter, Registers: Shift Registers, Analysis of Asynchronous Sequential Circuit: Transition Table, Flow Table	4	D,I	5	1,2,3,4
	UNIT V: Hardware Description Language	**8**			
17.	Introduction to HDL: Module Declaration, Gate delays, Boolean Expressions, User Defined Primitives	2	C	6	2,5,6
18.	HDL models for Combinational Circuits: Gate Level Modeling, Data Flow , Behavioral Modeling	3	D,I	6	2,5,6
19.	HDL flow Behavioural Sequential Circuits: HDL Models for Flip-Flops and Latches	3	D,I	6	2,5,6
	Total contact hours	45			

LEARNING RESOURCES	
Sl. No.	**TEXT BOOKS**
1.	John . M. Yarbrough," Digital Logic: Applications and Design", Cengage Learning, Reprint 2009
2.	M.Morris Mano, Michael D. Ciletti ,"Digital Design with an Introduction to the verilog HDL", Pearson Publications, Fifth edition 2014.
	REFERENCE BOOKS/OTHER READING MATERIAL
3.	Roth , Kinney,"Fundamentals of Logic Design", Cengage Learning, 7th edition, 2015
4.	Donald D. Givone, " Digital Principles and Design", McGraw Hill Education (India) Pvt. Ltd,2013
5.	Richard S. Sandige, Michael L Sandige, " Fundamentals of Digital and Computer Design with VHDL", McGraw Hill, 2014
6.	Stephen Brown, Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design",Second Edition, McGraw Hill, 2015.

Course nature		**Theory**					
Assessment Method (Weightage 100%)							
In-semester	**Assessment tool**	Cycle test I	Cycle test II	Cycle Test III	Surprise Test	Quiz	**Total**
	Weightage	**10%**	**15%**	**15%**	**5%**	**5%**	**50%**
End semester examination Weightage :							**50%**