SRM INSTITUTE OF SCIENCE AND TECHNOLOGY
FACULTY OF ENGINEERING AND TECHNOLOGY
SCHOOL OF COMPUTING
DEPARTMENT OF CSE
COURSE PLAN

Course Code /Title: 15CS203 / COMPUTER SYSTEM ARCHITECTURE
Year / Semester: II / 3rd
Course Duration: July 2018-Dec 2018
Groups and Slots: C1 and C2 Slot

Period	1	2	3	4	5	6	7	8	9	10
Time	8.00-8.50	8.50-9.40	9.45-10.35	10.40-11.30	11.35-12.25	12.30-1.20	1.25-2.15	2.20-3.10	3.15-4.05	4.05-4.55
Day 1										
Day 2										
Day 3	C1	C1				C2	C2			
Day 4				C2					C1	
Day 5					C1					C2

Location: SRM Institute of Science and Technology -Tech Park
TP403, TP406, TP501TP502, TP503, TP504, TP505, TP506, TP606
FACULTY DETAILS

BATCH	NAME	STAFF ROOM	OFFICE HOURS	MAIL ID	VENUE
B1	Dr.C.MALATHY	TP615	Monday-Friday	malathy.c@ktr.srmuniv.ac.in	TP506
B1	Mrs.T.MANORANJITHAM	TP106	Monday-Friday	manoranjitham.t@ktr.srmuniv.ac.in	TP406
B1	Mr. S.JAGADEESAN	TP708	Monday-Friday	jagadeesan.s@ktr.srmuniv.ac.in	TP501 TP502
B1	Mr.GOBINATH	TP810	Monday-Friday	gobinathsimha6583@gmail.com	TP503
B1	Mr. T.BALACHANDER	TP711A	Monday-Friday	balachander.t@ktr.srmuniv.ac.in	TP606
B1	Mrs DORATHI JEYASEELI	TP810	Monday-Friday	dorathijayaseeli.jd@ktr.srmuniv.ac.in	TP505
B1	Mr.M.V.RANJITH KUMAR	UB1112	Monday-Friday	ranjithkumar.mu@ktr.srmuniv.ac.in	TP504
B2	Mrs. I.SHABEENA BEGAM	TP810	Monday-Friday	i.shabeenabegam22@gmail.com	TP504
B2	Mrs.D.VANUSHA	TP003A	Monday-Friday	vanusha.d@ktr.srmuniv.ac.in	TP403
B2	Mrs.S.S.SARANYA	TP608A	Monday-Friday	saranya.ss@ktr.srmuniv.ac.in	TP501, TP502
B2	Mr.SELVIN PAUL PATER	TP710A	Monday-Friday	selvinpaulpeter.j@ktr.srmuniv.ac.in	TP606
B2	Mr.M.V.RANJITH KUMAR	UB1112	Monday-Friday	ranjithkumar.mu@ktr.srmuniv.ac.in	TP505
B2	Ms. M.LAKSHMI PRIYA	UB1111	Monday-Friday	lakshmipriya.m@ktr.srmuniv.ac.in	TP503

TEXT BOOKS

1. Carl Hamacher, ZvonkoVranesic, SafwatZaky, "Computer Organization", McGraw-Hill, Fifth Edition, Reprint 2015.
2. Pal Chaudhuri,"Computer Organization and Design",PHIPvt, Third Edition,2008.

REFERENCES

3. Ghosh T. K., "Computer Organization and Architecture", Tata McGraw-Hill, Third Edition,2011.
4.William Stallings, "Computer Organization and Architecture – Designing for Performance", Pearson Education, Tenth Edition,2015.
5.BehroozParahami, "Computer Architecture", Oxford University Press, Eighth Impression,2015.
6.John P. Hayes, "Computer Architecture and Organization", McGraw Hill, Third Edition,2015.
7.Kai Hwang &NareshJotwani,"Advanced Computer Architecture", McGraw Hill, Third Edition, 2016.
8.Carl Hamacher, ZvonkoVranesic, SafwatZaky, NaraigManjikian,"Computer Organization and Embedded Systems", McGraw-Hill, Sixth Edition, 2012.
9.P.V.S. Rao,"Computer System Architecture", PHI Learning Pvt Ltd, 2011

INSTRUCTIONAL OBJECTIVES

1. To study basic structures and functions of Control Unit, Memory unit, Storage devices and Input/output organization in a computer system.
2. To understand the representations of signed and unsigned numbers and arithmetic algorithms such as addition, subtraction, multiplication and division.
3. To learn the concepts of various instruction set architectures (ISA), addressing modes to understand the concepts of pipelining and superscalar execution.
4. To understand the various classes of instruction types such as data movement, arithmetic, logical and flow control and to study the various control unit design.
5. To identify the various memory technologies and memory hierarchies found in a computer and to describe the various ways of organizing cache memory and appreciate the cost-performance tradeoffs.
6. To understand how interrupts are used to implement I/O control and data transfers and to identify various types of buses in a computer system and understand how devices compete for a bus and are granted access to the system bus.

ASSESSMENT DETAILS

ASSESSMENT	MARKS
Cycle Test-I	**10%**
Cycle Test-II	**15%**
Cycle Test-III	**15%**
Surprise Test	**5%**
Quiz and Assignments	**5%**

TEST SCHEDULE

S.No	TEST	TOPICS	DURATION
1	Cycle Test-I	UNIT-1	2 Periods
2	Cycle Test-II	UNIT - 2 and 3	2 Periods
3	Cycle Test-II	UNIT - 4 and 5	2 Periods
4	Surprise Test	From Completed Units	1 Period

DETAILED LESSON PLAN

UNIT I BASIC STRUCTURE OF COMPUTERS

Functional units – Basic operational concepts - Bus structures – Memory locations and addresses – Memory operations – Instruction and instruction sequencing – Addressing modes – Assembly language – Basic I/O operations - Evolution of Parallel computers, System Attributes to Performance-Multiprocessors and Multicomputers**(8 Hrs)**

Session	Description of Topic	Time (Mins)	Ref	Teaching Method	Testing Method
	BASIC STRUCTURE OF COMPUTERS				
1.	Computer Types, Functional units, Basic operational concepts , Bus structures	50	TB1,TB2,TB4	BB	Quiz,Group Discussion
2.	Memory locations and addresses, Memory operations	50	TB1	BB	Group Discussion
3.	Instruction and instruction sequencing,	50	TB1	BB	Group Discussion
4.	Assembly language ,Addressing modes	50	TB1, TB2, TB4	BB	Assignment, Group Discussion
5.	Basic I/O operations	50	TB1	BB	Group Discussion
6.	Evolution of Parallel computers, System Attributes to Performance	50	RB8	BB	Group Discussion
7.	System Attributes to Performance	50	RB7	BB	Quiz,Group Discussion
8.	Multiprocessors and Multicomputers	50	RB4, RB5, RB7	BB	Brain storming

UNIT II ARITHMETIC UNIT

Addition and subtraction of signed numbers – Design of fast adders – Multiplication of positive numbers – Signed operand multiplication, fast multiplication- Bit pair recoding of Multipliers, Carry Save Addition of summands – Integer division – Restoring Division, Non Restoring Division -Floating point numbers and operations.**(9 Hrs)**

	ARITHMETIC UNIT				
9.	Addition and subtraction of signed numbers	50	TB1	BB	SurpriseTest
10.	Design of fast adders	50	TB1	BB	Group Discussion, Brain storming
11.	Multiplication of positive numbers	50	TB1	BB	Group Discussion, SurpriseTest
12.	Signed operand multiplication	50	TB1	BB	Brain storming
13.	Fast multiplication-Bit pair recoding of Multipliers	50	TB1	BB	Group Discussion, Assignment
14.	Fast multiplication- Carry Save Addition of summands	50	TB1	BB	Group Discussion, AssignmentAss
15.	Integer division- Restoring Division	50	TB1	BB	Group Discussion, Assignment
16.	Integer division- Non Restoring Division	50	TB1	BB	Group Discussion, Assignment
17.	Floating point numbers and its operations	50	TB1 RB4	BB	Group Discussion, Assignment

UNIT III BASIC PROCESSING UNIT

Fundamental concepts – Execution of a complete instruction – Multiple bus organization – Hardwired control – Micro programmed control – Pipelining – Basic concepts – Data hazards – Instruction hazards – Influence on Instruction sets – Data path and control considerations-Superscalar operation**(11 Hrs)**

	BASIC PROCESSING UNIT				
18.	Fundamental concepts	50	TB1	BB	Brain storming
19.	Execution of a complete instruction, Multiple bus organization	50	TB1, TB2	BB	Group Discussion
20.	Hardwired control	50	TB1, TB2, RB4, RB6	BB	Group Discussion
21.	Micro programmed control	50	TB1, TB2, RB4, RB6	BB	Group Discussion
22.	Micro programmed control	50	TB1, TB2, RB4, RB6	BB	Group Discussion
23.	Pipelining- Basic concepts,	50	TB1, RB5	BB	Quiz,Group Discussion
24.	Pipelining -Data hazards, Instruction hazards	50	TB1	BB	Group Discussion
25.	Pipelining - Instruction hazards,	50	TB1	BB	Group Discussion
26.	Pipelining- Influence on Instruction sets	50	TB1	BB	Group Discussion
27.	Pipelining- Datapath and control considerations	50	TB1	BB	Group Discussion
28.	Superscalar Operation	50	RB8	BB	Quiz,Group Discussion

UNIT IV MEMORY SYSTEM

Basic concepts of memory system – Semiconductor RAMs – ROMs – Speed – size and cost – Cache memories – Performance consideration – Virtual memory – Memory Management requirements – Secondary storage .**(8 Hrs)**

	UNIT IV: MEMORY UNIT				
29.	Basic concepts of memory system	50	TB1, TB2	BB	Quiz,Group Discussion
30.	Semiconductor RAMs	50	TB1, TB2	BB	Quiz,Group Discussion
31.	ROMs Speed, size and cost	50	TB1, TB2	BB	Quiz,Group Discussion

32.	Cache memories	50	TB1, RB3, RB4, RB5	BB	SurpriseTest
33.	Performance consideration	50	TB1	BB	Group Discussion
34.	Virtual memory	50	TB1 RB3, RB5	BB	Group Discussion
35.	Memory Management requirements	50	TB1	BB	Group Discussion
36.	Secondary storage	50	TB1, TB2, RB4	BB	Quiz,Group Discussion
UNIT V - INPUT – OUTPUT PROCESSING Introduction to Data transfer techniques-Bus Interface- UART, Interfacing UART to Microprocessor Unit - Programmed IO, Interrupt driven IO, Direct Memory Access - I/O Interrupt, I/O channel/Processor - Interconnection Standards – PCI Bus, SCSI, USB, Firewire, SATA, SAS, PCI Express.**(9 Hrs)**					
	INPUT – OUTPUT ORGANIZATION				
37.	Introduction to Data transfer techniques	50	TB2	BB	Group Discussion
38.	Bus Interface – UART	50	TB2	BB	Group Discussion
39.	Interfacing UART to Microprocessor Unit	50	TB2	BB	Group Discussion, Assignment
40.	Programmed IO, Interrupt driven IO	50	TB1, TB2, RB4	BB	Group Discussion
41.	Direct Memory Access	50	TB1, TB2, RB4	BB	Group Discussion
42.	I/O Interrupt	50	TB1, TB2	BB	Group Discussion
43.	I/O channel/Processor	50	TB2	BB	Group Discussion
44.	Interconnection Standards – PCI Bus, SCSI, USB	50	RB9	BB	Group Discussion, Assignment
45.	Interconnection Standards -Firewire, SATA, SAS, PCI Express	50	RB9	BB	Group Discussion, Assignment
	Total contact hours	**45**			

Course Co-coordinator,

S.Jagadeesan

Approved By,

Dr.B.Amutha

HOD/CSE