EC0323 COMMUNICATION LAB II

LABORATORY MANUAL

SEMESTER V

DEAPRTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING
SRM UNIVERISTY
(Under SECTION 3 of the UGC Act, 1956)
S.R.M. NAGAR, KATTANKULATHUR – 603203.
KANCHEEPURAM DISTRICT

SRM UNIVERSITY
(Under section 3 of UGC Act 1956)

Department of Electronics and Communication Engineering

EC0323

Communication Lab II

Laboratory Manual

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June 2014

Revision: 4

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EC0323	COMMUNICATION LAB-II	0	0	3	2
	Prerequisite : nil				

PURPOSE

To help the students to experiment on digital communication systems using kits and to use software's to simulate them.

INSTRUCTIONAL OBJECTIVES

To carry out experiments on various digital communications modulation schemes using kits. MATLAB software is used to simulate the digital modulation techniques.

LIST OF EXPERIMENTS **45**

HARDWARE

1. FSK Modulation and Demodulation.
2. PSK Modulation and Demodulation.
3. Pulse Code Modulation and Demodulation
4. Delta Modulation and Demodulation
5. Time Division Multiplexing
6. Data Formatting
7. Differential pulse code modulation and demodulation

SOFTWARE –MATLAB

8. FSK Modulation and Demodulation
9. PSK Modulation and Demodulation
10. QPSK
11. ASK Modulation and Demodulation
12. DPSK Modulation and Demodulation
13. Delta modulation and demodulation

TOTAL 45

REFERENCE: LABORATORY MANUAL

EC0323 – Communication Lab II

Course designed by		Department of Electronics & Communication Engineering											
1	Program outcome	a	b	c	d	e	F	g	h	i	j	k	
			x	x	x		x						
2	Category	General (G)	Basic Sciences (B)		Engineering Sciences and Technical Arts(E)			Professional Subjects(P)					
								x					
3	Broad area (for 'P'category)	Communication	Signal Processing		Electronics			VLSI		Embedded			
		x											
4	Staff responsible for preparing the syllabus	Mr.Diwakar R. Marur Mrs. CT. Manimegalai Ms.T.Ramya Mrs.M.Sangeetha											
5	Date of preparation	December 2006											

S.R.M University
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

Sub Code : EC0323 Semester : V
Sub Title : Communication lab II Course Time : Jul–Dec 2011

Pre_requisite : Nil
Co_requisite : EC0307 Digital Communication

Program Outcome

b. Graduate will demonstrate the ability to identify, formulate and solve engineering problem

Experiment 7: To identify the various encoding schemes for a given data stream

c. Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data

Experiment 2 : To analyze a PCM system and interpret the modulated and demodulated waveforms for a sampling frequency of 4KHz.

Experiment 3 : To analyze a DPCM system and interpret the modulated and demodulated waveforms for a sampling frequency of 8KHz.

Experiment 4 : To analyze a Delta modulation system and interpret the modulated and demodulated waveforms.

Experiment 5: To analyze a FSK modulation system and interpret the modulated and demodulated waveforms.

Experiment 6: To analyze a PSK modulation system and interpret the modulated and demodulated waveforms.

d. Graduate will demonstrate the ability to design a system, component or process as per needs and specification

Experiment 1:To demonstrate Time Division Multiplexing and demultiplexing process using Pulse amplitude modulation signals

f. Graduate will demonstrate the skills to use modern engineering tools, software's and equipment to analyze problems

Experiment 8: To simulate Binary Amplitude shift keying technique using MATLAB software

Experiment 9: To simulate Binary Frequency shift keying technique using MATLAB software

Experiment 10: To simulate Binary Phase shift keying technique using MATLAB software

Experiment 11: To simulate Quadrature Phase shift keying technique using MATLAB software

Experiment 11: To simulate Differential Phase shift keying technique using MATLAB software

Sub Code : EC0323 Semester : V
Sub Title : Communication Lab II Course Time : Jul- Dec 2011

Pre Requisite
Course Requisite : EC0307 Digital Communication

Instructional Objective and Program Outcome

S.No.	Instructional Objective	Program Outcome	Experiment Details
1	To carry out experiments on various digital communications modulation schemes using kits.	**c**. Graduate will demonstrate the ability to design and conduct experiments, analyze and interpret data	Experiment 2 : To analyze a PCM system. and interpret the modulated and demodulated waveforms for a sampling frequency of 4KHz Experiment 3 : To analyze a DPCM system. and interpret the modulated and demodulated waveforms for a sampling frequency of 8KHz Experiment 4 : To analyze a Delta modulation system. and interpret the modulated and demodulated waveforms. Experiment 5: To analyze a FSK modulation system. and interpret the modulated and demodulated waveforms. Experiment 6: To analyze a PSK modulation system. and interpret the modulated and demodulated waveforms.
		b. Graduate will demonstrate the ability to identify, formulate and solve engineering problem	Experiment 7: To identify the various encoding schemes for a given data stream.
		d. Graduate will demonstrate the ability to design a system, component or process as per needs and specification	Experiment 1:To demonstrate Time Division Multiplexing and demultiplexing process using Pulse amplitude modulation signals.
2	To simulate the digital modulation techniques using	**f.** Graduate will demonstrate the	Experiment 8: To simulate Binary Amplitude

	MATLAB software.	skills to use modern engineering tools, software's and equipment to analyze problems.	shift keying technique using MATLAB software Experiment 9: To simulate Binary Frequency shift keying technique using MATLAB software Experiment 10: To simulate Binary Phase shift keying technique using MATLAB software Experiment 11: To simulate Quadrature Phase shift keying technique using MATLAB software Experiment 12: To simulate Differential Phase shift keying technique using MATLAB software

S.R.M University
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

Sub Code : EC0323 Semester : V
Sub Title : Communication Lab II Course Time : Jul–Dec 2011

Pre Requisite :
Course Requisite : EC0307 Digital Communication

EXPERIMENTS DETAILS

S.No.	Experiments Detail	Equipments Required	Specifications
1	To demonstrate Time Division Multiplexing and demultiplexing process using Pulse amplitude modulation signals.	TDM Trainer kit CRO(30 MHz)	Crystal Frequency 6.4MHz Analog Input channel:4 Onboard analog signal:250Hz,500Hz,1KHz,2KHz Sampling Rate:16Khz/Channel Clock Regeneration at receiver: Using PLL Low pass filter cut off frequency:3.4Khz
2	To analyze a PCM system. and interpret the modulated and demodulated waveforms for a sampling frequency of 4KHz .	PCM Trainer Kit CRO(30 MHz)	Regulated power supply IC 7805 ,IC7812 : +5V and +12 V at 300 mA. AF Signal generator IC TL084: 200Hz, Sinewave Clock Generator IC555:64KHz and 4KHz DC Source : +5V LPF: Cut off frequency 200Hz Amplifier ICTL084: Gain 0 to 3. Sample and hold: LF198/LF298/LF398 A/D Converter IC ADC0808 : 8 bit P/S shift register SN74LS166 : 8 bit S/P shift register SN74LS164 : 8 bit DAC ICDAC 0808: 8 bit
3	To analyze a DPCM system and interpret the modulated and demodulated waveforms for a sampling frequency of 8 KHz. .	DPCM Trainer Kit CRO(30 MHz) ADCL-07 Kit	Regulated power supply IC 7805 ,IC7812 : +5V and +12 V at 300 mA. AF Signal generator IC TL084:400Hz, Sinewave Clock Generator IC 555 : 64KHz and 8KHz DC Source :0 to 290mV LPF: Cut off frequency 400Hz Amplifier ICTL084: Gain 0 to 3. Sample and hold: LF198/LF298/LF398 A/D Converter IC ADC0808 : 8 bit P/S shift register SN74LS166 : 8 bit S/P shift register SN74LS164 : 8 bit DAC ICDAC 0808: 8 bit

4	To analyze a Delta modulation system and interpret the modulated and demodulated waveforms.	Delta modulation Trainer Kit CRO(30 MHz)	Regulated power supply IC 7805 ,IC7812 : +5V and +12 V at 300 mA. AF Signal generator IC TL084: 100Hz, Sinewave Clock Generator IC 555 : 4 Khz DC Source : 0 to +5V LPF: Cut off frequency 100hz Buffer/Signal shaping circuit:IC TL084 Voltage comparator: IC LM339 DAC ICDAC 0808: 4 bit Amplifier ICTL084: Gain 0 to 6. UPdown Counter:IC74LS191, 4 bit.
5	To analyze a FSK modulation system and interpret the modulated and demodulated waveforms.	FSK Trainer Kit CRO(30 MHz)	VCO: IC XR2206 Comparator:LM565
6	To analyze a PSK modulation system and interpret the modulated and demodulated waveforms.	PSK Trainer Kit CRO(30 MHz)	4 channel analog Multiplexer: IC CD 4052 opampTL084
7	To identify the various encoding schemes for a given data stream.	Data formatting Trainer Kit CRO(30 MHz)	On-board carrier: Sine waves synchronized to transmitted data at 1.44MHz,960 KHz(0 deg. Phase),960 KHz(90 deg. Phase)
8	To simulate Binary Amplitude shift keying technique using MATLAB software	MATLAB software	version7.2
9	To simulate Binary Frequency shift keying technique using MATLAB software	MATLAB software	version7.2
10	To simulate Binary Phase shift keying technique using MATLAB software	MATLAB software	version7.2
11	To simulate Quadrature Phase shift keying technique using MATLAB software	MATLAB software	version7.2
12	To simulate Differential Phase shift keying technique using MATLAB software	MATLAB software	version7.2

EC0323 Laboratory Policies and Report Format

Reports are due at the beginning of the lab period. The reports are intended to be a complete documentation of the work done in preparation for and during the lab. The report should be complete so that someone else familiar with digital communication could use it to verify your work. The prelab and postlab report format is as follows:

1. A neat thorough prelab must be presented to your Staff Incharge at the beginning of your scheduled lab period. **Lab reports should be submitted on A4 paper.** Your report is a professional presentation of your work in the lab. Neatness, organization, and completeness will be rewarded. Points will be deducted for any part that is not clear.

2. In this laboratory students will work in teams of three. However, the lab reports will be written individually. Please use the following format for your lab reports.

a. **Cover Page:** Include your name, Subject Code, Section No., Experiment No. and Date.

b.**Objectives:** Enumerate 3 or 4 of the topics that you think the lab will teach you. DO NOT REPEAT the wording in the lab manual procedures. There should be one or two sentences per objective. Remember, you should write about what you will learn, not what you will do.

c. **Questions:** Specific questions(Prelab and Postlab) asked in the lab should be answered here.

3. Your work must be original and prepared independently. However, if you need any guidance or have any questions or problems, please do not hesitate to approach your staff incharge during office hours. Copying any prelab/postlab will result in a grade of 0. The incident will be formally reported to the University and the students should follow the dress code in the Lab session.

4. Each laboratory exercise (circuit) must be completed and demonstrated to your Staff Incharge in order to receive working circuit credit. This is the procedure to follow:

a. Circuit works: If the circuit works during the lab period (3 hours), call your staff incharge, and he/she will sign and date it.. This is the end of this lab, and you will get a complete grade for this portion of the lab.

b. Circuit does not work: If the circuit does not work, you must make use of the open times for the lab room to complete your circuit. When your circuit is ready, contact your staff incharge to set up a time when the two of you can meet to check your circuit.

5. Attendance at your regularly scheduled lab period is required. An unexpected absence will result in loss of credit for your lab. If for valid reason a student misses a lab, or makes a reasonable request in advance of the class meeting, it is permissible for the student to do the lab in a different section later in the week if approved by the staff incharge of both the sections. Habitually late students (i.e.,

students late more than 15 minutes more than once) will receive 10 point reductions in their grades for each occurrence following the first.

6. Final grade in this course will be based on laboratory assignments. All labs have an equal weight in the final grade. Grading will be based on pre-lab work, laboratory reports, post-lab and in-lab performance (i.e., completing lab, answering laboratory related questions, etc.,).The Staff Incharge will ask pertinent questions to individual members of a team at random. Labs will be graded as per the following grading policy:

Pre-Lab Work	10.00%
In-Lab Performance	20.00%
Post Lab Work	10.00%

7. **Reports Due Dates**: Reports are due one week after completion of the corresponding lab. A late lab report will have 10% of the points deducted for being one day late. If a report is 2 days late, a grade of 0 will be assigned.

8. **Systems of Tests:** Regular laboratory class work over the full semester will carry a weightage of 75%. The remaining 25% weightage will be given by conducting an end semester practical examination for every individual student

Laboratory Report Cover Sheet

SRM University
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

EC0323 Communication Lab II Laboratory
Fifth Semester, 2014-15 (odd semester)

Name :

Register No. :

Day / Session : **Day order 1 AN / Day Order 4 FN**

Venue : communication Lab/Computing Lab 10th floor
Title of Experiment :

Date of Conduction :

Date of Submission :

Particulars	Max. Marks	Marks Obtained
Pre-lab	10	
Lab Performance	20	
Post-lab	10	
Lab Report	10	
Total	**50**	

REPORT VERIFICATION

Date :

Staff Name : **Mrs.T.Theresal/ Anantha Venkatesan**

Signature :

CONTENTS

12.4 Theory
12.5 Algorithm
12.6 Test Procedure
12.7 Lab result
12.8 Post lab

Appendix

1. TIME-DIVISION MULTIPLEX1NG

1.1.OBJECTIVE

To demonstrate Time Division Multiplexing and demultiplexing process using Pulse amplitude modulation signals.

1.2. HARDWARE REQUIRED

1. TDM Trainer Kit—ST2102
2. CRO
3. Patch Chords
4. Probes

1.3. INTRODUCTION

An important feature of pulse-amplitude modulation is a conservation of time. That is, for a given message signal, transmission of the associated PAM wave engages the communication channel for only a fraction of the sampling interval on a periodic basis. Hence, some of the time interval between adjacent pulses of the PAM wave is cleared for use by the other independent message signals on a time-shared basis. By so doing, we obtain a time-division multiplex system (TDM), which enables the joint utilization of a common channel by a plurality of independent message signals without mutual interference.

Each input message signal is first restricted in bandwidth by a low-pass pre-alias filter to remove the frequencies that are nonessential to an adequate signal representation. The pre-alias filter outputs are then applied to a commutator, which is usually implemented using electronic switching circuitry. The function of the commutator is two-fold: (1) to take a narrow sample of each of the N input messages at a rate fs that is slightly higher than 2W, where W is the cutoff frequency of the pre-alias filter, and (2) to sequentially interleave these N samples inside a sampling interval Ts 1/fs. Indeed, this latter function is the essence of the time-division multiplexing operation. Following the commutation process, the multiplexed signal is applied to a pulse-amplitude modulator, the purpose of which is to transform the multiplexed signal into a form suitable for transmission over the communication channel.

At the receiving end of the system, the received signal is applied to a pulse- amplitude demodulator, which performs the reverse operation of the pulse amplitude modulator. The short pulses produced at the pulse demodulator output are distributed to the appropriate low-pass reconstruction filters by means of a decommutator, which operates in

synchronism with the commutator in the transmitter. . This synchronization is essential for satisfactory operation of the TDM system, and provisions have to be made for it.

1.4 BLOCK DIAGRAM

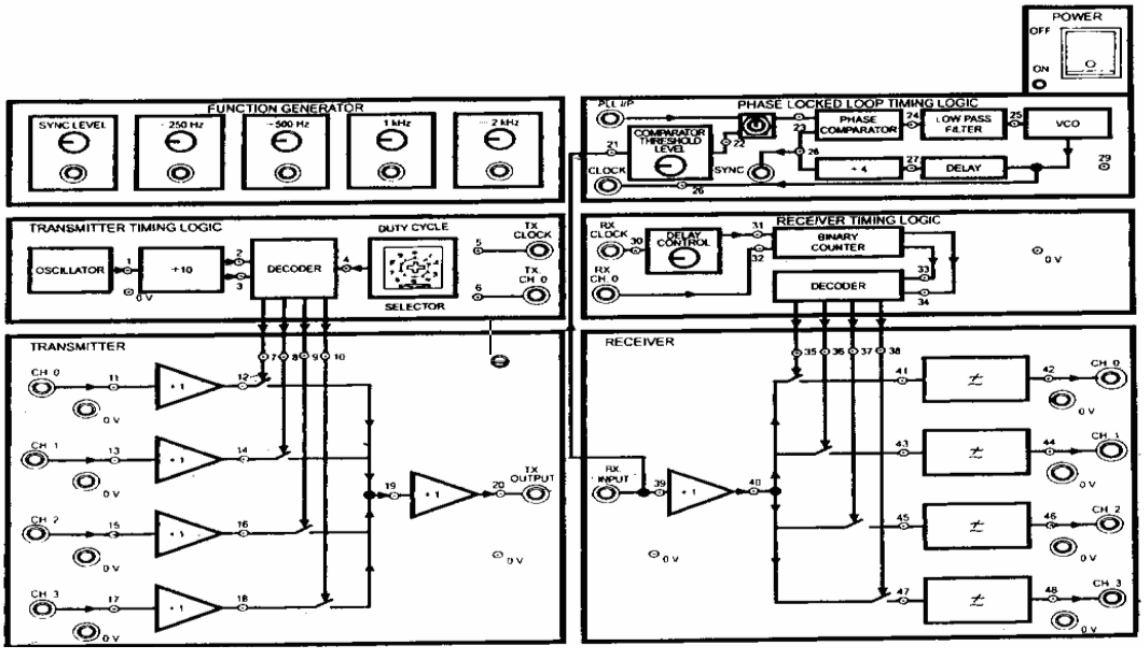


Figure 1.1 TDM Trainer Kit –ST2102 Block Diagram

1.5 PRELAB QUESTIONS

1. What is multiplexing?
2. Mention the types of multiplexing?
3. What is the need for multiplexing?
4. What is the bit rate of T1,T2,T3 and T4 carrier systems?
5. Compare synchronous and asynchronous TDM.
6. What are the functions of commutator switch?
7. Give the advantages of multiplexing.

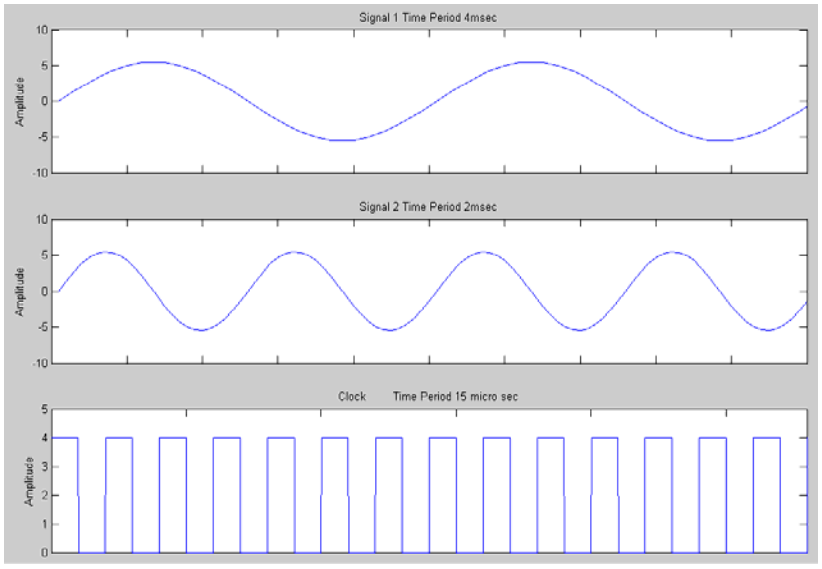
1.6 TEST PROCEDURE:

1. Take the signals from the function generator and give it to the channels (CH0 ... CH3) present in the transmitter using patch chords. Note down the amplitude and time period of each signal.
2. Measure the amplitude and time period at the transmitter output point.
3. Using a patch chord, connect transmitter output to receiver input.
4. For synchronization purpose, connect the transmitter clock and receiver clock and also transmitter CH0 and receiver CH0.

5. See the output before the filter and after the filter for all the channels connected.

1.7. MODEL GRAPH:

TRANSMITTER SECTION



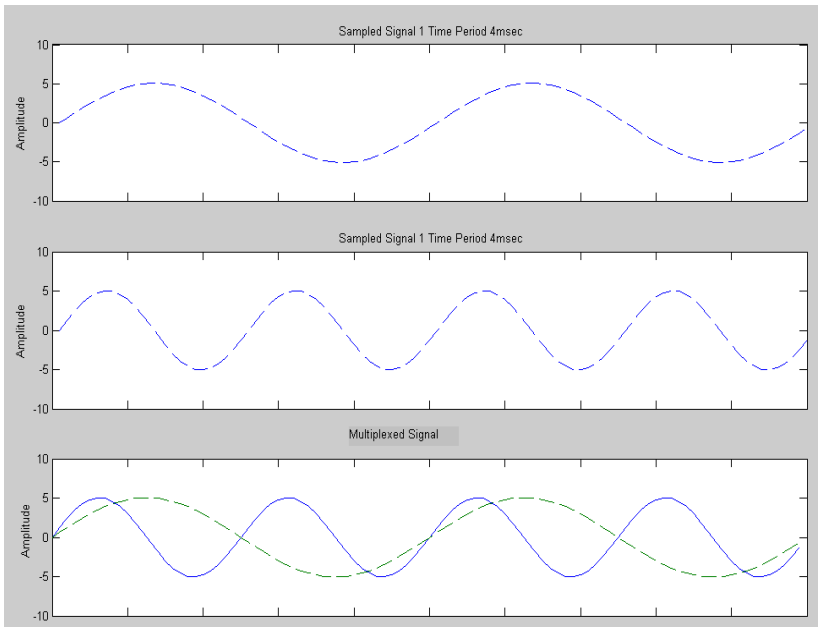


Figure 1.2 TDM Multiplexed Signal

MODEL GRAPH:

RECEIVER SECTION

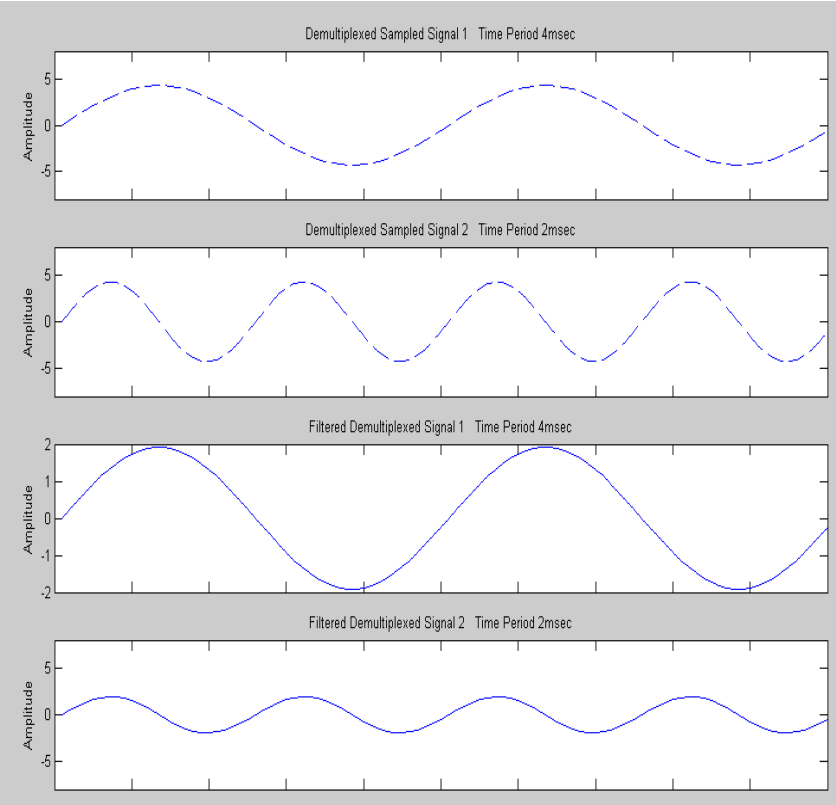


Figure 1.3 TDM Received Signal

1.8. OBSERVATION

Transmitter Section		**Receiver Section**	
Signal 1		**Demultiplexed Signal 1**	
Amplitude	**Time Period**	**Amplitude**	**Time Period**
Signal 2		**Demultiplexed Signal 2**	
Amplitude	**Time Period**	Amplitude	**Time Period**
Transmitter Output		**Filtered Demultiplexed Signal 1**	
Amplitude	**Time Period**	**Amplitude**	**Time Period**
		Filtered Demultiplexed Signal 1	
		Amplitude	**Time Period**

1.9. LAB RESULT

Time division multiplexing and de-multiplexing using PAM signals were performed and respective waveforms were plotted.

1.10. POST LAB QUESTIONS

1. Two signals $g_1(t)$ and $g_2(t)$ are to be transmitted over a common channel by means of time division multiplexing. The highest freq of $g_1(t)$ is 1 KHz and that $g_2(t)$ is 1.5 KHz. What is the minimum value of the permissible sampling rate? Justify your answer.
2. How is synchronization achieved in TDM?
3. Twenty four voice signals are sampled uniformly and then time division multiplexed. The sampling operation uses flat top samples with 1μs duration. The multiplexing operation includes provision for synchronization by adding an extra pulse of sufficient amplitude and also 1 μs duration. The highest frequency component of each voice signal is 3.4KHz.
    a. Assuming a sampling rate of 8 KHz, Find the spacing between successive pulses of the multiplexed signal.
    b. Repeat your calculation assuming the use of nyquist rate sampling.
4. What is the major drawback of digital communication?
5. Three signals m1,m2 and m3 are to be multiplexed.m1 and m2 have a 5 KHz bandwidth and m3 has 10KHz bandwidth. Design a commutator switching system so that each signal is sampled at its Nyquist rate.
6. Define bandwidth expansion factor.

2. PULSE CODE MODULATION AND DEMODULATION

2.1 OBJECTIVE

To analyze a PCM system and interpret the modulated and demodulated waveforms for a sampling frequency of 4 KHz.

2.2 HARDWARE REQUIRED

1. PCM modulator trainer kit-AET-68M
2. PCM Demodulator trainer kit-AET-68D
3. Storage oscilloscope
4. Digital multimeter

2.3 INTRODUCTION

In Pulse code modulation (PCM) only certain discrete values are allowed for the modulating signals. The modulating signal is sampled, as in other forms of pulse modulation. But any sample falling within a specified range of values is assigned a discrete value. Each value is assigned a pattern of pulses and the signal transmitted by means of this code. The electronic circuit that produces the coded pulse train from the modulating waveform is termed a coder or encoder. A suitable decoder must be used at the receiver in order to extract the original information from the transmitted pulse train.

This PCM system consists of

2.3.1. PCM Modulator (AET-68M):

1. Regulated power supply
2. Audio Frequency signal generator
3. Sample & Hold circuit
4. 8 Bit A/D Converter
5. 8 Bit Parallel-Serial Shift register
6. Clock generator/Timing circuit
7. DC source

2.3.2. PCM Demodulator (AET-68D):

1. Regulated power supply
2. 8 Bit Serial-Parallel to shift register
3. 8 Bit D/A converter
4. Clock generator

5. Timing circuit
6. Passive low pass filter
7. Audio amplifiers

2.4 BLOCK DIAGRAM

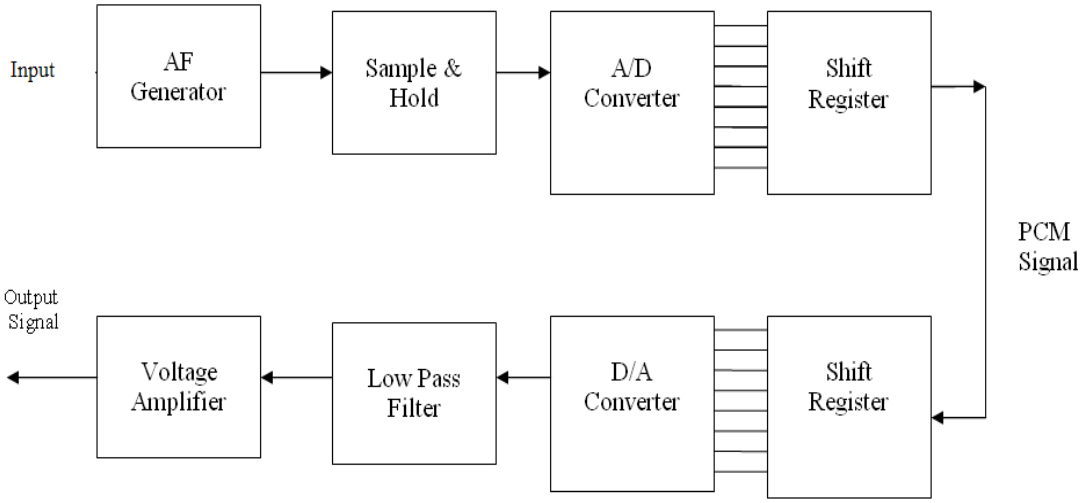


Fig 2.1. PCM Modulator AND Demodulator

Regulated power supply (68M & 68D):

This consists of a bridge rectifier followed by capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of +5V and +12V @ 300mA each to the on board circuits. These supplies have been internally connected to the circuits, so no external connections are required for operation.

Audio Frequency (AF) Signal generator (68M):

Sine wave signal of 200Hz is generated to use as a modulating (message or information) signal to be transmitted. This is an Op-Amp based Wein bridge Oscillators using IC TL084. IC TL084 is a FET input general purpose Operational Amplifier. Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

Clock generator/Timing circuit (68M & 68D):

A TTL compatible clock signal of 64 KHz and 4KHz frequency are provided on board to use as a clock to the various circuits in the system. This circuit is a astable multivibrator using 555 timer followed by a buffer and frequency dividers

DC source (68M):

A 0 to +5V variable DC voltage is provided on board to use as a modulating signal instead of AF signal. This is useful to study step by operation of PCM modulation and demodulation. This is a simple circuit consisting of potentiometer and fixed power supply.

Low pass filters (68D):

This is a series of simple RC networks provided on board to smoothen the output of the D/A converter output (stair case signal). RC values are chosen such that the cutoff frequency would be at 200Hz

Amplifiers (68D):

This is an Op-amp (IC TL084) based non-inverting variable gain amplifiers provided on board to amplify the recovered message singles i.e. output of the Low pass filter to desired level. Amplitude control is provided in circuit to vary the gain of the amplifier between 0 and 3. AC/DC Switch facilitates to couple the input signal through capacitor or directly to the amplifier input.

Sample & Hold circuit (AET-68M):

This block (circuit) is a combination of buffer, level shifting network and sample & hold network. Op- amp IC TL084 is connected as buffer followed by non-inverting summer circuit. One of the inputs of summer is connected a voltage divider network and other being drawn as input. A dedicated sample& hold integrated circuit LF 398 is used as an active component followed by buffer. The LF198/LF298/LF398 is monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of 10^{10}(Ohm) allows high source impedance to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μf hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Logic inputs on the LF198 are fully differential with low current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from +5V to +18V supplies.

8 Bit A/D Converter (AET-68M):

This has been constructed with a popular 8 bit successive approximation A/D Converter IC ADC0808. The ADC0808, data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals. A dedicated 1MHz clock generator is provided in side this block. For complete specifications and operating conditions please refer the data sheet of ADC0808.

8 Bit Parallel-Serial Shift register (AET-68M):

A dedicated parallel in serial out shift register integrated circuit is used followed by a latch The SN74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. For complete specifications and operating conditions please refer the data sheet of SN74LS166.

8 Bit Serial-Parallel Shift register (AET-68D):

A dedicated serial in parallel out shift register integrated circuit is used followed by a latch. The SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features as asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all TTL products. For complete specifications and operating conditions please refer the data sheet of SN74LS164.

8 Bit D/A Converter (AET-68D):

This has been constructed with a popular 8 bit D/A converter IC DAC 0808. The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150ns while dissipating only 33mW with +5V supplies No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically +1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than +0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4μA provides 8-bit zero accuracy for I_{REF} >= 2mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. For complete specifications and operating conditions please refer the data sheet of DAC0808.

PCM Operation:

Figure 2.1 shows the block diagram of the PCM system. The modulating signal is applied to sample & hold circuit. This applied signal will be super imposed by +2.5V DC so that the negative portion the modulating signal will clamped to positive, this process is needed, because input of the A/D Converter should be between 0 and +5V. After level shifting is done the signal will be passed to sample & hold circuit. Sample & hold circuit will sample the input signal during on period of the clock signal and will hold the sampled output till next pulse comes. Sampling rate is 4KHz in this system.

So input of the A/D Converter is a stable voltage of certain level in between 0 and +5V. A/D converter (encoder) will give a predetermined 8 bit code for the sampled input. This entire conversion process will be made at a fast rate as ADC0808 is operating at high frequency clock i.e. 1MHz.

Coded output of the A/D converter is applied to input of the parallel in serial out register through a latch (741s373). This shift register is operating at 64KHz (sampling

frequency is 4KHz, so to shift 8 bits from parallel to serial we need 64KHz). This output (PCM) is transmitted through a co-axial cable which represents a communication channel. PCM signal from modulator (encoder) is applied to serial to parallel register. This shift register is also operating at 64KHz clock at which parallel to serial shift register is operating at PCM modulator (these both the clock signals should be in synchronized with each other in order to get proper decoded output). So the output of the serial to parallel register is a 8 bit code. This 8 bit code is applied to 8 bit D/A converter. Output of the D/A converter will be a staircase signaling between 0 and +5V. This stair case signal is applied a low pass filter. This low pass will smoothen the staircase signal so that we will get a recovered AF signal. We can use a voltage amplifier at the output of the low pass filter to amplify the recovered AF signal to desired voltage level.

2.5 PRE LAB QUESTIONS

1. State sampling theorem.
2. What is aliasing?
3. Give the expression for aliasing error and the bound for aliasing error.
4. What is quantization?
5. What are the various steps involved in A/D conversion.
6. Define step size.
7. What is the importance of regenerative repeater?
8. List out the three basic functions of regenerative repeater.
9. What is companding?
10. Write the mean square quantization error if the step size is S.
11. What is a mid tread quantizer?
12. What is a mid rise quantizer?

2.6 TEST PROCEDURE

1. Connect the modulator trainer to the mains and switch on the power supply.
2. Observe the output of the AF generator using CRO, it should be a sine wave of 200Hz frequency with 3Vpp amplitude.
3. Verify the output of the DC source with multimeter/scope, output should vary from 0 to +5V.
4. Observe the output of the clock generator using CRO, they should be 64KHz and 4KHz frequency of square wave with 5Vpp amplitude.
5. The clock signals are internally connected the circuit so no external connections are required.

6. Connect the demodulator trainer to the mains and switch on the power supply.
7. Observe the output of the clock generator using CRO, it should be 64KHz square wave with 5Vpp amplitude.

2.6.1 PCM Operation (with DC input):

Modulation:

8. Set DC source to some value say 4.4V with the help of multimeter and connect it to the A/D converter input and observe the output LED's
9. Note down the digital code i.e. output of the A/D converter and compare with the theoretical value.

   Theoretical value can be obtained by: $\frac{A/D\ Input\ voltage}{1\ LSB\ Value} = X_{(10)} = Y_{(2)}$

   Where

   1 LSB Value = $V_{ref}/2^n$

   Since V_{ref} = 5 V and n=8

   1 LSB Value = 0.01953

   Example:

   A/D Input voltage = 4.4 V

   = $225.28_{(10)1}$

   = $1110\ 0001_{(2)}$

   So digital output is 1110 0001

10. Keep CRO in dual mode. Connect one channel to 4KHz signal (one which is connected to the Shift register) and another channel to the PCM output.
11. Observe the PCM output with respect to 4 Khz signal and sketch the waveforms. Compare them with the given waveforms

    Note: From this waveform you can observe the LSB bit enters the output first.

Demodulation

12. Connect PCM signal to the demodulators(S-P shift register) from the PCM modulator (AET-68M) with the help of coaxial cable.
13. Connect clock signal (64KHz) from the transmitter (AET-68M) to the receiver (AET-68D) using co axial cable.
14. Connect transmitter clock to the timing circuit.
15. Observe and note down the S-P shift register output data and compare it with transmitted data(i.e. output A/D converter at transmitter).You will notice that the output of the S-P shift register is following the A/D converter output in the modulator.

16. Observe D/A converter output (Demodulated output) using multimeter /scope and compare it with the original signal and you can observe that there is no loss in information in process of conversion and transmission.

Sample work sheet:

1.	Modulating signal	:	4.4 V
2.	A/D Output (theoretical)	:	$1110\ 0001_{(2)}$
3.	A/D Output (practical)	:	$1110\ 0001_{(2)}$
4.	S-P Output	:	$1110\ 0001_{(2)}$
5.	D/A Converter output (Demodulated output)	:	4.4 V

2.6.2 PCM Operation (with AC input):

Modulation:

17. Connect AC signal of 2Vpp amplitude to Sample & Hold circuit.
18. Keep the CRO in dual mode. Connect one channel to the AF signal and another channel to the Sample & Hold output. Observe and sketch the sample & hold output.
19. Connect the Sample and Hold output to the A/D converter and observe the PCM output using Storage oscilloscope.
20. Observe PCM output by varying AF signal voltage.

Demodulation:

21. Connect PCM signal to the demodulator input (AET-68D) (S-P shift register) from the PCM modulator (AET- 68M) with the help of coaxial cable (supplied with the trainer).
22. Connect clock signal (64 KHz) from the transmitter (AET-68M) to the receiver (AET-68D) using coaxial cable.
23. Connect transmitter clock to the timing circuit.
24. Keep CRO in dual mode. Connect CH1 input to the sample and hold output (AET-68M) and CH2 input to the D/A converter output (AET-68D)
25. Observe and sketch the D/A output.
26. Connect D/A output to the LPF input.
27. Observe the output of the LPF/Amplifier and compare it with the original modulating signal (AET-68M).
28. From above observation you can verify that there is no loss in information (modulating signal) in conversion and transmission process.
29. Disconnect clock from transmitter (AET-68M) and connect to local oscillator (i.e., Clock generator output from AET-68D) with remaining setup as it is.

30. Observe D/A output and compare it with the previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

Note: You can take modulating signals from external sources. Maximum amplitude should not exceed 4V incase of DC and 3 Vpp incase AC (AF) signals.

2.7 MODEL GRAPH:

i) With AC Input

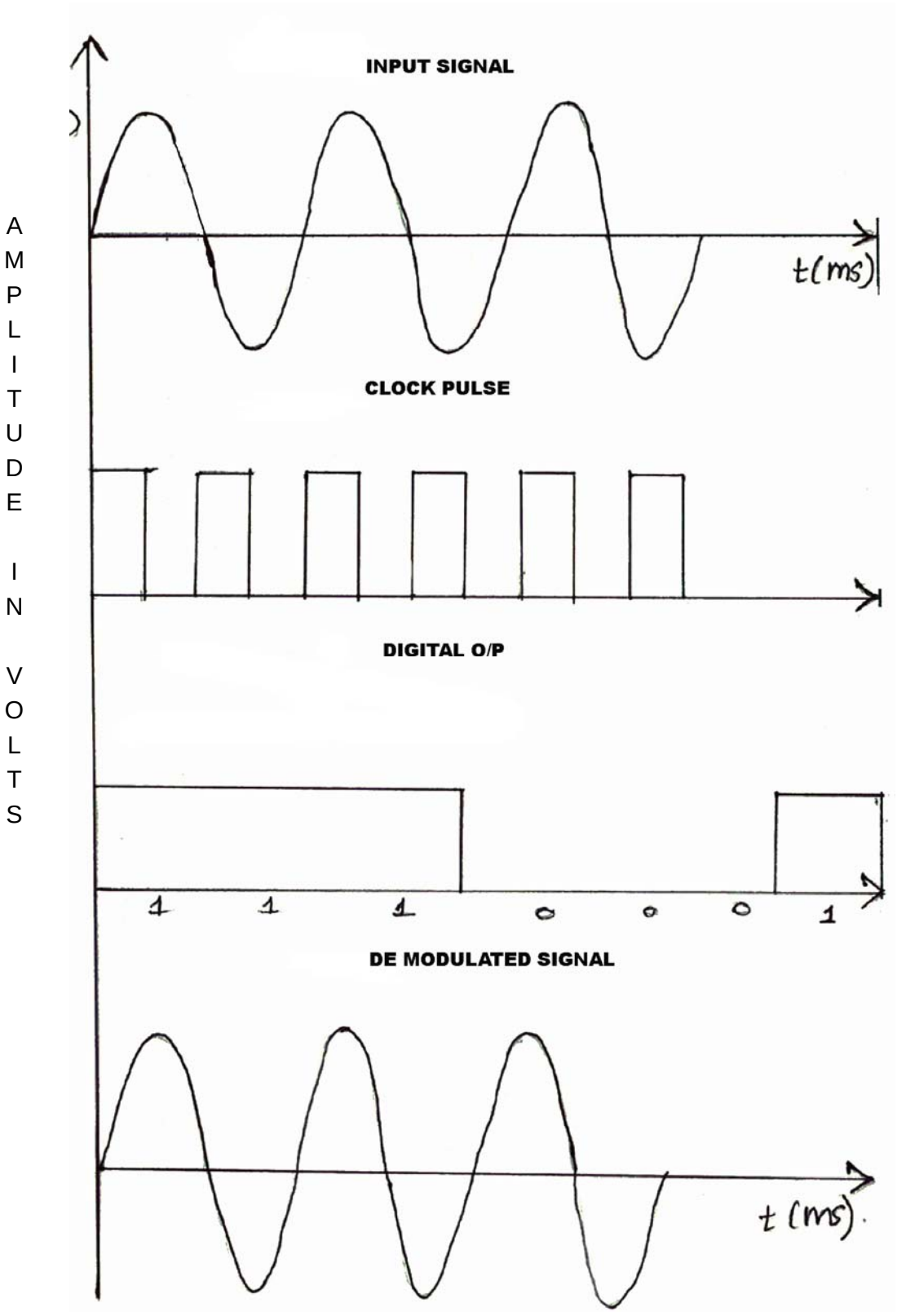


Fig 2.2 PCM Waveform with AC input

ii)With DC Input

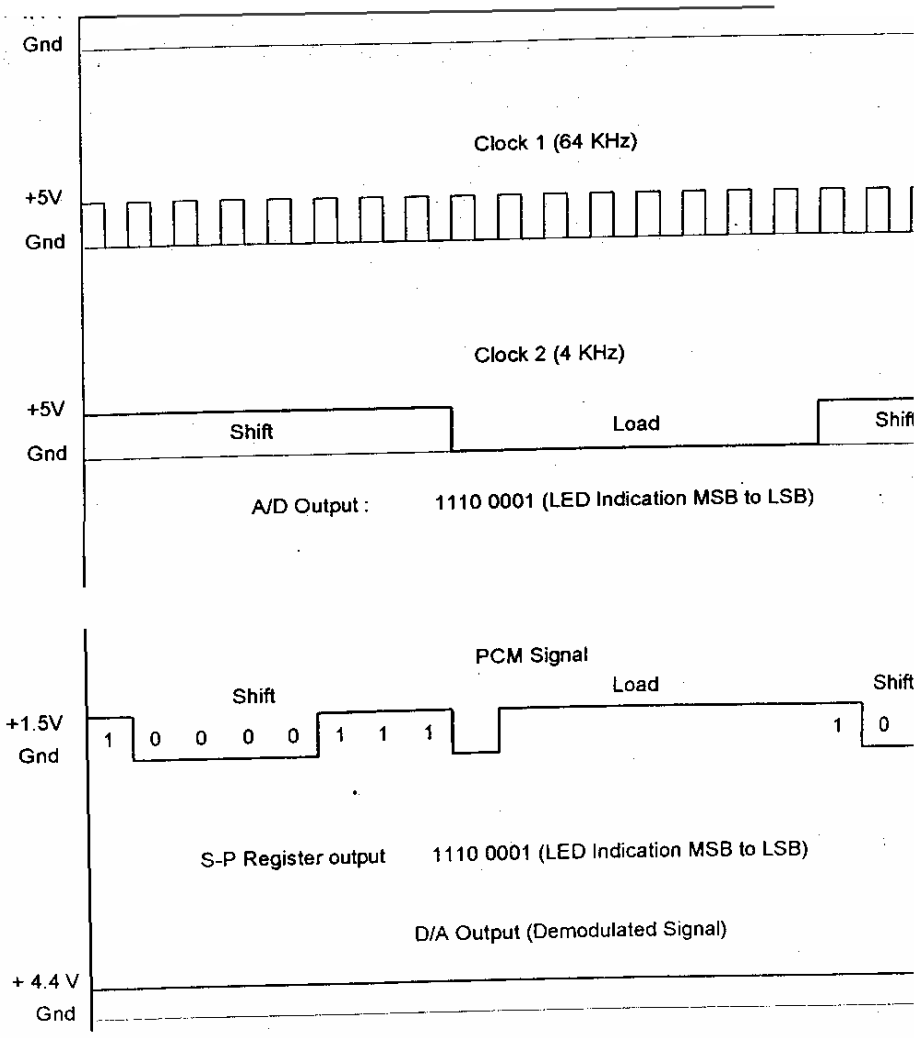


Fig 2.3 PCM Waveforms/Timing diagram(DC Input)

2.8 OBSERVATION

PCM Modulation (With AC input)

	Amplitude	Time Period
AC input		
Sample and hold signal		
Clock signal(4 KHz)		
Clock signal(64 KHz)		
PCM Output		

PCM Demodulation (with AC input)

	Amplitude	Time Period
D/A Converter output Signal		
LPF output signal		
Demodulated output		

PCM Modulation (With DC input)

	Amplitude	Time Period
DC input		
Clock signal(4 KHz)		
Clock signal(64 KHz)		
PCM Output		

PCM Demodulation (With DC input)

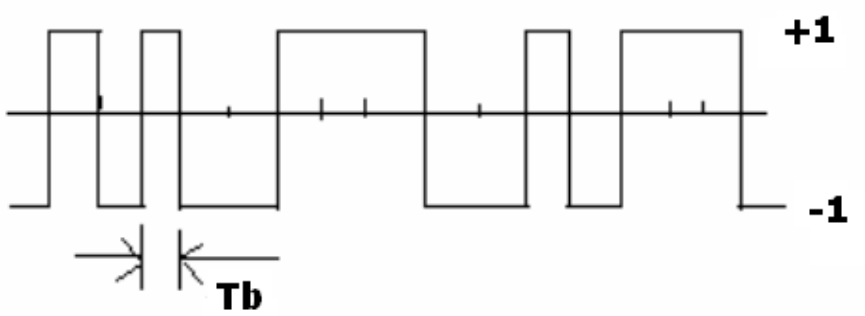
	Amplitude	Time Period
D/A Converter output Signal		
LPF output signal		
Demodulated Output		

2.9 LAB RESULT

Thus the Pulse Code modulation and demodulation were performed and graphs were plotted.

2.10 POST LAB QUESTIONS

1. What do you mean by quantizing process?
2. What will happen when sampling rate is greater than Nyquist rate ?
3. What will happen when sampling rate is less than Nyquist rate ?
4. Find the A/D Converter output for input DC voltage of 3.6V.
5. Fig shown below shows a PCM wave in which the amplitude levels of +1 volt and -1 volt are used to represent binary symbols 1 and 0 respectively. The code word used consists of three bits. Find the sampled version of an analog signal from which this PCM wave is derived.



6. In digital telephony,

(a)What kind of modulation is used?

(b)Give the typical sampling rate, output data rate and speech signal Bandwidth.

7.Mention some applications of PCM.

8. What is the function of Sample and Hold circuit?

3. DIFFERENTIAL PULSE CODE MODULATION AND DEMODULATION

3.1 OBJECTIVE

To analyze a DPCM system and to interpret the modulated and demodulated waveforms for a sampling frequency of 8 KHz.

3.2 HARDWARE REQUIRED

1. ADCL-07 Kit
2. 20MHz Dual Trace Oscilloscope
3. Connecting chords
4. Power supply

NOTE: KEEP THE SWITCH FAULTS IN OFF POSITION

3.3 INTRODUCTION

Pulse Code Modulation (PCM) is different from Amplitude Modulation (AM) and Frequency Modulation (FM) because, those tow are continuous forms of modulation. PCM is used to convert analog signals into binary form. In absence of noise and distortion it is possible to completely recover a continuous analog modulated signals. But in real time they suffer from transmission distortion and noise to an appreciable extent. In the PCM systems, groups of pulses or codes are transmitted which represent binary numbers corresponding to modulating signal voltage levels. Recovery of transmitter information does not depend on the height, width or energy content of the individual pulses, but only in their presence or absence. Regeneration of the pulse is easy, resulting in the system that produces excellent result for long distance communication.

Differential PCM is quite similar to ordinary PCM. Each word in this system indicates the difference in amplitude, positive or negative, between this sample and the previous sample. Thus the relative value of each sample is indicated rather than, the absolute value in normal PCM.

This unique system consists of :

3.3.1. DPCM Modulator

1. Regulated Power Supply
2. AF Signal generator
3. Prediction Filter
4. Sample & Hold Circuit
5. A / D Converter
6. Parallel – Serial Shift generator

7. Clock generator / Timing Circuit
8. DC Source

3.3.2 DPCM Demodulator

1. Regulated Power Supply
2. Serial - Parallel Shift generator
3. D / A Converter
4. Clock generator
5. Timing Circuit
6. Prediction Filter
7. Passive Low Pass Filter

3.4. BLOCK DIAGRAM / CIRCUIT DESCRIPTION

Regulated Power Supply :

This consists of a bridge rectifier followed by capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of $\pm$ 5V and +12V @ 300mA. Each on the on-board circuits. These supplies have been internally connected to the circuits, so no external connections are required for operation.

Audio Frequency Signal Generator :

Sine wave signal of 400HZ is generated to use as a modulating signal to be transmitted. This is an Op-Amp based Wein Bridge Oscillators using IC TL084, which is a FET input general purpose operational amplifier. Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

Clock Generator / Timing Circuit :

A TTL compatible clock signal of 64KHz and 8KHz frequencies are provided on-board to use as a clock to the various circuits in the system. This circuit is Astable multivibrator using 555 timer followed by a buffer and frequency divider

DC Source :

A 0 to 290mV variable DC voltage is provided on board to use as a modulating signal instead of AF signal. This is useful to study step by operation of DPCM modulation and demodulation. This is a simple circuit consists of potentiometer and fixed power supply.

Low Pass Filter :

This is a series of simple RC networks provided on board to smoothen the output of the D/A converter output. RC values are chosen such that the cutoff frequency would be at 400Hz.

Sample & Hold Circuit :

This block is a combination of buffer, level shifting network and sample & hold network. Op-amp is connected as buffer followed by non-inverting summer circuit. One of the inputs of summer is connected a voltage divider network and other being drawn as input. A dedicated sample & hold integrated circuit LF 398 is used as an active component followed by a buffer. LF398 is a monolithic sample and hold circuits, which utilize BI – FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF398to be included inside the feedback loop of 1MHz op-amps without having stability problems. Input impedance of 10^{10} ohm. Allows high source impedances to be used without degrading accuracy. P-channel junction FET's are combined with bipolar devices in the output amplifier to give a droop rates as low as 5mV / min with 1μF hold capacitor. The JFETS have much lower noise than MOS devices used in previous design and do not exhibit high temperature instabilities. The overall design guarantees no feed through from input to output in the hold mode, even for input signals equal to the supply voltages. Logic inputs on the LF198 are fully differential with low input current, allowing direct connections to TTL, PMOS and CMOS. Differential threshold is 1.4V. The LF 198 will operate from $\pm$5V to $\pm$18V supplies.

A/D Converter :

This has been constructed with a popular 8-bit successive approximations A/D converter IC ADC0808, data acquisition component is a monolithic CMOS device with an 8-bit A-D Converter, 8 – channel multiplexer and microprocessor compatible control logic. The 8-bit ADC uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator., 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any 8-single-ended analog signals.

Parallel-Serial Shift Register

A dedicated parallel in serial out shift register integrated circuit is used followed by a latch. The SN74LS166 is an 8-bit Shift register. Designed with all inputs buffers, the drive requirements are lowered to one 74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified. The LS166 is a parallel in or serial out shift register, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding cleat input. The shift / load input establishes the parallel – in or serial-in mode. When high, this input enables the serial data input and couples the eight flip flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit funation. Clocking is inhibited when either of the clock inputs is held high; holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A Change from low- to high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs. Including the clock, and sets all flip-flops to zero. For complete specifications and operating conditions please refer the data sheet of SN74LS166

Serial-Parallel Shift Register :

A dedicate serial in parallel out shift register integrated circuit is used followed by a latch. The SN74LS164 is a high speed 8 Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset, which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all TTL products. For complete specifications and operating conditions please refer the data sheet of SN74LS164.

D/A converter :

This has been constructed with a popular 8 –bit D/A Converter IC DAC 0808. The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33m W with ±5V supplies.

BLOCK DIAGRAM

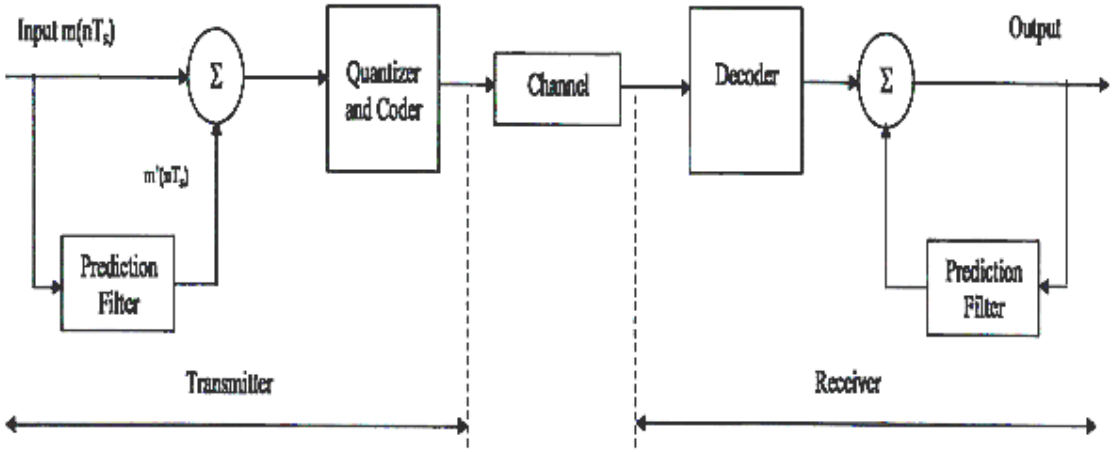


Fig 3.1 Block diagram of DPCM System

Reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/ 256. Relative level output current of less than 4μA provides 8-bit zero accuracy for I_{REF} >=2mA. The power supply current of the DAC0808 is independent of bit codes and exhibits essentially constant device characteristics over the entire supply voltage range. For complete specifications and operating conditions please refer the data sheet of DAC0808.

DPCM Operation:

The modulating signal is applied to positive terminal of the summer circuit and the output pf the prediction filter is connected to negative terminal of the summer circuit. The output of the summer circuit is connected to the sample & hold circuit. Sample & hold circuit will sample the input signal during ON period of the clock signal and will hold the sampled output till next pulse comes. Sampling rate is 8KHz in this system.

So input of the A/D converter is stable voltage of certain level in between 0 and + 280mV. A/D converter will give a predetermined 4-bit code for the sampled input. This entire conversion process will be made at a fast rate as ADC 0808 is operating at high frequency clock.

Coded output of the ADC is applied to input of the parallel in serial out register through a latch (74LS373). This shift register is operating at 64KHZ. This output is transmitted through a coaxial cable, which represent a communication channel.

DPCM signal from modulator is applied to serial to parallel register. This shift register is also operating at 64KHz clock to which parallel to serial shift register is

operating at DPCM modulator. So the output of the serial to parallel register is a 4-bit code.

This 4-bit code is applied to D/A converter. Output of the DAC will be a staircase signal lying between 0 and +280mV. This stair case signal is applied a low pass filter. This low pass will smoothen the stair case signal so that we will get a recovered AF signal.

3.5. PRELAB QUESTIONS:

1. Compare DPCM and PCM.
2. What is the significance of predictor in DPCM?
3. How is a predictor constructed?
4. What is prediction error?
5. What is the significance of accumulator in DPCM?
6. Why DPCM is used for speech compression?

3.6. TEST PROCEDURE

DPCM modulation:

1. Refer to the block diagram and carry out the following Connections and switch settings.
2. Connect power supply in proper polarity to the kit ADCL-07 and switch it ON.
3. Keep the clock frequency at 512 KHz by changing the jumper position of JP1 in the clock generator section
4. Keep the amplitude of the onboard sine wave, of frequency 500Hz to 1Vpp DPCM modulation.
5. Connect the 500Hz sine wave to the lN post of Analog Buffer.
6. Connect OUT post of Analog Buffert o lN post of DPCM modulator section.
7. Observe the sample output at the given test point the input signal is sampled at the clock frequency of 16KHz.
8. Observe the linear predictor output at the PREDICTED OUT post of the Linear predictor in the DPCM modulator section.
9. Observe the differential pulse code modulate data(DPCM) at the DPCM OUT post of the DPCM modulator section.
10. Observe the DPCM data at DPCM OUT post by varying input signal from to 2V.

DPCM demodulation:

1. Connect the DPCM modulated data from the DPCM OUT post of the DPCM Modulator to the lN post of the DPCM demodulator.

2. Observe the demodulated data at the output of summation block.
3. Observe the integrated demodulated data at the DEMOD OUT post of the DPCM demodulator.
4. Connect the demodulated data from the DEMOD OUT post of the DPCM demodulator to the lN post of the low-pass filter.
5. Observe the reconstructed signal at the OUT post of the filter.Use RST switch for clear observation of output.
6. Now, simultaneously reduce the clock frequencies f rom 512KHz to 256KHz,128KHz and 64KHz by changing the jumper position of JP1 and observe the difference in the DPCM modulated and demodulated data.As the frequency of clock decreases DPCM demodulated data at DEMOD OUT becomes distorted.
7. Observe various waveform as mentioned below

3.7. MODEL GRAPH

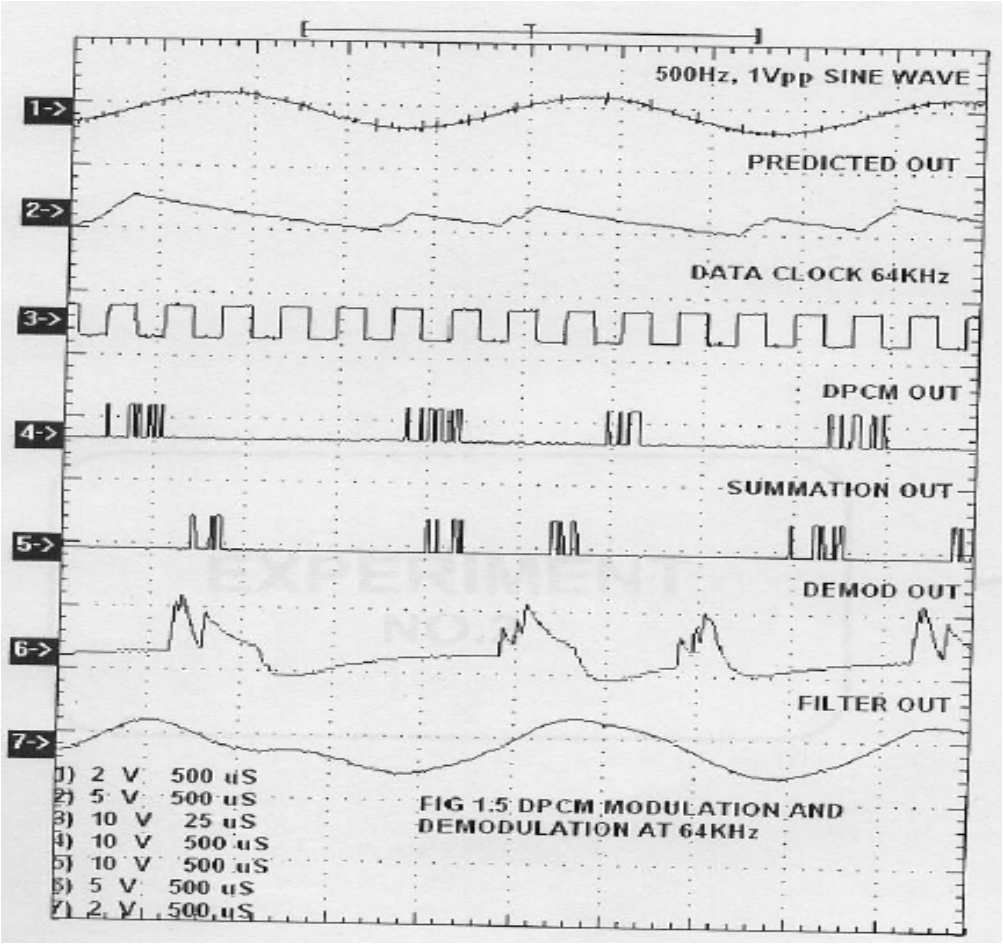


Fig.3.2 DPCM OPERATION (with AC input) MODULATION & DEMODULATION

3.8. Observation:

ON KIT ADCL-07

Observe the following waveforms on the oscilloscope and plot on the paper.

1. 500Hz ,lV pp input sine wave.
2. Sampled out at the provided test point SAMPLER OUT
3. Linear predictor out at PREDICTED OUT post.
4. DPCM data at DPCM OUT post
5. Line interface out at the given output test point of line interface block in DPCM Demodulator
6. Demodulated DPCM data at the output test point of summation block in DPCM demodulator.
7. Integrated demodulated data at the DEMOD OUT post of the DPCM demodulator
8. Reconstructed sine wave at the OUT post of the filter
9. Observe the data at different clock rates.

DPCM Operation - with AC input

Modulation		
	Amplitude	**Time Period**
AC Input		
Prediction Filter Output		
Sample and Hold Output		
Clock – 1 Output		
DPCM Output		

Demodulation		
	Amplitude	**Time Period**
DPCM Input		
D/A Converter Output		
LPF Output		
Demodulated output Prediction Filter Output		

3.9. LAB RESULT

Thus the Differential Pulse code modulation and demodulation were performed.

3.10 POST LAB QUESTIONS:

1. For data compression say whether ADPCM or DPCM is better. Justify.
2. What is the need for compression?Mention the types of compression.
3. List the communication standards which use DPCM.
4. Based upon the knowledge that you have gained after doing the experiment write the functions of sample and hold circuit.
5. Name the circuit used to achieve synchronization between transmitter and receiver.

5. DELTA MODULATION AND DEMODULATION

4.1. OBJECTIVE

To analyze a Delta modulation system. and interpret the modulated and demodulated waveforms

4.2. HARDWARE REQUIRED

1. PCM Modulator trainer- AET-73M
2. PCM Demodulator trainer-AET-73D
3. Storage Oscilloscope
4. Digital Multimeter
5. Co-axial cables (standard accessories with AET-73 trainer)

4.3. INTRODUCTION

Delta Modulation is a form of pulse modulation where a sample value is represented as a single bit. This is almost similar to differential PCM, as the transmitted bit is only one per sample just to indicate whether the present sample is larger or smaller than the previous one. The encoding, decoding and quantizing process become extremely simple but this system cannot handle rapidly varying samples. This increases the quantizing noise.

The trainer is a self sustained and well organized kit for the demonstration of delta modulation & demodulation .The system consist of :

4.3.1. DM Modulator (AET-73M) trainer kit

1. Regulated power supply
2. Audio Frequency signal generator
3. Buffer/signal shaping network
4. Voltage comparator
5. 4 Bit UP/DOWN counter
6. Clock generator/Timing circuit
7. 4 Bit D/A converter
8. DC source

4.3.2. DM Demodulator (AET-73D) trainer kit

1. Regulated power supply
2. 4 Bit UP/DOWN counter
3. 4 Bit D/A converter
4. Clock generator
5. Passive low pass filter

6. Audio amplifier

Regulated power supply (73M & 73D):

This consists of a bridge rectifier followed by Capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of +-5V and +12V@ 300mA each to the on board circuits. These supplies have been internally connected to the circuits. so no external connections are required for operation.

Audio Frequency (AF) S signal generator (73M):

Sine wave signal of 100 Hz is generated to use as a modulating (message or information) signal to be transmitted. This is an Op-Amp based Wein bridge Oscillators using IC TL084 is a FET.input general purpose Operational Amplifier .Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

Clock generator/Timing circuit (73M & 73D):

A TTL compatible clock signal of 4 KHz frequency is provided on board to use as a clock to the various circuits in the system. This circuit is a astable multivibrator using 555 timer followed by a buffer.

DC Source (73M):

A 0 to +5V variable DC voltage is provided on board to use as a modulating signal instead of AF Signal. is useful to study step by step operation of Delta modulation and Demodulation. This is a simple circuit consists of potentiometer and fixed power supply.

Buffer/Signal shaping circuit (73M):

A non inverting buffer using IC TL 084 is provided at the input of the DM modulator followed by a level shifting network. Buffer provides the isolation between DM circuit and the signal source. Signal Shaping super imposes the 1.5V DC on incoming modulating signal so that the input of the comparator lies between 0 and +3V maximum.

4.4.BLOCK DIAGRAM

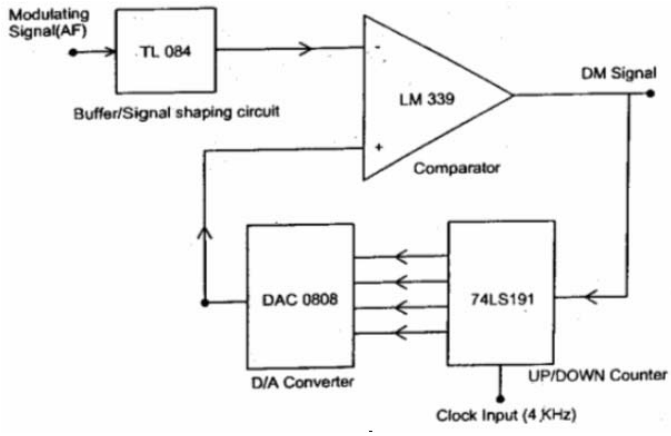


Fig.4.1. DM Modulator

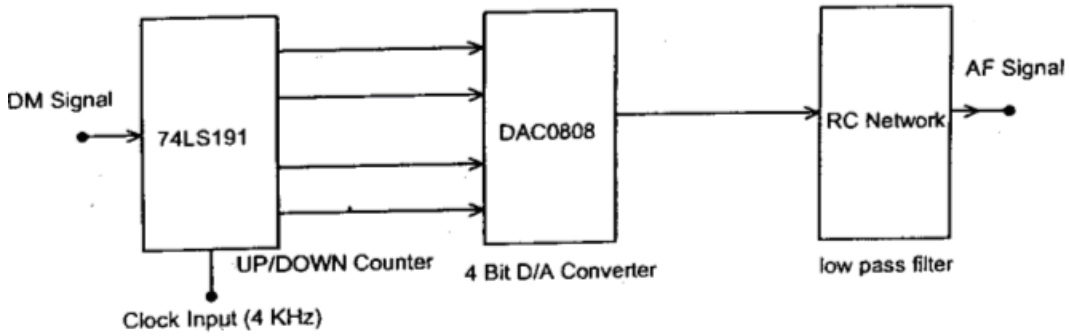


Fig.4.2. DM Demodulator

Voltage comparator (73D):

This circuit is build with IC LM339 The LM339 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2mV for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages .Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the common mode voltage range includes ground, even though operated from a single power supply voltage. Application areas include limit comparators simple analog to digital converters: pulse, square and time delay generators. wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates .The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power

supplies, they will directly interface with MOS logic where the low power drain of the LM339 is a distinct advantage over standard comparators .For circuit connections and other operating conditions.

Low pass filters (73D):

This is a series of simple RC networks provided on board to smoothen the output of the D/A converter output. RC values are chosen such that the cutoff frequency would be at 100 Hz.

Amplifiers (73D):

This is an Op-amp (IC TL084) based non-inverting variable gain amplifiers provided on board to amplify the recovered message singles i.e. output of low pass filter to desired level. Amplitude control is provided in circuit to vary the gain of the amplifier between 0 and 6.AC/DC Switch facilitates to couple the input signal through capacitor to directly to the amplifier input.

4 Bit UP/DOWN Counter (73M & 73 D):

This circuit is made using Synchronous 4-Bit Up/Down Counter with Mode Control IC 74LS191 .The DM 74LS191 circuit is a synchronous, reversible, counter. Synchronous operation is provided by having all flip-flops clocked simultaneously. so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with the asynchronous counters. The outputs of the four master slave flip flops are triggered on a LOW to HIGH level transition of the clock input. if the enable input is LOW a HIGH at the enable input inhibits counting .Level changes at either the enable input or the down/up input should be made only when the clock input is HIGH. The direction of the count is determined by the level of the down/up input. When LOW the counter counts up and when HIGH it counts down. The counter is fully programmable that is the outputs may be preset to either level by placing a LOW on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down/up and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers required for parallel words. The ripple clock input produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock

input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high speed operation.

4 Bit D/A converter (AET-73M & 73D):

This has been constructed with a popular 8 bit D/A Converter IC DAC 0808.The DAC0808 is an 8-bit monolithic DAC featuring a full scale output current settling time of 150 Ns while dissipating only 33 maw with +-5V supplies. No reference current ($I_{REF)}$ trimming is required for most applications since the full scale output current is typically +- 1 LSB of 255 $I_{REF}/256$ .Relative accuracies of better than +- 0.19 % assure 8 bit monotonic and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for I_{REF} [greater than or equal] 2 math power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.4 LSB Bits are permanently grounded to make 4 bit converter. For complete specifications and operating conditions please refer the data sheet of DAC0808.

DM Operation:

Figure 4.1 shows the basic block diagram of the PCM system. The modulating signal is applied to buffer /signal shaping network. This applied signal will be superimposed by +1.5V DC so that the negative portion the modulating signal will clamped to positive ,this process is needed ,because input of the comparator should be between 0 and +3V.

After level shifting is done the signal will be passed to inverting input of the comparator. on inverting input of the comparator is connected to output of the 4 Bit D/A converter. Comparator is operating at +5V single supply .So output of the comparator will be high (i.e. +vet V_{ast}) when modulating signal is less than the reference signal i.e. D/A output, otherwise it will be 0V. And this signal is transmitted as DM signal .same signal is also connected as UP/DOWN control to the UP/DOWN counter (74LS 191).

UP/DOWN counter is programmed for 0000 starting count. So initially output of the counter is at 0000 and the D/A converter will be at 0V .Comparator compares the modulating signal is greater than the reference signal. For next clock pulse depending on the UP/DOWN input counter will count up or down. If the UP/DOWN input is low (nothing but comparator output).

Counter will make up and output will be 0001. So the D/A converter will convert this 0001 digital input to equivalent analog signal(i.e. 0.3V 1 LSB Value).Now the reference signal is 0.3V.If still modulating signal is greater than the D/A output again

comparator output(DM) will be low and UP count will occur. If not DOWN Count will take place. This process will continue till the reference signal and modulating signal voltages are equal. So DM signal is a series of 1 and 0.

DM signal is applied to a UP/DOWN input of the UP/DOWN counter at the receiver. This UP/DOWN counter is programmed for 1001 initial value (i.e. power on reset) and mode control is activated. So depend on the UP/DOWN input for the next clock pulse counter will count UP or DOWN. This output is applied to 4 Bit D/A converter. A logic circuit is added to the counter which keeps the output of the counter in between 0000 to 1111 always. Output of the D/A converter will be a staircase signal lies between 0 and +4.7V.This staircase signal is applied a low pass filter .This low pass will smoothen the staircase signal so that original AF signal will be recovered.

We can use a voltage amplifier at the output of the low pass filter to amplify the recovered AF signal to desired voltage level.

4.5. PRELAB QUESTIONS

1. What are two types of quantization errors?
2. What is granular noise?
3. What is slope overload distortion ?
4. What happens to the output signal if the variation of the message signal is
   (i)greater than the step size (ii) less than the step size
5. What is the advantage of delta modulation over PCM?

4.6. TEST PROCEDURE:

DM Modulator:

1. Study the theory of operation
2. Connect the trainer (AET-73M) -
3. Observe the output of AF generator using CRO; it should be a Sine wave of 100 Hz frequency with 3Vpp amplitude.
4. Verify the output of the DC source with multimeter/scope; output should vary 0 to +4V
5. Observe the output of the clock generator using Crotchety should be 4 KHz frequency of square wave with 5 Up amplitude.

   Note: This clock signal is internally connected to the up/down counter so no external connection is required.

DM With DC Voltage as modulating signal:

6. Connect DC signal from the DC source to the inverting input of the comparator and set some voltage says 3V.
7. Observe and plot the signals at D/A converter output (i.e. non-inverting input of the comparator), DM signal using CRO and compare them with the waveforms given in figure.
8. Connect DM signal (from 73M) to the DM input of the demodulator.
9. Connect clock (4KHz) from modulator (73M) to the clock input of the demodulator (73D). Connect clock input of UP/DOWN counter (in 73D) to the clock from transmitter with the help of springs provided.
10. Observe digital output (LED indication) of the UP/DOWN counter (in 73 D) and compare it with the output of the UP/DOWN (in 73M) .By this you can notice that the both the outputs are same.
11. Observe and plot the output of the D/A converter and compare it with the waveforms given in figure.
12. Measure the demodulated signal (i.e. output of the D/A converter 73D with the help of multimeter and compare it with the original signal 73 M. From the above observation you can notice that both the voltages are equal and there is no loss in process of modulation, transmission and demodulation.
13. Similarly you can verify the DM operation for different values of modulating signal.

DM With AF Voltage as modulating signal:

14. Connect AF signal from the AF source to the inverting input of the comparator and set ome voltage says 3V.
15. Observe and plot the signals at D/A converter output (i.e. non-inverting input of the comparator), DM signal using CRO and compare them with the waveforms given in figure.
16. Connect DM signal (from 73M) to the DM input of the demodulator.
17. Connect clock (4KHz) from modulator (73M) to the clock input of the demodulator (73D).
18. Connect clock input of UP/DOWN counter (in 73D) to the clock from transmitter with the help of springs provided.
19. Observe and plot the output of the D/A converter and compare it with the waveforms given in figure.

20. Observe and sketch the D/A output.
21. Connect D/A output to the LPF input.
22. Observe the output of the LPF/Amplifier and compare it with the original modulating signal (AET-73M).
23. From the above observation you can verify that there is no loss in information in conversion and transmission process.
24. Disconnect clock from transmitter (AET-73M) and connect to local oscillator (i.e. clock generator output from AET-73D) with remaining setup as it is. Observe demodulated signal output and compare it with the previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

    Note: you can take modulating signals from external sources. Maximum amplitude should not exceed 4 V incase of DC and 3 Vpp incase of AC (AF) signals.

4.7.MODEL GRAPH

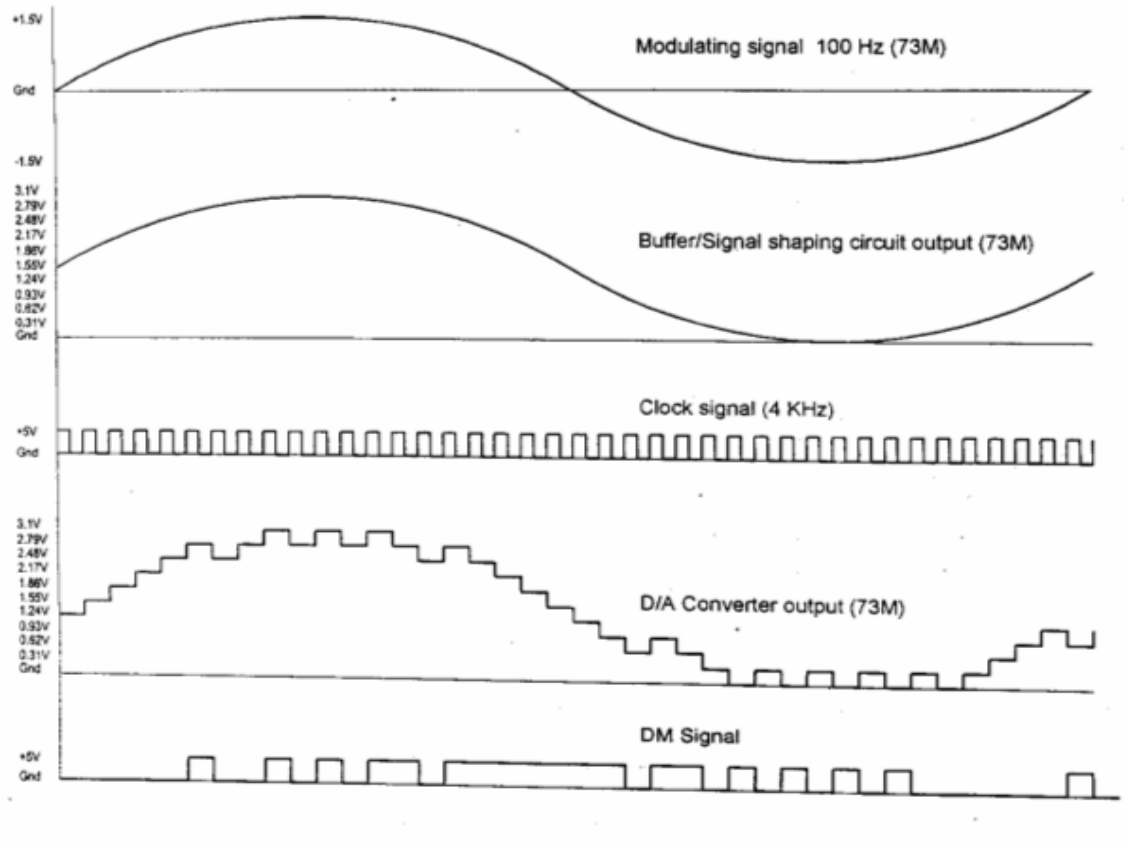


Fig 4.3 DM Waveforms for AC input signal

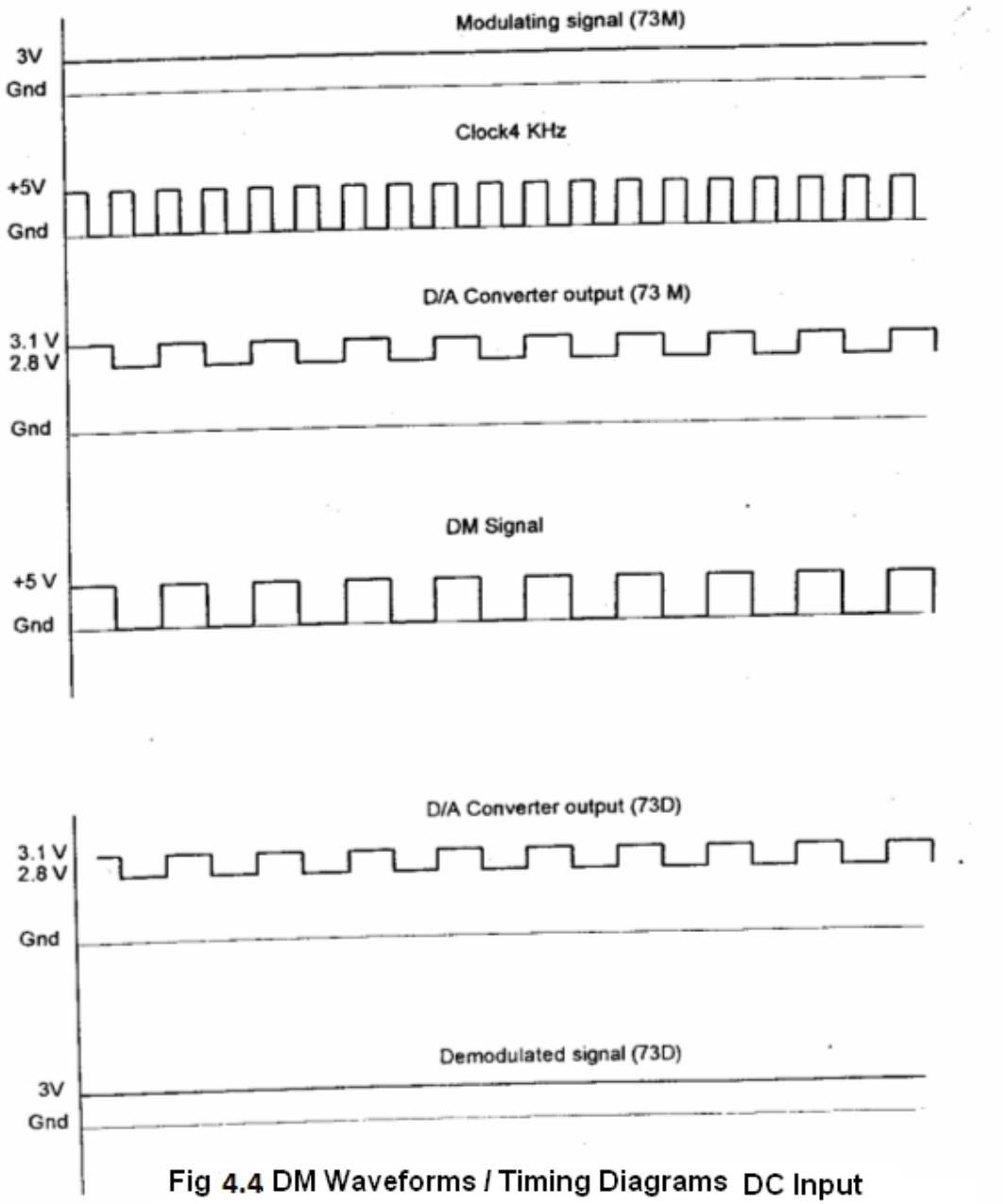


Fig 4.4 DM Waveforms / Timing Diagrams DC Input

4.8.OBSERVATION

DM Modulation (With AC input)

	Amplitude	Time Period
AC input		
D/A Converter Output		
Clock signal(4 KHz)		
DM Output		

DM Demodulation (with AC input)

	Amplitude	Time Period
DM input		
D/A Converter output Signal		
Demodulated Output		
Clock signal(4 KHz)		

DM Modulation (With DC input)

	Amplitude	Time Period
DC input		
D/A Converter Output		
Clock signal(4 KHz)		
DM Output		

DM Demodulation (With DC input)

	Amplitude	Time Period
DM input		
D/A Converter output Signal		
Demodulated Output		
Clock signal(4 KHz)		

4.9. LAB RESULT

Thus the Delta modulation and demodulation were performed and graphs were plotted.

4.10. POST LAB QUESTIONS:

1. Compare DPCM ,PCM& Delta modulation.
2. How to reduce the quantization noise that occurs in DM?
3. A band pass signal has a spectral range that extends from 20 to 82 KHz.Find the acceptable sampling frequency.
4. Find the fourier series expansion of an Impulse train.
5. Mention the applications of DM.

5. FSK MODULATION AND DEMODULATION

5.1 OBJECTIVE

To analyze a FSK modulation system. and interpret the modulated and demodulated waveforms

5.2 HARDWARE REQUIRED

1. FSK Trainer Kit - AET-48
2. Dual Trace oscilloscope
3. Digital Multimeter

5.3 INTRODUCTION

In Frequency shift keying, the carrier frequency is shifted (i.e. from one frequency to another) corresponding to the digital modulating signal. If the higher frequency is used to represent a data '1' & lower frequency a data '0', the resulting FSK waveform appears. Thus

Data =1 High Frequency

Data =0 Low Frequency

It is also represented as a sum of two ASK signals. The two carriers have different frequencies & the digital data is inverted. The demodulation of FSK can be carried out by a PLL. As known, the PLL tries to 'lock' the input frequency. It achieves this by generating corresponding O/P voltage to be fed to the VCO, if any frequency deviation at its I/P is encountered. Thus the PLL detector follows the frequency changes and generates proportional O/P voltage. The O/P voltage from PLL contains the carrier components. Therefore to remove this, the signal is passed through Low Pass Filter. The resulting wave is too rounded to be used for digital data processing. Also, the amplitude level may be very low due to channel attenuation.

5.3.1 FSK Modulator

Figure 5.1 shows the FSK modulator using IC XR 2206. IC XR 2206 is a VCO based monolithic function generator capable of producing Sine, Square, Triangle signals with AM and FM facility. In this trainer XR2206 is used generate FSK signal. Mark (Logic 1) and space (logic 0) frequencies can be independently adjusted by the choice of timing potentiometers FO & Fl. The output is phase continuous during transitions. The keying signal i.e. data signal is applied to pin 9.

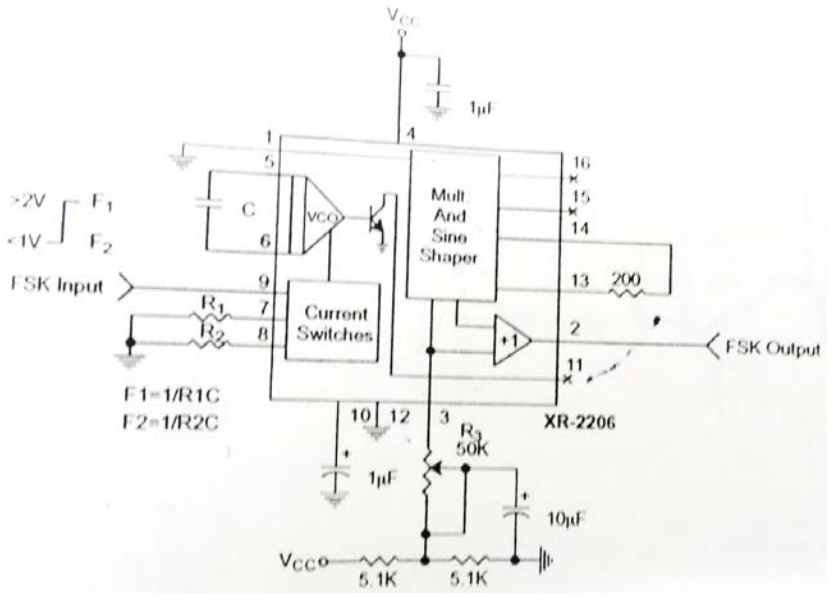
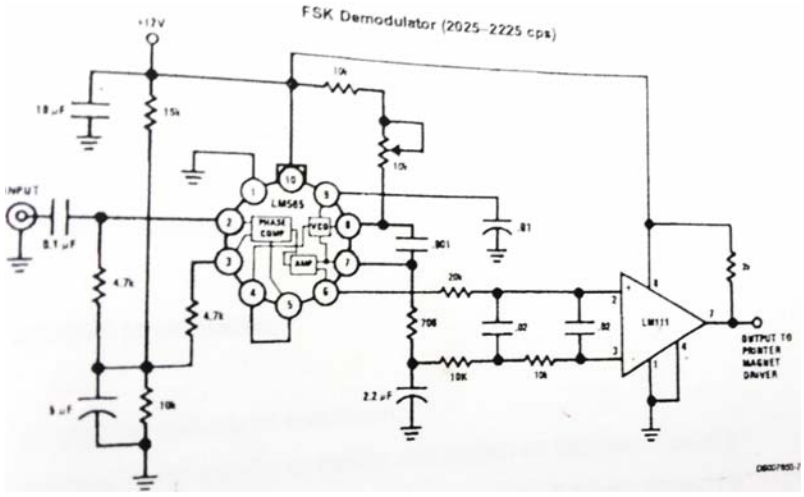


Figure 5.1

5.3.2 FSK Demodulator:

Figure 5.2 shows FSK demodulator in a combination of PLL (LM565) and comparator (Op-amp). The frequency-changing signal at the input to the PLL drives the phase detector to result in rapid change in the error voltage, which is applied to the input of the comparator. At the space frequency, the error voltage out of the phase detector is below the comparison voltage of the comparator. The comparator is a non-inverting circuit, so its output level is also low. As the phase detector input frequency shifts low (to the mark frequency), the error voltage steps to a high level, passing through the comparison level, causing the comparator output voltage to go high. This error voltage change will snap the comparator output voltage between its two output levels in manner that duplicates the data signal input to the XR22OS modulator.

The free running frequency of the PLL (no input signal) is set midway between the mark and space frequencies. A space at 2025 Hz and mark at 2225 Hz will have a free running VCO frequency of 2125 Hz.



5.4 FSK SYSTEM DIAGRAM

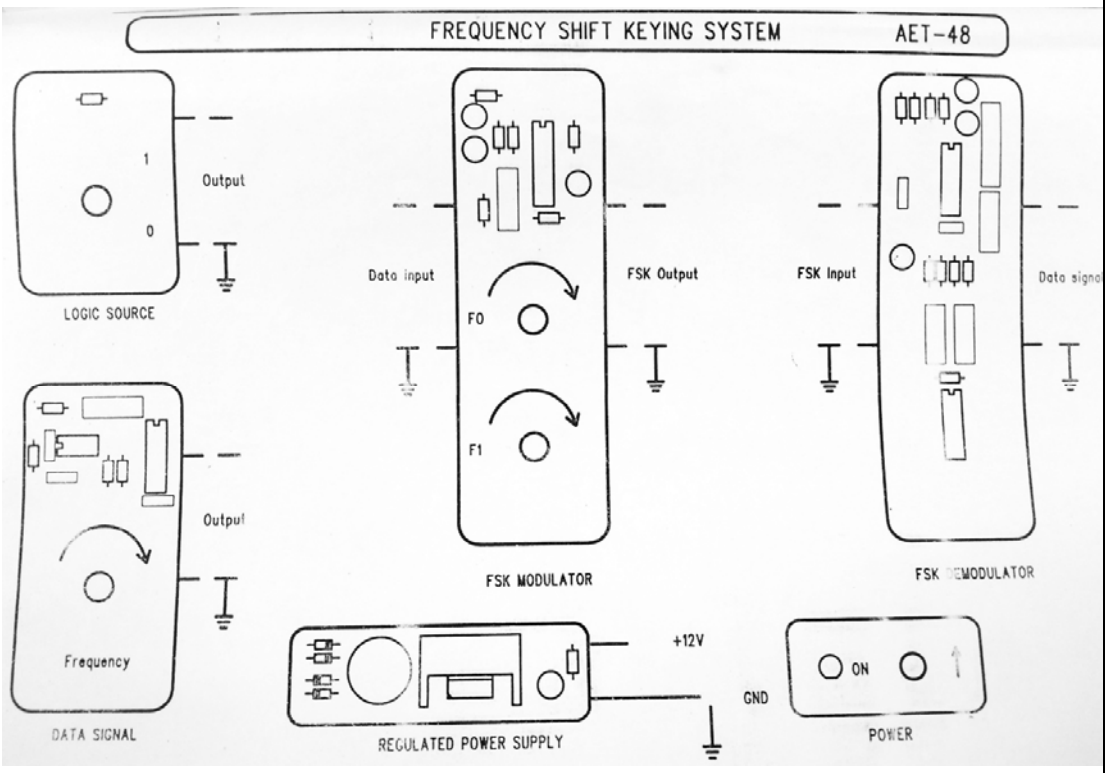


Figure 5.3

5.5 PRE LAB QUESTIONS

1. List some applications of FSK.
2. Define digital modulation schemes.
3. Identify the differences between Pass band and Base band Communication.
4. What is a matched filter?
5. What are the properties of matched filter?

5.6 TEST PROCEDURE

1. Connect the trainer kit to the mains and switch on the power supply
2. Check internal RPS voltage (it should be 12V) and logic source voltage for logic one (it should be 12V)
3. Observe the data signal using oscilloscope. Note down the value. (Amplitude and Time Period)
4. Connect the output of the logic source to data input of the FSK modulator

5. Set the output frequency of the FSK modulator as 1.2KHz using control F0 (this represents logic 0). Then set another frequency as 2.4KHz using control F1 (this represents logic 1) using multimeter.
6. Connect the data input of the FSK modulator to the output of the data signal generator. Observe the signal that comes out of FSK modulator and note down the readings.
7. Connect the FSK modulator output to the input of the FSK demodulator. Observe the waveform of FSK demodulator output using CRO and note down the readings.

5.7 OBSERVATION

Data source			**Carrier signal**		
Signal Type	**Time Period**	**Amplitude**	**Signal Name**	**Frequency**	**Amplitude**
Square wave			F1	2.4KHz	
			F0	1.2KHz	
Modulated Output			**Demodulated output**		
Signal Name	**Frequency**	**Amplitude**	**Signal Type**	**Time Period**	**Amplitude**
FSK	1.2KHz and 2.4KHz alternately appearing		Square wave		

5.8 MODEL GRAPH

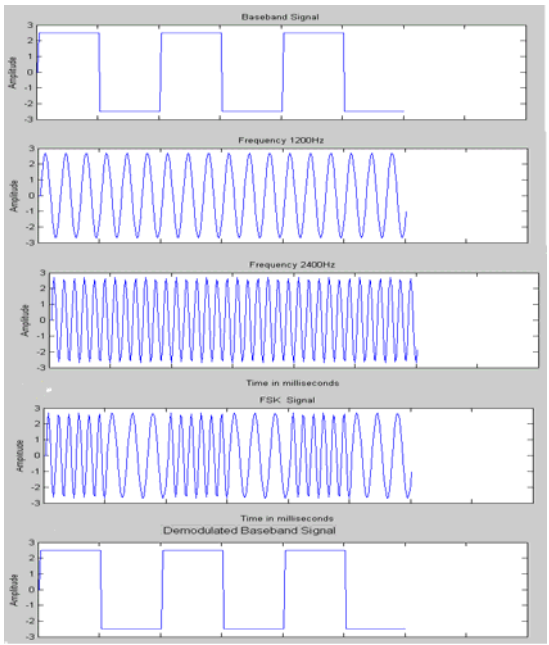


Figure 5.4

5.9 LAB RESULT

Thus the FSK modulation and demodulation were performed and required graphs were plotted.

5.10 POST LAB QUESTIONS

1. What is MSK?
2. For the given 8 bit data 10111010 draw the FSK output waveform.
3. Draw the constellation diagram of FSK.
4. What will happen if the same frequency is used for both the carriers?

6. PSK MODULATION AND DEMODULATION

6.1 OBJECTIVE

To analyze a PSK modulation system. and interpret the modulated and demodulated waveforms.

6.2 HARDWARE REQUIRED

1. PSK Trainer Kit - AET-71
2. Dual Trace oscilloscope-POS-2020
3. Digital Multimeter

6.3 INTRODUCTION

Phase shift keying is a modulation/data transmitting technique in which phase of the carrier signal is shifted between two distinct levels. In a simple PSK(ie binary PSK) unshifted carrier $V\cos\omega_0 t$ is transmitted to indicate a 1 condition, and the carrier shifted by 180^0 ie $-V\cos\omega_0 t$ is transmitted to indicate as 0 condition.

6.3.1 PSK Modulator

Figure 6.2shows the PSK modulator. IC CD 4052 is a 4 channel analog multiplexer and is used as an active component in this circuit. One of the control signals of 4052 is grounded so that 4052 will act as a two channel multiplexer and other control is being connected to the binary signal ie data to be transmitted. Unshifted carrier signal is connected directly to CH1 and carrier shifted by 180^0 is connected to CH2.phase shift network is a unity gain inverting amplifier using OP-amp (TL084).

When input data signal is 1 ie control signal is at high voltage, output of the 4052 is connected to CH1 and unshifted (or 0 phase)carrier is passed on to output. Similarly When data signal is 0 ie control signal is at zero voltage output of 4052 is connected to CH2 and carrier shifted by 180^0 is passed on to output.

6.3.2 PSK Demodulator:

Demodulation of PSK is achieved by subtracting the received carrier from a derived synchronous reference carrier of constant phase. Figure shows the simple coherent(synchronous) PSK demodulator.

Received PSK signal is converted to square wave using an op-amp(TL084) based zero crossing detector and connected to EX-OR circuit. The derived reference carrier is connected to other input of the EX-OR Gate through an op-amp based zero crossing detector. For the simplicity same carrier is used at receiver as reference carrier (In

practical communication system reference carrier is generated at receiver).We can observe the exact operation of demodulator with the help of waveforms at various nodes in the circuit.

CIRCUIT DIAGRAM

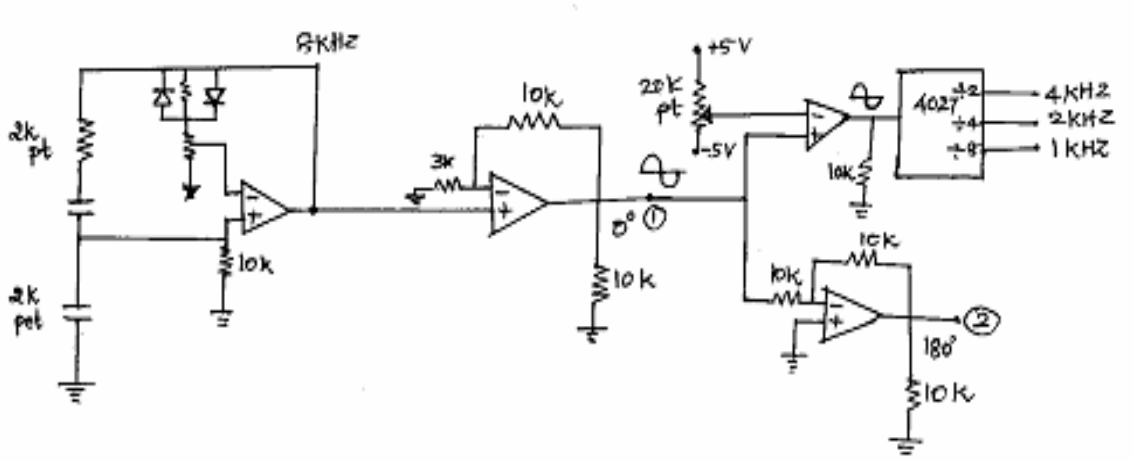


Fig 6.1. Phase Shift Keying

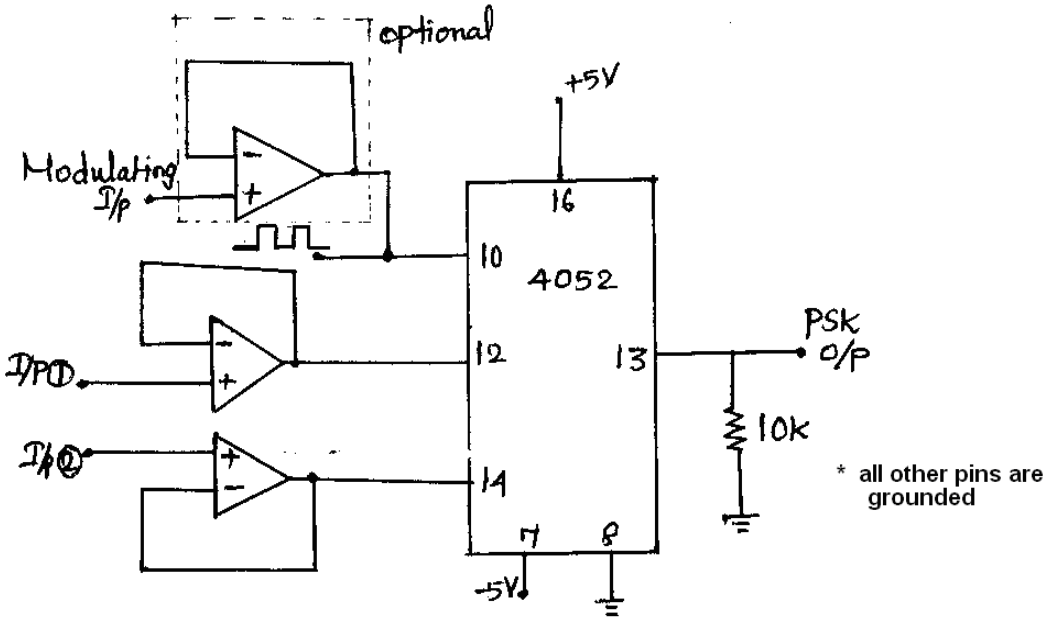


Fig 6.2 PSK Modulator

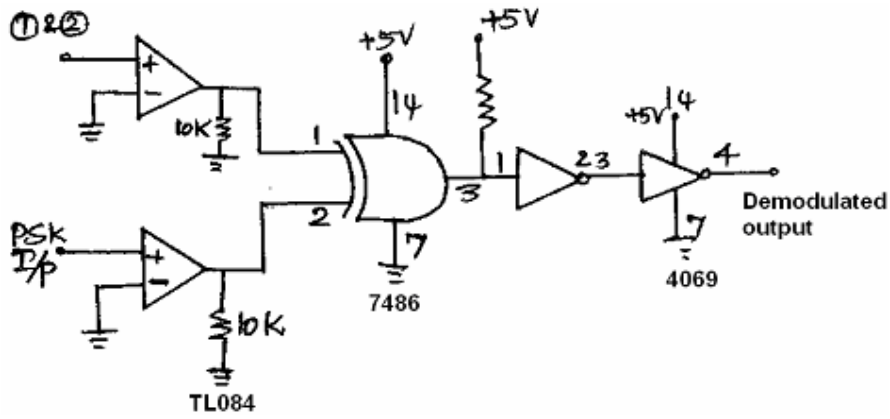


Fig 6.3 PSK Demodulator

Received PSK signal is converted to square wave using an op-amp(TL084) based zero crossing detector and connected to EX-OR circuit. The derived reference carrier is connected to other input of the EX-OR Gate through an op-amp based zero crossing detector. For the simplicity same carrier is used at receiver as reference carrier (In practical communication system reference carrier is generated at receiver).We can observe the exact operation of demodulator with the help of waveforms at various nodes in the circuit.

6.5 PRE LAB QUESTIONS

1. What are the applications of PSK?
2. What are antipodal signals?
3. Give the equation for average probability of symbol error for coherent binary PSK.
4. Explain how QPSK differs from PSK in terms of transmission bandwidth and bit information it carries
5. Draw the constellation diagram for PSK.

6.6 PROCEDURE

1. Connect the trainer to mains and switch on the power supply.
2. Measure the output of the regulated power supply ie +5V and -5V with the help of digital multimeter.
3. Observe the output of the carrier generator using CRO, it should be an 8KHZ sine with 5Vpp amplitude.
4. Observe the various data signals(1KHZ,2KHZ and 4KHZ0 using CRO

6.6.1 Modulation:

5. Connect carrier signal to carrier input of the PSK modulator.
6. Connect data signal say 4KHZ from data source to data input of the modulator.
7. Keep CRO in dual mode and connect CH1 input of the CRO to data signal and CH2 to the output of the PSK modulator.
8. Observe the PSK output signal with respect to data signal and plot the waveforms.

6.6.2 Demodulation:

9. Connect the PSK output to the PSK input of the demodulator.
10. Connect carrier to the carrier input of the PSK demodulator.
11. Keep CRO in dual mode and connect CH1 to data signal(at modulator) and CH2 to the output of the demodulator.
12. Compare the demodulated signal with the original signal. By this we can notice that there is no loss in modulation and demodulation process
13. Repeat the steps 6 to 12 with different data signals ie 2KHZ and 1KHZ

6.7 MODEL GRAPH

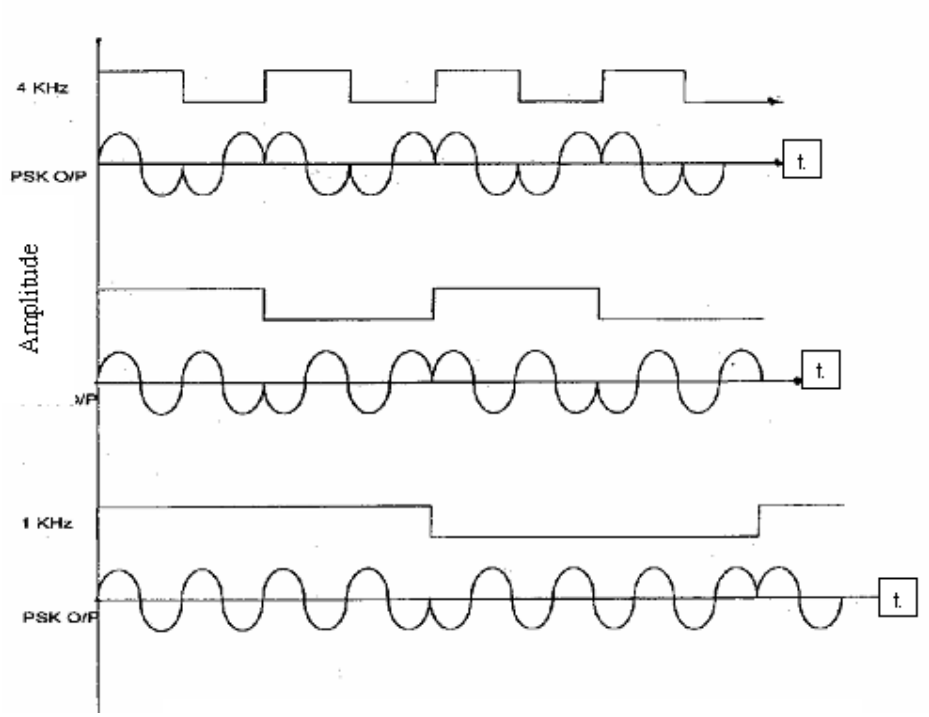


Fig 6.4. PSK Waveforms for different data input signals

6.8 OBSERVATION

PSK (Modulation) -AC signal

	Amplitude	Time Period
Carrier signal		
Data source For 4KHz For 2KHz For 1KHz		
Modulated output For 4KHz For 2KHz For 1KHz		

Demodulation

	Amplitude	Time Period
Demodulated output For 4KHz For 2KHz For 1KHz		

6.9 LAB RESULT

Thus the PSK modulation and demodulation were performed and graphs were plotted.

6.10 POST LAB QUESTIONS

1. Compare FSK and PSK.
2. List the Characteristics of TL084 op-amp.
3. Compare TL084 op amp with IC 741 op amp.
4. What do we infer from constellation diagrams of various modulation schemes.

7. DATA FORMATTING

7.1. OBJECTIVE

To identify the various encoding schemes for a given data stream.

7.2. HARDWARE REQUIRED

1. Coding Kits.
2. CRO

7.3. INTRODUCTION

'1' and '0' can be represented in various formats in different levels and waveforms. The selection of coding technique depends on system band width, systems ability to pass dc level information, error checking facility.

Non return to Zero (level):

The NRZ(L) waveform simply goes low for one bit time to represent a data '0' and high to represent data '1'.For lengthy data the clock is lost in asynchronous mode. The maximum rate at which NRZ can change is half the data clock.[when alternate 0's and 1's are there.

DC Level:

A length data will have only a dc level as its waveform, a dc voltage cannot be used in circuits which involve transformers like telephone, AC coupled amplifiers, capacitors, filter etc.

Manchester Biphase:

'0' is encoded low during first half of bit time & high for other half of bit & vice versa for '1'.There is no synchronization problem in the receiver. It is independent of DC levels, since there is a transition occurring in each bit. Its max frequency is equal to data clock rate. There is at least one transition per bit. Since there is midway transition, it makes clock regeneration difficult so we use special bi phase clock recovery circuit

7.4 MODEL GRAPH

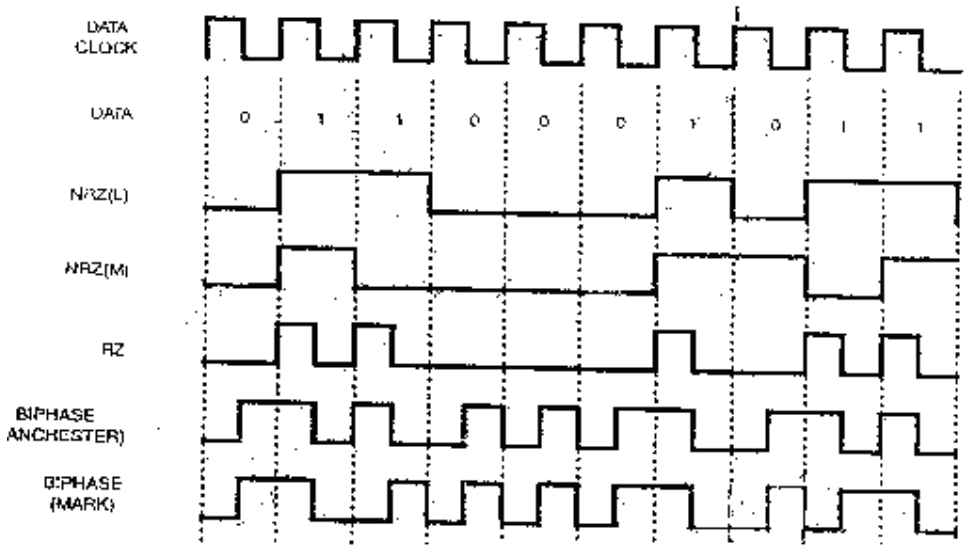


Fig 7.1 Data Encoding Schemes

Return to Bias:

It is a 3 level code it consist of positive, negative and zero. Easy clock synchronization is possible.'1' for positive,'0' for negative in first half and zero bias for second half. Maximum frequency is equal to data clock frequency. DC levels of waveforms depends on strings of 1's and 0's.Hence we cannot use AC coupled communication link. Timing information is easily obtained. The system is referred to as 'self clocking system', as magnitude of waveform is original data signal. It requires complex transmitters.

7.5 PRELEB QUESTIONS

1. Compare NRZ-I and NRZ- L .
2. What is the use of data formatting?
3. Compare NRZ and biphase encoding .
4. What is the relationship between quantization levels and number of bits in a code word?
5. Give the advantages of Manchester encoding.

7.6.TEST PROCEDURE

1. Connect the data generator output to code generator kit. This gives the random binary sequence o the kit.
2. Connect the clock signal to the trainer kit.
3. Connect the output to the CRO channel along with the clock signal.
4. Observe the waveforms with respect to clock on a dual channel CRO, and compare with the model graph.
5. Plot the waveforms for different codes.

7.7 LAB RESULT

Thus the different coding techniques were studied and observed for a given binary data, and their corresponding waveforms plotted.

7.8. POST LAB QUESTIONS

1. Assume a data stream is made of ten 0s. Encode this stream using the following encoding schemes. How many change can you find for each scheme?

   a)NRZ

   b)RZ

   c)Bi phase
2. If the bit rate of a signal is 1000 bits/seconds, how many bits can be sent in 4 seconds? How many bits in 1/5 seconds? How many in 100 milli seconds?
3. List out the merits & demerits of each data formats .
4. Represent the given data 11010100 in Manchester encoding and NRZ –M scheme.

8. Amplitude Shift Keying

8.1 OBJECTIVE

To simulate Binary Amplitude shift keying technique using MATLAB software

8.2 SOFTWARE REQUIRED

MATLAB ,Computer installed with Windows XP or higher Version.

8.3 PREPARATION (PRE-LAB)

1. Given a bandwidth of 5000 Hz for an ASK signal, what are the baud rate and bit rate?
2. Find the minimum bandwidth for an ASK signal transmitting at 2000bps.

8.4 MATLAB® INTRODUCTION

MATLAB® is a programming language and numerical computing environment. The name MATLAB® is an acronym for "Matrix Laboratory". As it name suggests it allows easy manipulation of matrix and vectors. Plotting functions and data is made easy with MATLAB®. It has a good Graphic User Interface and conversion of matlab files to C/C++ is possible. It has several toolboxes that possess specific functions for specific applications. For example Image Processing, Neural Networks, CDMA toolboxes are name a few. An additional package, Simulink, adds graphical multidomain simulation and Model-Based Design for dynamic and embedded systems. Simulink contains Blocksets that is analogous to Toolboxes.It was created by Mathworks Incorporation, USA. MATLAB® has become a defacto programming language for Engineers. Writing MATLAB programs for modulation applications require knowledge on very few functions and operators. The operators mostly used are arithmetic operators and matrix operators. To know more type in the command prompt 'help ops'. MATLAB will give a list in that to know on specific operator say addition type in the command prompt 'help plus'. MATLAB will give how to use and other relevant information. Commonly used graphical functions are plot, figure, subplot, title, and mathematical functions are sin and cos only. The mathematical functions sin and cos are self explanatory. The graphical function figure will create a new window and then subsequent graphical commands can be applied. The plot function usually takes two vectors and plot data points according to given vector data. In this case it will time Vs signal. Subplot function is used when two or more plots are drawn on the same figure. As title function suggests it helps to write title of the graph in the figure. For further details type 'help plot' or 'help subplot' in the command prompt and learn the syntax.

8.5 THEORY

Amplitude Shift Keying

ASK is a form of modulation that represents digital data as variations in the amplitude of a carrier wave.The amplitude of an analog carrier signal varies in accordance with the bit stream (modulating signal), keeping frequency and phase constant.

On-off keying (**OOK**) the simplest form of amplitude-shift keying (ASK) modulation that represents digital data as the presence or absence of a carrier wave. In its simplest form, the presence of a carrier for a specific duration represents a binary one, while its absence for the same duration represents a binary zero.

In a ASK system, the pair of signal $S_1(t)$ used to represent binary symbols 1 & 0 are defined by

$S_1(t) = \sqrt{2E_b/\tau b} \cos 2\pi f_c t$
0 where $0 \leq t < T_b$ and
Eb = Transmitted signed energy for bit
The carrier frequency $fc = n/T_b$ for some fixed integer n.

Block Diagram of ASK Transmitter

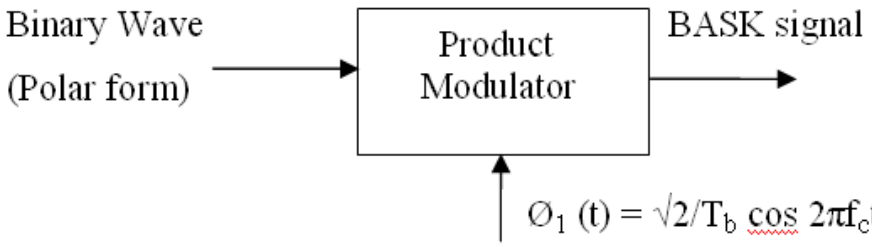


Fig 8.1 ASK Transmitter block diagram

The input binary symbols are represented in polar form with symbols 1 & 0 represented by constant amplitude levels √Eb & -√Eb. This binary wave is multiplied by a sinusoidal carrier in a product modulator. The result is a ASK signal.

ASK Receiver

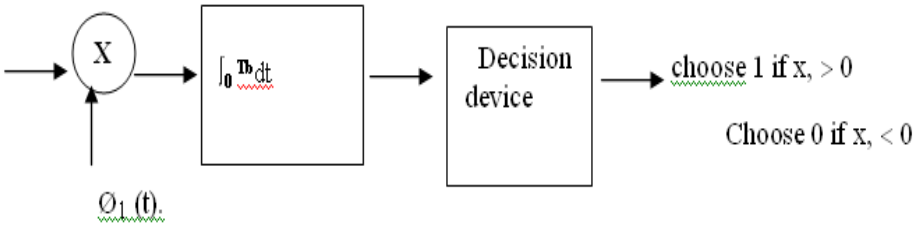


Fig 8.2 ASK Receiver block diagram

The received ASK signal is applied to a correlator which is also supplied with a locally generated reference signal $Ø_1(t)$. The correlated o/p is compared with a threshold

of zero volts. If x1> 0, the receiver decides in favour of symbol 1. If x1< 0, it decides in favour of symbol 0

8.6 ALGORITHM

ASK Modulation

4. Generate the carrier signal ($Ø_1$ (t) = $\sqrt{2}/T_b \cos 2\pi f_c t$)
5. Generate the base band data signal .
6. Multiply the polar form data signal and carrier signal. The resultant signal is a PSK signal.
7. Plot the carrier, data and PSK signal.

ASK Demodulation

4. Multiply the received PSK signal with the carrier signal ($Ø_1$ (t) = $\sqrt{2}/T_b \cos 2\pi f_c t$)
5. Integrate the resultant signal(x1) .
6. If x1 is greater than zero then choose 1 and if it is less than 0 choose 0.
7. Plot the demodulated signal.

8.7 TEST PROCEDURE

1. Open the MATLAB® software by double clicking its icon.
2. MATLAB® logo will appear and after few moments Command Prompt will appear.
3. Go to the File Menu and select a New M- file. (File □New□M-file) or in the left hand corner a blank white paper icon will be there. Click it once.
4. A blank M- file will appear with a title 'untitled'
5. Now start typing your program. After completing, save the M- file with appropriate name. To execute the program Press F5 or go to Debug Menu and select Run.
6. After execution output will appear in the Command window .If there is an error then with an alarm, type of error will appear in red color.
7. Rectify the error if any and go to Debug Menu and select Run.

8.8 LAB RESULT

Thus the ASK modulated and demodulated waves are simulated .

8.9 POST LAB QUESTIONS

1. Write a matlab program to generate sync function
2. Perform the Binary ASK modulation and demodulation using hardware kit and study the waveform output
3. Differentiate plot and subplot commands in MATLAB.

9. Binary Frequency Shift Keying

9.1 OBJECTIVE

To simulate Binary Frequency shift keying technique using MATLAB software

9.2 SOFTWARE REQUIRED

MATLAB ,Computer installed with Windows XP or higher Version.

9.3 PREPARATION (PRE-LAB)

1. Define modulation index.
2. Write a matlab program for generating PN sequence.
3. What is MSK and mention its significance.
4. Differentiate coherent and non-coherent FSK.
5. Give the expression for bandwidth of FSK scheme.

9.4 THEORY

Binary Frequency Shift Keying

In binary FSK system, symbol 1 & 0 are distinguished from each other by transmitting one of the two sinusoidal waves that differ in frequency by a fixed amount.

$Si(t) = \sqrt{2E/T_b} \cos 2\pi f_1 t \quad ; \quad 0 \leq t \leq T_b$

$0 \quad ; \quad$ elsewhere

Where i=1, 2 & E_b=Transmitted energy/bit

Transmitted freq= $fi = (nc+i)/T_b$, and n = constant (integer), T_b = bit interval

Symbol 1 is represented by $S_1(t)$

Symbol 0 is represented by $S_0(t)$

The set of orthonormal basis function is

$Øi(t) = \{\sqrt{2/T_b} \cos 2\pi f_1 t \quad ; \quad 0 \leq t \leq T_b$

$0 \quad ; \quad$ elsewhere

Where i = 1, 2.

The two message points (M =2) are defined by signal vectors

$S_1 = [\sqrt{E_b}\ 0]$ S2 = $[0\ \sqrt{E_b}]$

Block diagram of BFSK Transmitter

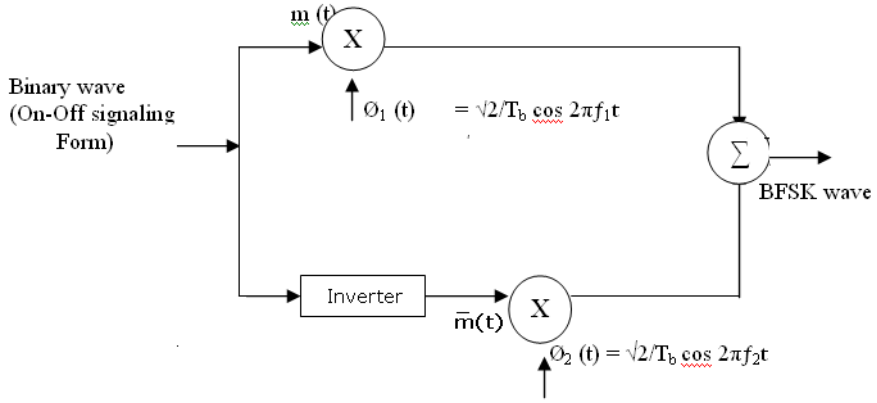


Fig 9.1 FSK Transmitter Block Diagram

The i/p binary sequence is represented in its on-off form, with symbol 1 represented by constant amplitude of $\sqrt{E_b}$ with & symbol 0 represented by zero volts. By using inverter in the lower channel, we in effect make sure that when symbol 1is at the i/p, The two frequency f1& f2 are chosen to be equal integer multiples of the bit rate $1/T_b$

By summing the upper & lower channel outputs, we get BFSK signal.

BFSK Receiver

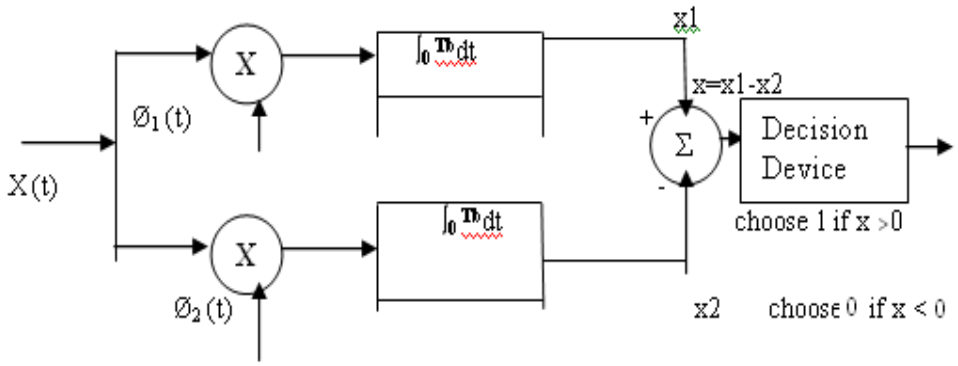


Fig 9.2 FSK Receiver Block Diagram

The receiver consists of two correlators with common inputs which are supplied with locally generated coherent reference signals $Ø_1(t)$ and $Ø_2$ (t).

The correlator outputs are then subtracted one from the other, and the resulting difference L is compared with a threshold of zero volts. If L >0, the receiver decides in favour of symbol 1 and if L <0, the receiver decides in favour of symbol 0.

9.5 ALGORITHM

BFSK Modulation

1. Generate two carrier signals ($Ø_1$ (t) = $\sqrt{2}/T_b \cos 2\pi f_1 t$ and $Ø_2$ (t) = $\sqrt{2}/T_b \cos 2\pi f_2 t$)
2. Generate the base band data signal .
3. Convert the base band signal into on-off form.(i.e m(t))
4. Multiply the on-off form data signal m(t) and carrier signal 1 in one channel .
5. Invert the signal m(t) to get m_1 (t)
6. Multiply the on-off form data signal m_1 (t)and carrier signal 2in another channel
7. Sum the output resultant signals of step 4 and 5.
8. The resultant signal is a FSK signal
9. Plot the carrier, data and FSK signal.

BFSK Demodulation

1. Multiply the received FSK signal with the carrier signal $Ø_1$ (t) = $\sqrt{2}/T_b \cos 2\pi f_1 t$ in one channel and integrate the resultant signal(x1)
2. Multiply the received FSK signal with the carrier signal $Ø_2$ (t) = $\sqrt{2}/T_b \cos 2\pi f_2 t$ in another channel and integrate the resultant signal(x2)
3. Find x=x1-x2.
4. If x is greater than zero then choose 1 and if it is less than 0 choose 0 .
5. Plot the demodulated signal.

9.6 TEST PROCEDURE

1. Open the MATLAB® software by double clicking its icon.
2. MATLAB® logo will appear and after few moments Command Prompt will appear.
3. Go to the File Menu and select a New M- file. (File □New□M-file) or in the left hand corner a blank white paper icon will be there. Click it once.
4. A blank M- file will appear with a title ‘untitled’
5. Now start typing your program. After completing, save the M- file with appropriate name. To execute the program Press F5 or go to Debug Menu and select Run.
6. After execution output will appear in the Command window .If there is an error then with an alarm, type of error will appear in red color.
7. Rectify the error if any and go to Debug Menu and select Run.

9.7 LAB RESULT

Thus the FSK modulated and demodulated waves are simulated.

9.8 POST LAB QUESTIONS

1. Determine the bandwidth and baud for an BFSK signal with mark frequency of 49 KHz, a space frequency of 51 KHz, and a bit rate of 2 Kbps.
2. Write a matlab program for finding the sum of series 1+ 2+ 3 +……+N
3. Sketch the FSK waveform for the input a) 1010110 b) 1100101

10. Binary Phase Shift Keying

10.1 OBJECTIVE

To simulate Binary Phase shift keying technique using MATLAB software

10.2 SOFTWARE REQUIRED

MATLAB, Computer installed with Windows XP or higher Version.

10.3 PREPARATION (PRE-LAB)

1) An analog signal carries four bits in each signal element. If 1000 signal elements are sent per second , find the baud rate and bit rate.
2) What is a correlator?

10.4 MATLAB® INTRODUCTION

MATLAB® is a programming language and numerical computing environment. The name MATLAB® is an acronym for "Matrix Laboratory". As it name suggests it allows easy manipulation of matrix and vectors. Plotting functions and data is made easy with MATLAB®. It has a good Graphic User Interface and conversion of matlab files to C/C++ is possible. It has several toolboxes that possess specific functions for specific applications. For example Image Processing, Neural Networks, CDMA toolboxes are name a few. An additional package, Simulink, adds graphical multidomain simulation and Model-Based Design for dynamic and embedded systems. Simulink contains Blocksets that is analogous to Toolboxes.It was created by Mathworks Incorporation, USA. MATLAB® has become a defacto programming language for Engineers. Writing MATLAB programs for modulation applications require knowledge on very few functions and operators. The operators mostly used are arithmetic operators and matrix operators. To know more type in the command prompt 'help ops'. MATLAB will give a list in that to know on specific operator say addition type in the command prompt 'help plus'. MATLAB will give how to use and other relevant information. Commonly used graphical functions are plot, figure, subplot, title, and mathematical functions are sin and cos only. The mathematical functions sin and cos are self explanatory. The graphical function figure will create a new window and then subsequent graphical commands can be applied. The plot function usually takes two vectors and plot data points according to given vector data. In this case it will time Vs signal. Subplot function is used when two or more plots are drawn on the same figure. As title function suggests it helps to write title

of the graph in the figure. For further details type 'help plot' or 'help subplot' in the command prompt and learn the syntax.

10.5 THEORY

Binary Phase Shift Keying

In a coherent binary PSK system, the pair of signal $S_1(t)$ and $S_2(t)$ used to represent binary symbols 1 & 0 are defined by

$S_1(t) = \sqrt{2E_b/\tau b} \cos 2\pi f_c t$

$S_2(t) = \sqrt{2E_b/T_b}(2\pi f_c t + \pi) = -\sqrt{2E_b/T_b} \cos 2\pi f_c t$ where $0 \le t < T_b$ and

Eb = Transmitted signed energy for bit

The carrier frequency $fc = n/T_b$ for some fixed integer n.

In BPSK, there is only one basis function of unit energy.

$\emptyset_b(t) = \sqrt{2/T_b} \cos 2f\pi ct$ $0 \le t < T_b$

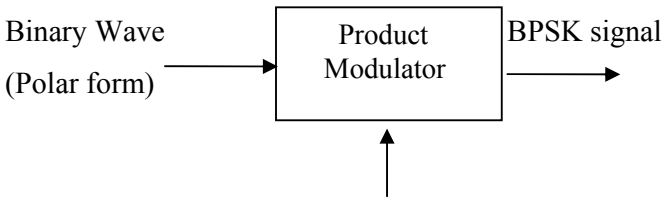
$S_1(t) = \sqrt{E_b}\ \emptyset_1(t)$ $0 \le t \le T_b$

$S_2(t) = \sqrt{E_b}\ \emptyset_1(t)$ $0 \le t < T_b$

The signal space is 1dimensional (N=1) having two message points (M = 2)

Block Diagram of BPSK Transmitter

The input binary symbols are represented in polar form with symbols 1 & 0 represented by constant amplitude levels √Eb & -√Eb. This binary wave is multiplied by a sinusoidal carrier in a product modulator. The result in a BSPK signal.



$\emptyset_1(t) = \sqrt{2/T_b} \cos 2\pi f_c t$

Fig 10.1 PSK Transmitter Block Diagram

BSPK Receiver:

The received BPSK signal is applied to a correlator which is also supplied with a locally generated reference signal $\emptyset_1(t)$. The correlated o/p is compared with a threshold of zero volts. If x1> 0, the receiver decides in favour of symbol 1. If x1< 0, it decides in favour of symbol 0

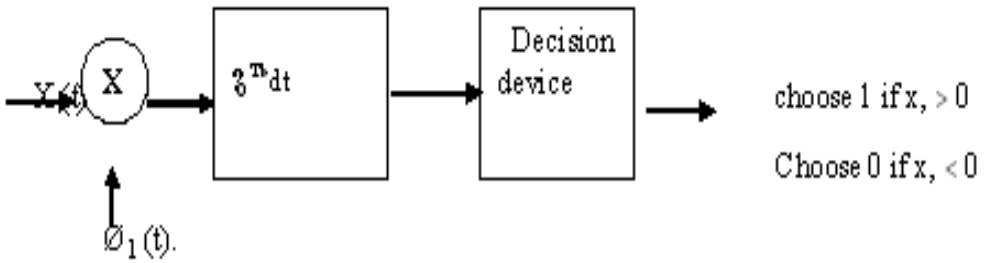


Fig 10.2 PSK Receiver Block Diagram

The received BPSK signal is applied to a correlator which is also supplied with a locally generated reference signal $\emptyset_1$ (t). The correlated o/p is compared with a threshold of zero volts. If x1> 0, the receiver decides in favour of symbol 1. If x1< 0, it decides in favour of symbol 0

10.6 ALGORITHM

BPSK Modulation

1. Generate the carrier signal ($\emptyset_1$ (t) = $\sqrt{2}/T_b \cos 2\pi f_c t$)
2. Generate the base band data signal .
3. Convert the base band signal into polar form.
4. Multiply the polar form data signal and carrier signal. The resultant signal is a PSK signal.
5. Plot the carrier, data and PSK signal.

BPSK Demodulation

1. Multiply the received PSK signal with the carrier signal ($\emptyset_1$ (t) = $\sqrt{2}/T_b \cos 2\pi f_c t$)
2. Integrate the resultant signal(x1) .
3. If x1 is greater than zero then choose 1 and if it is less than 0 choose 0.
4. Plot the demodulated signal.

10.7 TEST PROCEDURE

1. Open the MATLAB® software by double clicking its icon.
2. MATLAB® logo will appear and after few moments Command Prompt will appear.
3. Go to the File Menu and select a New M- file. (File □New□M-file) or in the left hand corner a blank white paper icon will be there. Click it once.

4. A blank M- file will appear with a title ‘untitled’
5. Now start typing your program. After completing, save the M- file with appropriate name. To execute the program Press F5 or go to Debug Menu and select Run.
6. After execution output will appear in the Command window .If there is an error then with an alarm, type of error will appear in red color.
7. Rectify the error if any and go to Debug Menu and select Run.

10.8 LAB RESULT

Thus the FSK modulated and demodulated waves are simulated .

10.9 POST LAB QUESTIONS

1. Write matlab program to encode the data sequence using
    a) RZ
    b) NRZ
    c) Manchester
    d) Differential encoding.

2.Why do we make 180 degree phase shift in PSK and why not 90 or 270?comment on this.

3. What is the function of a decision device.

11. Quadrature Phase Shift Keying

11.1 OBJECTIVE

To simulate Quadrature Phase shift keying technique using MATLAB software

11.2 SOFTWARE REQUIRED

MATLAB, Computer installed with Windows XP or higher Version.

11.3 PREPARATION (PRE-LAB)

1. What are the types of QPSK?
2. What is the significance of Q-channel and I channel in QPSK modulator?
3. What is the minimum bandwidth requirement of QPSK?
4. Draw the output phase versus time relationship for a QPSK modulator.
5. Compare OQPSK and QPSK.

11.4 THEORY

Quadrature Phase Shift Keying

Phase of the carrier takes on one of four equally spaced values such as π/4, 3π/4, /4,7π/4.

$$Si(t) = \sqrt{2E/T_b}\cos\{2\pi f_c t + (2i-1)\pi/4\}, \quad 0 \le t \le T_b$$

$$0, \quad \text{elsewhere}$$

Where i = 1,2,3,4, & E= Tx signal energy per symbol

T_b = symbol duration

Each of the possible value of phase corresponds to a pair of bits called dibits.

Thus the gray encoded set of dibits: 10,00,01,11

$Si(t) = \sqrt{2E/T_b}\cos[(2i-1)\pi/4]\cos(2\pi f_c t) - \sqrt{2E/T_b}\sin[(2i-1)\pi/4)]\sin(2\pi f_c t)$,$0 \le t \le T_b$ 0 , else where

There are two orthononormal basis functions

$$\emptyset_1(t) = \sqrt{2/T_b}\cos 2\pi f_c t, \qquad 0 \le t \le T_b$$

$$\emptyset_2(t) = \sqrt{2/T_b}\sin 2\pi f_c t, \qquad 0 \le t \le T_b$$

There are four message points

Input debits	Phase of QPSK signal	Co-ordinates of message signals	
		S1	S2
10	π/4	√E/2	-√E/2
00	3π/4	-√E/2	-√E/2
01	5π/4	-√E/2	+√E/2
11	7π/4	+√E/2	+√E/2

Block diagram of QPSK Transmitter

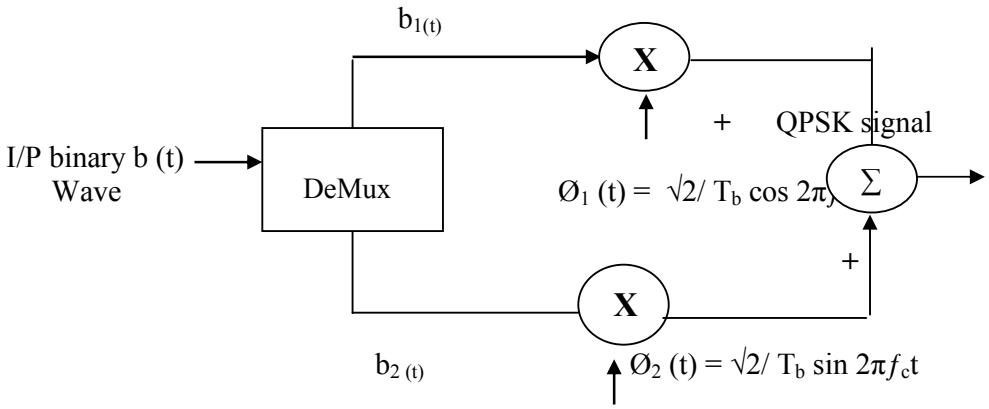


Fig 11.1 QPSK Transmitter Block Diagram

The i/p binary sequence b(t) is represented in polar from with symbols 1 & 0 represented as $+\sqrt{E/2}$ and $-\sqrt{E/2}$ .This binary wave is demultiplexed into two separate binary waves consisting of odd & even numbered I/P bits denoted by b_1 (t) & b_2 (t)

b_1 (t) & b_2(t) are used to modulate a pair of quadrature carrier or orthogonal Basis function $Ø_1$ (t) & $Ø_2$ (t).

The result is two PSK waves' .These two binary PSK waves are added to produce the desired QPSK signal .

QPSK Receiver:

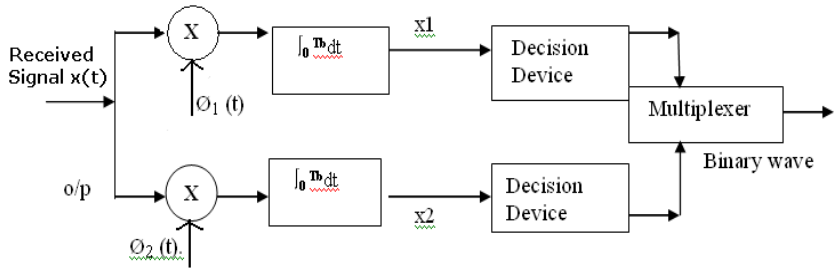


Fig 11.2 QPSK Receiver Block Diagram

QPSK receiver consists of a pair of correlators with common I/P & supplied with Locally generated Signal $Ø_1$ (t) & $Ø_2$ (t).The correlator O/P, x_1, & x_2 are each compared with a threshold of zero volts.If $x_1 > 0$, decision is made in favour of symbol '1' for upper channel and if $x_1 > 0$, decision is made in favour of symbol 0.

Parallely Y $x_2 > 0$, decision is made in favour of symbol 1 for lower channel & if $x_2 < 0$, decision is made in favour of symbol 0.

These two channels are combined in a multiplexer to get the original binary output.

11.5 ALGORITHM

QPSK Modulation

1. Generate two carrier signals ($Ø_1$ (t) = $\sqrt{2}/T_b \cos 2\pi f_c t$ and $Ø_2$ (t) = $\sqrt{2}/T_b \cos 2\pi f_c t$)

2. Generate the base band data signal .
3. Binary wave is divided into odd($b_1(t)$) and even($b_2(t)$) numbered input bits.
4. Multiply the odd numbered data signal ($b_1(t)$) and carrier signal 1 in one channel .
5. Multiply the even numbered data signal b_2 (t)and carrier signal 2in another channel
6. Sum the output resultant signals of step 4 and 5.
7. The resultant signal is a QPSK signal
8. Plot the carrier, data and QPSK signal.

QPSK Demodulation

1. Multiply the received QPSK signal with the carrier signal $Ø_1$ (t) = $\sqrt{2}/T_b \cos 2\pi f_c t$ in one channel and integrate the resultant signal(x1)
2. Multiply the received QPSK signal with the carrier signal $Ø_2$ (t) =$\sqrt{2}/T_b \cos 2\pi f_c t$ in another channel and integrate the resultant signal(x2)
3. If x_1 is greater than zero then choose 1 and if it is less than 0 choose 0.
4. If x_1 is greater than zero then choose 1 and if it is less than 0 choose 0
5. Multiply the resultant signal from step 3 and 4.
6. Plot the demodulated signal.

11.6 TEST PROCEDURE

1. Open the MATLAB® software by double clicking its icon.
2. MATLAB® logo will appear and after few moments Command Prompt will appear.
3. Go to the File Menu and select a New M- file. (File □New□M-file) or in the left hand corner a blank white paper icon will be there. Click it once.
4. A blank M- file will appear with a title 'untitled'
5. Now start typing your program. After completing, save the M- file with appropriate name. To execute the program Press F5 or go to Debug Menu and select Run.
6. After execution output will appear in the Command window .If there is an error then with an alarm, type of error will appear in red color.
7. Rectify the error if any and go to Debug Menu and select Run.

11.7 LAB RESULT

Thus the QPSK modulated and demodulated waves are simulated .

11.8 POST LAB QUESTIONS

1. Write a matlab program to sample a message signal m(t) and reconstruct it.
2. Identify the error in the mat lab command Sin 3.

3. Draw the constellation diagram of QPSK.
4. Give some applications of QPSK modulation scheme
5. Find the output of the following command.

   5^ (2/3) – 25/(2*3)

6. What is the relationship between 4 QAM and QPSK?
7. Design a SIMULINK model for QPSK.

12. Differential Phase-shift Keying

12.1 OBJECTIVE

To simulate Differential Phase shift keying technique using MATLAB software

12.2 SOFTWARE REQUIRED

MATLAB ,Computer installed with Windows XP or higher Version.

12.3 PREPARATION (PRE-LAB)

1. What are the applications of DPSK?
2. Give the equation for average probability of symbol error for DPSK.
3. List the operations performed in DPSK transmitter.

12.4 THEORY

Differential phase shift keying

It is the non-coherent version of PSK. It eliminates the need for a coherent reference signal at the receiver by combining two basic operations at the transmitter:

i) Differential encoding of the input binary wave

ii) Phase shift keying

In effect, to send symbol 0 we phase advance the current signal waveform by 180˚ , and to send symbol 1 we leave the phase of the current signal waveform unchanged.

Block diagram of DPSK Transmitter:

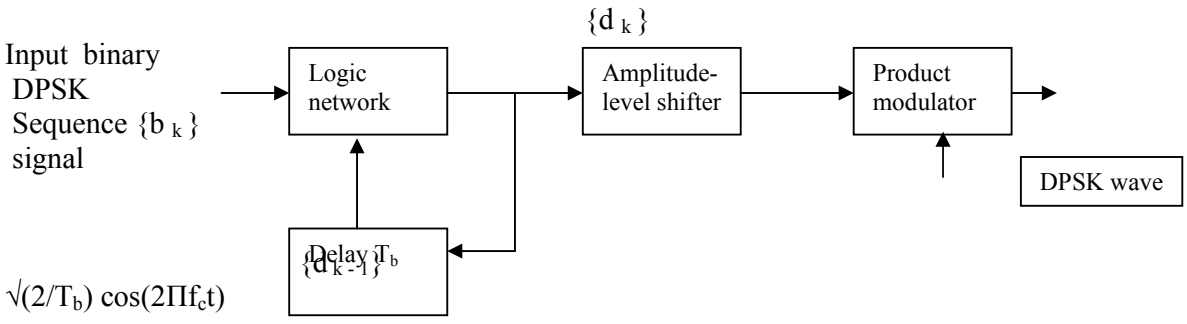


Fig 12.1 DPSK Transmitter Block Diagram

The DPSK transmitter consists of a logic network and a one-bit delay element interconnected so as to convert an input sequence $\{b_k\}$ into a differentially encoded

sequence $\{d_k\}$. This sequence is amplitude level shifted and then used to modulate a carrier wave of frequency f_c, thereby producing the desired DPSK wave.

Block Diagram of DPSK Receiver:

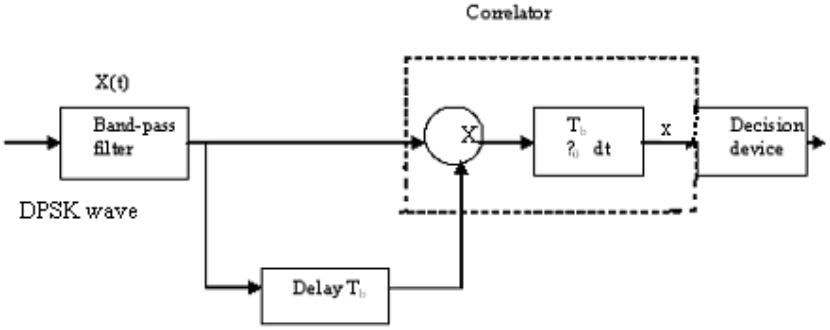


Fig 12.2 DPSK Receiver Block Diagram

The received DPSK signal plus noise is passed through a band pass filter centered at the carrier frequency f_c , so as to limit the noise power. The filter output and a delayed version of it, with the delay equal to the bit duration T_b, are applied to a correlator. The resulting correlator output is proportional to the cosine of the difference between the carrier phase angles in the two correlator inputs. The correlator output is finally compared with a threshold of zero volts, and a decision is thereby made in favor of symbol 1 or symbol 0. If the correlator output is positive, the phase difference between the waveforms received during the pertinent pair of bit intervals lies inside the range –Π/2 to Π/2, and the receiver decides in favor of symbol 1.If , on the other hand, the correlator output is negative, the phase difference lies outside the range –Π/2 to Π/2, modulo-2Π, and the receiver decides in favor of symbol 0.

12.5 ALGORITHM

DPSK Modulation

1. Generate the base band data signal b_k.
2. Generate the differentially encoded sequence d_k, using the equation
3. $d_K = d_{K-1} b_K \oplus \overline{d_{K-1}}\,\overline{b_K}$
4. Convert d_k into amplitude level shifted sequence.
5. Generate the carrier signal $\sqrt{(2/T_b)}\cos(2\Pi f_c t)$
6. Multiply the amplitude level shifted sequence with the carrier signal .
7. The resultant signal is a DPSK signal
8. Plot the carrier, data and DPSK signal.

DPSK Demodulation

1. Multiply the received DPSK signal with the delayed version of it and integrate the resultant signal (x).
2. If x is greater than zero then choose 1 and if it is less than 0 choose 0 .
3. Plot the demodulated signal.

12.6 TEST PROCEDURE

1. Open the MATLAB® software by double clicking its icon.
2. MATLAB® logo will appear and after few moments Command Prompt will appear.
3. Go to the File Menu and select a New M- file. (File □New□M-file) or in the left hand corner a blank white paper icon will be there. Click it once.
4. A blank M- file will appear with a title 'untitled'
5. Now start typing your program. After completing, save the M- file with appropriate name. To execute the program Press F5 or go to Debug Menu and select Run.
6. After execution output will appear in the Command window .If there is an error then with an alarm, type of error will appear in red color.
7. Rectify the error if any and go to Debug Menu and select Run.

12.7 LAB RESULT

Thus the DPSK modulated and demodulated waves are simulated.

12.8 POST LAB QUESTIONS

1. Write a matlab program for computing linear and circular convolution of two sequences.
2. Compare DPSK with QPSK modulation scheme.
3. What is differential encoding technique.

Appendix
Data sheet of IC7805

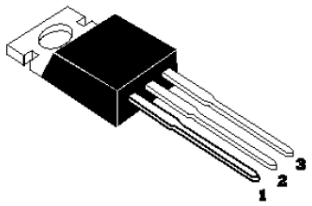
FORWARD INTERNATIONAL ELECTRONICS LTD.

SEMICONDUCTOR
TECHNICAL DATA

7805
LINEAR INTEGRATED CIRCUIT

3-TERMINAL POSITIVE VOLTAGE REGULATOR

Package: TO-220



PIN: / STYLE	1	2	3
NO.1	I	G	O

FEATURES

*Output current In Excess Of 1A
*Fixed output voltage of 5V available
*Thermal overload shutdown protection
*Short circuit current limiting
*Output transistor SOA protection

ABSOLUTE MAXIMUM RATINGS

(Operating temperature range applies unless otherwise specified)

Characteristic	Symbol	Rating	Unit
Input voltage	V_I	35	V
Output Current	I_O	1.5	A
Power Dissipation	P_D	internally Limited	mW
Operating Junction Temperature Range	T_{OPR}	-20~150	^{0}C
Storage Temperature Range	T_{STG}	-55~150	^{0}C

ELECTRICAL CHARACTERISTICS at Tamb=25^{0}C

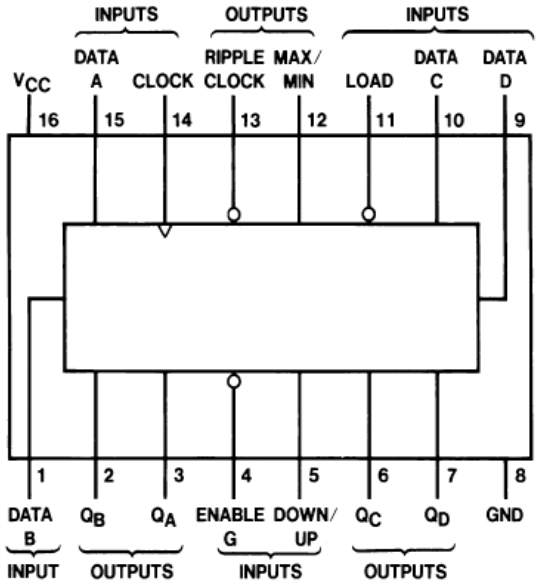
(V_I=10V,I_O=0.5A,0°C<T_j<125°C,C_i=0.33uF,C_O=0.1uF,unless otherwise specified)(Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Voltage	V_O	4.8	5	5.2	V	T_j=25°C
Output Voltage	V_O	4.75		5.25	V	8V≦ V_I≦ 20V,I_O=5mA-1.0A PD<15W
Load Regulation	ΔV_O		1.3	100	mV	T_j=25°C,I_O=5mA-1.5A
Load Regulation	ΔV_O		0.15	50	mV	T_j=25°C,I_O=0.25A-0.75A
Line Regulation	ΔV_O		5	100	mV	7V≦ V_I≦ 25V,T_j=25°C
Line Regulation	ΔV_O		1.3	50	mV	8V≦ V_I ≦12V,T_j=25°C
Quiescent Current	Iq		3.2	8	mA	T_j=25°C
Quiescent Current Change	Δ Iq			1.3	mA	8V≦ V_I≦ 25V
Quiescent Current Change	Δ Iq			0.5	mA	5mA≦ I_O≦ 1.0A
Output Noise Voltage	V_N		10		uV	10Hz≦ f≦100kHz
Temperature coefficient of V_O	$\Delta V_O/\Delta T$		-0.30		mV/°C	
Ripple Rejection	RR		68		dB	8V≦ V_I≦ 18V,f=120Hz,T_j=25°C
Peak Output Current	Ipk		2.2		A	Tj=25°C
Short-Circuit Current	Isc		200		mA	VI=35V,Tj=25°C
Dropout Voltage	V_D		2.0		V	T_j=25°C Io=1A

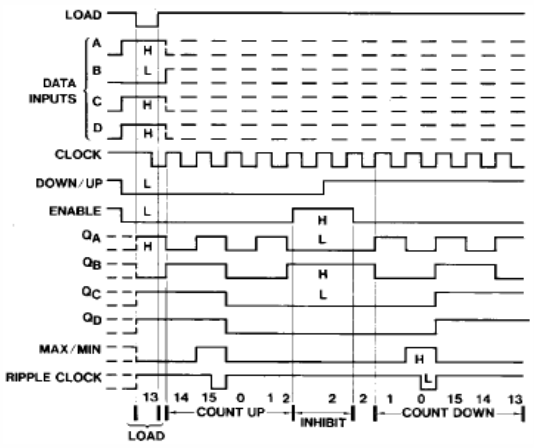
Note1: The maximum steady state usable output current is dependent on input voltage, heat sinking, lead length of the package and copper patten of PCB. The data above represent pulse test conditions with junction temperatures specified at the initiation of test.

Data sheet of IC74LS191

Connection Diagram



Timing Diagram



Absolute Maximum Ratings (Note 1)

Storage Temperature Range	−65°C to +150°C
Input Voltage	7V
Operating Free Air Temp. Range	0°C to +70°C
Supply Voltage	7V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)		0		20	MHz
t_W	Pulse Width	Clock	25			ns
	(Note 2)	Load	35			
t_{SU}	Data Setup Time (Note 2)		20			ns
t_H	Data Hold Time (Note 2)		0			ns
t_{EN}	Enable Time to Clock (Note 2)		30			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

DC Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output	V_{CC} = Min, I_{OH} = Max	Mil	2.5	3.4		
	Voltage	V_{IL} = Max, V_{IH} = Min	Com	2.7	3.4		V
V_{OL}	LOW Level Output	V_{CC} = Min, I_{OL} = Max			0.25	0.4	
	Voltage	V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max	V_{CC} = Max	Enable			0.3	mA
	Input Voltage	V_I = 7V	Others			0.1	
I_{IH}	HIGH Level Input	V_{CC} = Max	Enable			60	µA
	Current	V_I = 2.7V	Others			20	
I_{IL}	LOW Level Input	V_{CC} = Max	Enable			−1.08	mA
	Current	V_I = 0.4V	Others			−0.4	
I_{OS}	Short Circuit	V_{CC} = Max	Mil	−20		−100	mA
	Output Current	(Note 4)	Com	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			20	35	mA

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

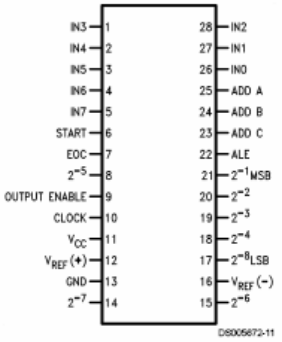
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all inputs grounded and all outputs open.

Data sheet of IC74LS191

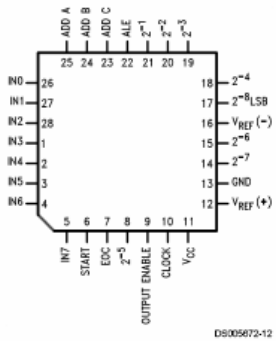
Connection Diagrams

Dual-In-Line Package



Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C			−55°C to +125°C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC}+0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1, 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CCN,ADC0809CCN	−40°C≤T_A≤+85°C
ADC0808CCV, ADC0809CCV	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	µA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	µA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			µA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			µA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Data sheet of IC74LF198

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 2)	500 mW
Operating Ambient Temperature Range	
LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 3)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Note 4)	
H package (Soldering, 10 sec.)	260°C
N package (Soldering, 10 sec.)	260°C
M package:	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Thermal Resistance (θ_{JA}) (typicals)	
H package	215°C/W (Board mount in still air) 85°C/W (Board mount in 400LF/min air flow)
N package	115°C/W
M package	106°C/W
θ_{JC} (H package, typical)	20°C/W

Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \le V_{IN} \le +V_S - 3.5V$, $+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

Parameter	Conditions	LF198/LF298			LF398			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 5)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 5)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 6)	$T_j = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 5)	$T_j \ge 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	µA
Leakage Current into Hold Capacitor (Note 5)	$T_j = 25°C$, (Note 7) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000\ pF$		4			4		µs
	$C_h = 0.01\ \mu F$		20			20		µs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V
Input Offset Voltage, (Note 5)	$T_j = 25°C$		1	1		2	2	mV
	Full Temperature Range			2			3	mV
Input Bias Current, (Note 5)	$T_j = 25°C$		5	25		10	25	nA
	Full Temperature Range			75			50	nA

Data sheet of IC74LS164

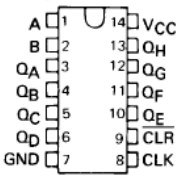
SN54164, SN54LS164, SN74164, SN74LS164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

MARCH 1974 – REVISED MARCH 1988

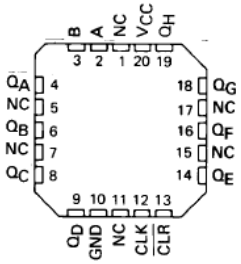
- **Gated Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Asynchronous Clear**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'164	36 MHz	21 mW per bit
'LS164	36 MHz	10 mW per bit

SN54164, SN54LS164 . . . J OR W PACKAGE
SN74164 . . . N PACKAGE
SN74LS164 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS164 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74164 and SN74LS164 are characterized for operation from 0°C to 70°C.

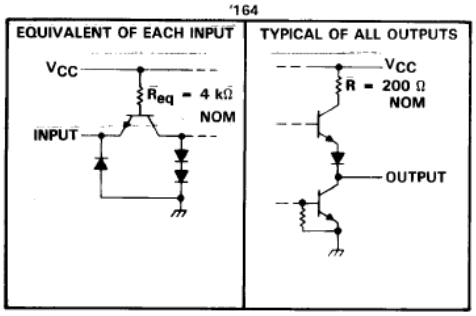
FUNCTION TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

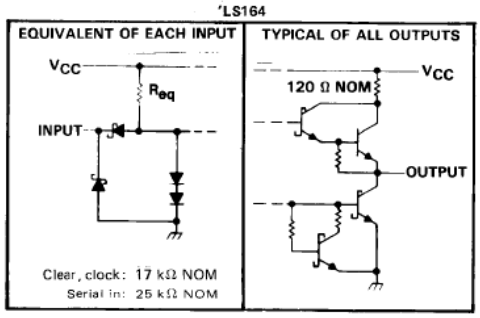
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

schematics of inputs and outputs

'164



'LS164



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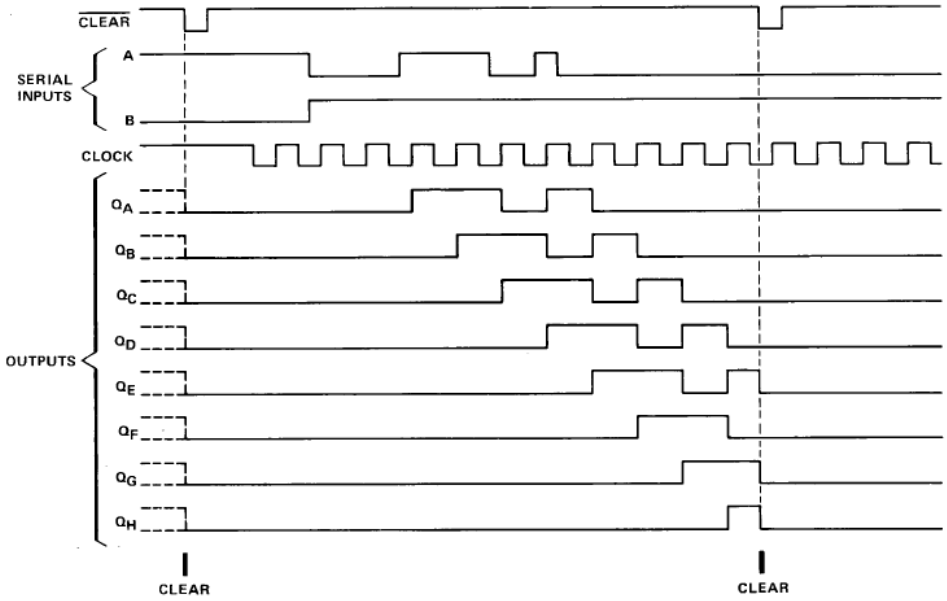
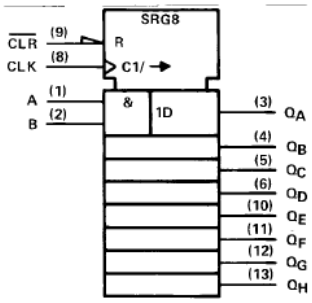
typical clear, shift, and clear sequences



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

XR-2206

Monolithic
Function Generator

EXAR ...the analog plus company™

June 1997-3

FEATURES

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C, Typ.
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V, Typ.
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2206M	16 Lead 300 Mil CDIP	-55°C to +125°C
XR-2206P	16 Lead 300 Mil PDIP	–40°C to +85°C
XR-2206CP	16 Lead 300 Mil PDIP	0°C to +70°C
XR-2206D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C

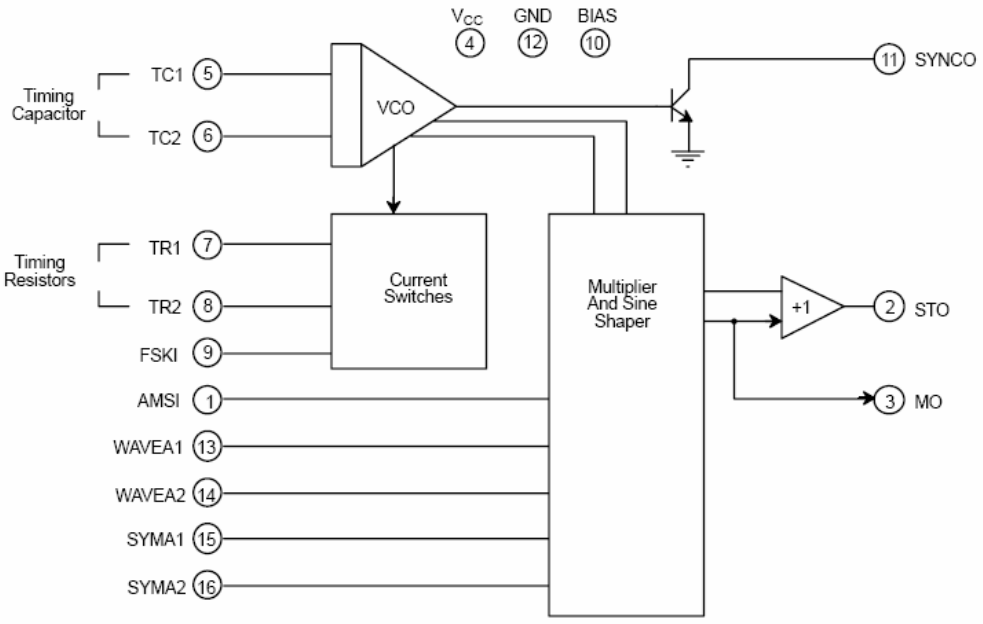
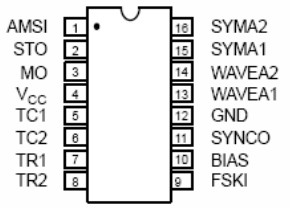
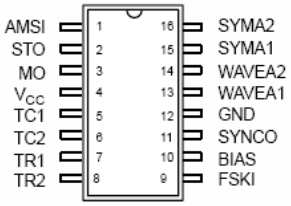


Figure 1. XR-2206 Block Diagram



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	AMSI	I	**Amplitude Modulating Signal Input.**
2	STO	O	**Sine or Triangle Wave Output.**
3	MO	O	**Multiplier Output.**
4	V_{CC}		**Positive Power Supply.**
5	TC1	I	**Timing Capacitor Input.**
6	TC2	I	**Timing Capacitor Input.**
7	TR1	O	**Timing Resistor 1 Output.**
8	TR2	O	**Timing Resistor 2 Output.**
9	FSKI	I	**Frequency Shift Keying Input.**
10	BIAS	O	**Internal Voltage Reference.**
11	SYNCO	O	**Sync Output.** This output is a open collector and needs a pull up resistor to V_{CC}.
12	GND		**Ground pin.**
13	WAVEA1	I	**Wave Form Adjust Input 1.**
14	WAVEA2	I	**Wave Form Adjust Input 2.**
15	SYMA1	I	**Wave Symetry Adjust 1.**
16	SYMA2	I	**Wave Symetry Adjust 2.**

Data sheet of IC555

FEATURES

- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

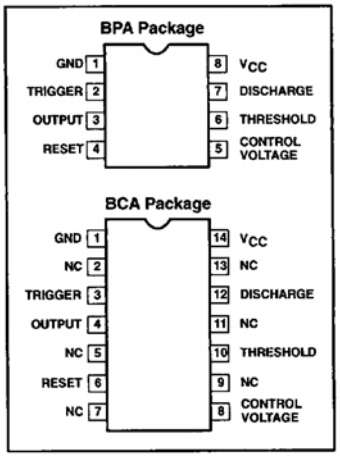
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

PIN CONFIGURATION

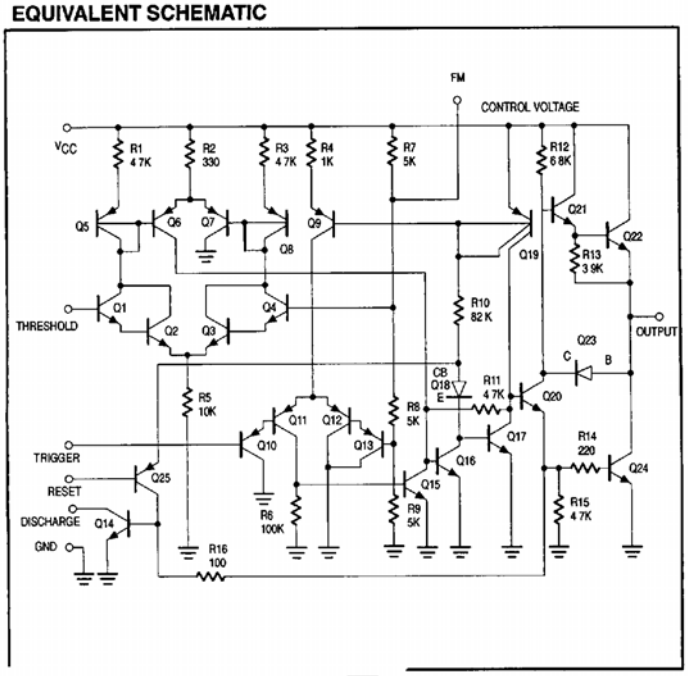


ORDERING INFORMATION

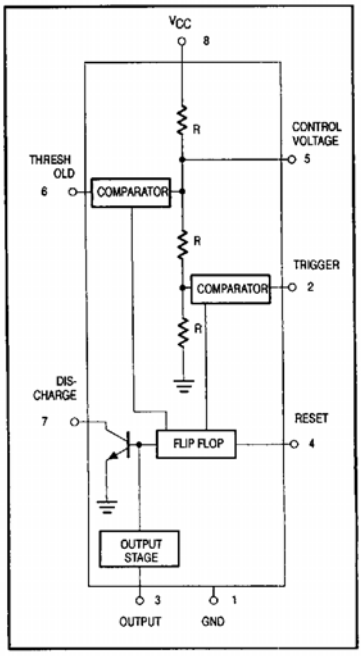
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
14-Pin Ceramic DIP	555/BCA	GDIP1-T14
8-Pin Ceramic DIP	555/BPA	GDIP1-T8

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

EQUIVALENT SCHEMATIC



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING[1]	UNIT
V_{CC}	Supply voltage	+18	V
P_D	Power dissipation	600	mW
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V to V_{CC} = +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	T_{amb} = +25°C			T_{amb} = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5		18	4.5		18	V
I_{CC}	Supply current (low state)[2]	V_{CC} = 5V, R_L = ∞		3	5			6	mA
		V_{CC} = 15V, R_L = ∞		10	12			14	mA
	Timing error (monostable)	R_A = 2kΩ to 100kΩ							
t_M	Initial accuracy[3]	C = 0.1µF		0.5	2.0			2.5	%
$\Delta t_M/\Delta T$	Drift with temperature[7, 8]							100	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2			0.25	%/V
	Timing error (astable)	R_A, R_B = 1kΩ to 100kΩ							
t_A	Initial accuracy[3]	C = 0.1µF		4	6			10.0	%
$\Delta t_A/\Delta T$	Drift with temperature[7]	V_{CC} = 15V						500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage[9]			0.15	0.6			1.5	%/V
V_C	Control voltage level	V_{CC} = +15V	9.6	10.0	10.4	9.6		10.4	V
		V_{CC} = +5V	2.9	3.33	3.8	2.9		3.8	V
V_{TH}	Threshold voltage	V_{CC} = +15V	9.4	10.0	10.6	9.4		10.6	V
		V_{CC} = +5V	2.7	3.33	4.0	2 4		4.0	V
I_{TH}	Threshold current[4]	V_{TH} = 10.6V		0.1	0.25			0.35	mA
V_{TRIG}	Tngger voltage	V_{CC} = +15V	4.8	5.0	5.2	4.5		5.5	V
		V_{CC} = +5V	1.45	1.67	1.9	1.5		2.2	V
I_{TRIG}	Trigger current	V_{TRIG} = 0V		0.5	0.9			2.0	µA
V_{RESET}	Reset voltage[5]		0.3		1.0	0.1		1.3	V
I_{RESET}	Reset current	V_{RESET} = 0.4V		-0.1	-0.4			-0.6	mA
I_{RESET}	Reset current	V_{RESET} = 0V		-0.4	-1.0			-1.2	mA
v_{OL}	Output voltage (low)[10]	V_{CC} = +15V							
		I_{SINK} = 10mA		0.1	0.15			0.25	V
		I_{SINK} = 50mA		0.4	0.5			0.70	V
		I_{SINK} = 100mA		2.0	2.2			2.6	V
		V_{CC} = +5V							
		I_{SINK} = 8mA		0.1	0.25			0.43	V
		I_{SINK} = 5mA		0.05	0.2			0.38	V
V_{OH}	Output voltage (high)[10]	V_{CC} = +15V							
		I_{SOURCE} = 100mA	13.0	13.3		12.5			V
		V_{CC} = +5V							
		I_{SOURCE} = 100mA	3.0	3.3		2.6			V
I_D	Discharge leakage current			20	100			500	nA

Data sheet of ICCD4051

National Semiconductor

October 1989

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD}=5V$, $V_{SS}=0V$ and $V_{EE}=-5V$, analog signals from $-5V$ to $+5V$ can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

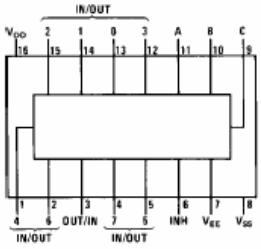
Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD}-V_{EE}=15V$
- High "OFF" resistance: channel leakage of ± 10 pA (typ.) at $V_{DD}-V_{EE}=10V$
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD}-V_{SS}=3-15V$) to switch analog signals to 15 V_{p-p} ($V_{DD}-V_{EE}=15V$)
- Matched switch characteristics: $\Delta R_{ON}=5\Omega$ (typ.) for $V_{DD}-V_{EE}=15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V$
- Binary address decoding on chip

Connection Diagrams

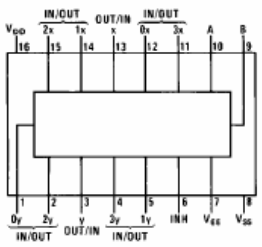
Dual-In-Line Packages

CD4051BM/CD4051BC



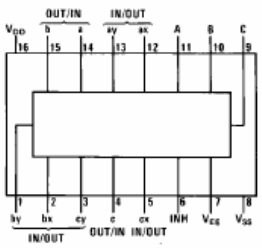
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW

TL/F/5662–1

Order Number CD4051B, CD4052B, or CD4053B

DC Electrical Characteristics (Note 2) (Continued)

Symbol	Parameter	Conditions		−40°C		+25°C			+85°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{IN}	Input Current	$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=0V$			−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=15V$			0.1		10^{-5}	0.1		1.0	μA
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			20			20		150	μA
		$V_{DD}=10V$			40			40		300	μA
		$V_{DD}=15V$			80			80		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \le V_{IS} \le V_{DD}$)	$R_L=10$ kΩ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		850		270	1050		1200	Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		330		120	400		520	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		210		80	240		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10$ kΩ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, $V_{EE}=-7.5V$ O/I = ±7.5V, I/O = 0V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V	CD4051		±200		±0.08	±200		±2000	nA
		$V_{DD}=7.5V$, $V_{EE}=-7.5V$, O/I = 0V	CD4052		±200		±0.04	±200		±2000	nA
		I/O = ±7.5V	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1$ kΩ to V_{SS} $I_{IS}<2$ μA on all OFF Channels $V_{IS}=V_{DD}$ thru 1 kΩ									
		$V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V
I_{IN}	Input Current	$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=0V$			−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=15V$			0.1		10^{-5}	0.1		1.0	μA

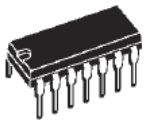
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

LM139,A
LM239,A-LM339,A

LOW POWER QUAD VOLTAGE COMPARATORS

- WIDE SINGLE SUPPLY VOLTAGE RANGE OR DUAL SUPPLIES FOR ALL DEVICES : +2V TO +36V OR ±1V TO ±18V
- VERY LOW SUPPLY CURRENT (1.1mA) INDEPENDENT OF SUPPLY VOLTAGE (1.4mW/comparator at +5V)
- LOW INPUT BIAS CURRENT : 25nA TYP
- LOW INPUT OFFSET CURRENT : ±5nA TYP
- LOW INPUT OFFSET VOLTAGE : ±1mV TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250mV TYP. (I_O = 4mA)
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE SUPPLY VOLTAGE
- TTL, DTL, ECL, MOS, CMOS COMPATIBLE OUTPUTS



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

P
TSSOP14
(Thin Shrink Small Outline Package)

DESCRIPTION

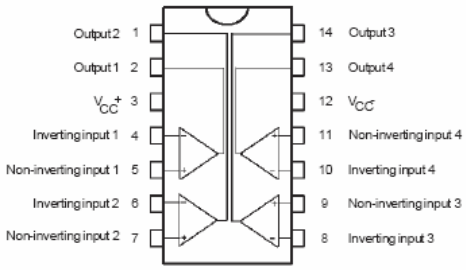
These devices consist of four independent precision voltage comparators with an offset voltage specifications as low as 2mV max for LM339A, LM239A and LM139A. All these comparators were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

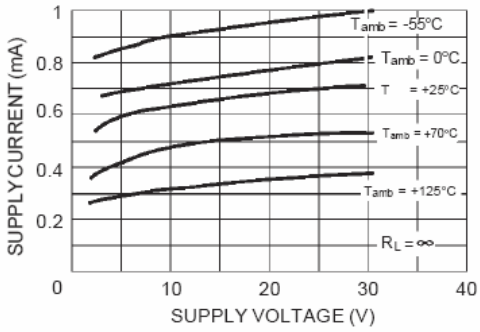
ORDER CODES

Part Number	Temperature Range	Package		
		N	D	P
LM139,A	-55, +125°C	•	•	•
LM239,A	-40, +105°C	•	•	•
LM339,A	0, +70°C	•	•	•
Example : LM139AN				

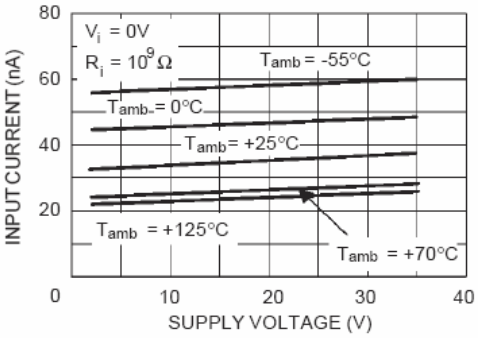
PIN CONNECTIONS (top view)



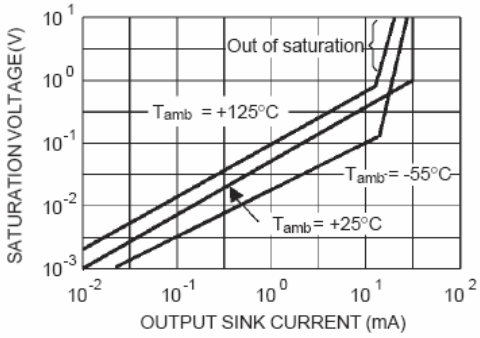
SUPPLY CURRENT versus
SUPPLY VOLTAGE



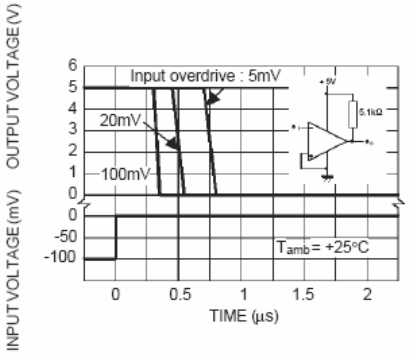
INPUT CURRENT versus
SUPPLY VOLTAGE



OUTPUT SATURATION VOLTAGE
versus OUTPUT CURRENT



RESPONSE TIME FOR VARIOUS INPUT
OVERDRIVES - NEGATIVE TRANSITION



Data sheet of ICLM565

May 1999

National Semiconductor

LM565/LM565C
Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system — bandwidth, response speed, capture and pull in range — may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CN is specified for operation over the 0°C to +70°C temperature range.

Features

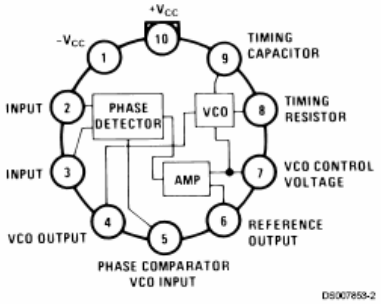
- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%

Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

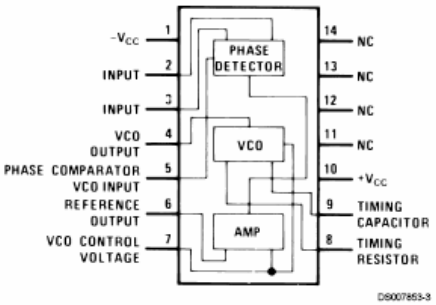
Connection Diagrams

Metal Can Package



Order Number LM565H
See NS Package Number H10C

Dual-in-Line Package



Order Number LM565CN
See NS Package Number N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±12V
Power Dissipation (Note 2)	1400 mW
Differential Input Voltage	±1V
Operating Temperature Range	
LM565H	−55°C to +125°C
LM565CN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

AC Test Circuit, T_A = 25°C, V_{CC} = ±6V

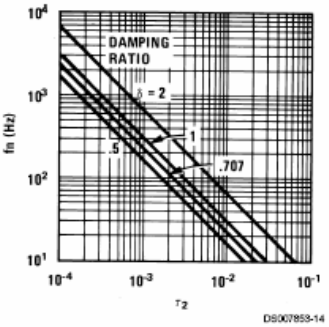
Parameter	Conditions	LM565			LM565C			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	C_o = 2.7 pF	300	500		250	500		kHz
VCO Free-Running Frequency	C_o = 1.5 nF R_o = 20 kΩ f_o = 10 kHz	−10	0	+10	−30	0	+30	%
Operating Frequency Temperature Coefficient			−100			−200		ppm/°C
Frequency Drift with Supply Voltage			0.1	1.0		0.2	1.5	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2			0.5		%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	f_o = 10 kHz		6600			6600		Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	400	200	300	450	mV_{p-p}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\lvert V_7 - V_6 \rvert$			30	100		50	200	mV
Temperature Drift of $\lvert V_7 - V_6 \rvert$			500			500		µV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D			0.68			0.68		V/radian

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

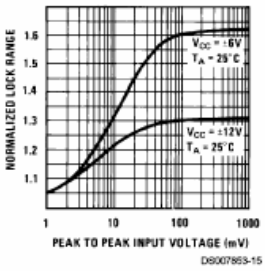
Note 2: The maximum junction temperature of the LM565 and LM565C is +150°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W junction to ambient or +45°C/W junction to case. Thermal resistance of the dual-in-line package is +85°C/W.

Typical Performance Characteristics

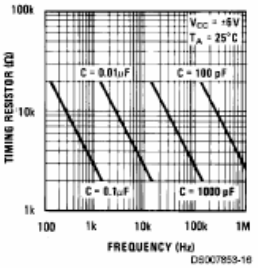
Power Supply Current as a Function of Supply Voltage



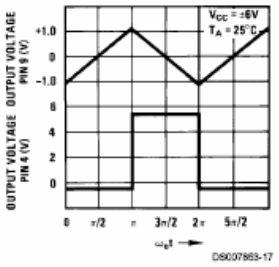
Lock Range as a Function of Input Voltage



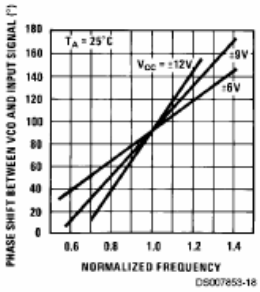
VCO Frequency



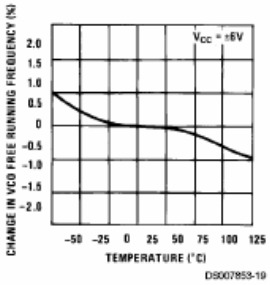
Oscillator Output Waveforms



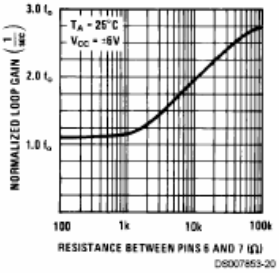
Phase Shift vs Frequency



VCO Frequency as a Function of Temperature



Loop Gain vs Load Resistance



Hold in Range as a Function of R_{8-7}