SRM UNIVERSITY
FACULTY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTER APPLICATIONS
COURSE PLAN

Course Code : MC0505
Course Title : Digital Computer Fundamentals
Semester : I
Course Time : September - December 2012

Day	D	
	Hour	Timing
I	1	8.45 am – 9.35 am
II	3	10.35 am – 11.25 am
II	5	1.30 pm – 2.20 pm
III	1	8.45 am – 9.35 am

Location :- Tech Park Second Floor
Faculty Details

Sec.	Name	Office	Office hour	Mail id
B	Mr.A. PANDIAN	MCA Staff Room 206 A (East Wing)	Monday to Friday	pandianmtech@gmail.com

Required Books:
1. Bartee T.C. – Digital Computer Fundamentals – McGraw Hill – 6th Edition – 1985
2. Morris Mano M – Digital Logic and Computer Design – Prentice Hall India – 4th Edition – 2000
3. Malvino Leach – Digital Principles and Applications – McGraw Hill – 4th Edition 1986
4. Vijayendran V – Digital Fundamentals – S.V. Publishers – 1st Edition - 2003

Web resources
http://zebu.uoregon.edu/~rayfrey/432/DigitalNotes.pdf
http://www.asic-world.com/digital/tutorial.html
http://en.wikipedia.org/wiki/Digital_electronics

Prerequisite
1. Basic Electronics 2. Discrete Mathematics

Objectives
- To train the students on fundamentals of Digital basics
- To train the students to lay a strong foundation for digital systems.

Assessment Details

Announced Quiz	:	10 Marks
Cycle Test – I	:	20 Marks
Unannounced Quiz	:	10 Marks
Model Exam	:	20 Marks
Assignment	:	10 Marks

Test Schedule

S.No.	DATE	TEST	TOPICS	DURATION
1	12.10.2012	Cycle Test - I	Unit I & II	2 periods
2	22.11.2012	Model Exam	All 5 units	3 Hrs

Outcomes

Students who have successfully completed this course will have full understanding of the following concepts

Course outcome	**Program outcome**
To learn the Number Systems	To understand and operate on various number systems
To Know Boolean algebra and K-map	To minimize Boolean equations
To understand combinational circuits	To understand the working of combinational circuits.
To know the concept of sequential circuits	To understand the working of combinational circuits.
Understand the concept of ALU	To understand the concepts of digital systems

Detailed Session Plan

Overview of Number Systems: Number Systems – Conversions – Arithmetic – Logic Gates.					
Session No.	**Topics to be covered**	**Time (min)**	**Ref**	**Teaching Method**	**Testing Method**
1	Binary number system, Binary to decimal & decimal to binary conversion	50	1	BB	Discussion
2	Hexadecimal number system, Hexa to decimal & Decimal to Hexa conversion	50	1	BB	Discussion
3	Hexa to binary & Binary to Hexa conversion	50	1	BB	Group discussion
4	Octal Number system, Octal to decimal & Decimal to Octal conversion	50	1	BB	Discussion
5	Octal to binary & Binary to Octal Conversion	50	1	BB	Comparative Study
6	Basic Gates: AND , OR, NOT	50	1	BB	Assignment
7	Logic Circuits and logic expressions	50	1	BB	Comparative Study
8	SOP and POS	50	1	BB	Group discussion
9	NAND, NOR, EX-OR and EX-NOR	50	1	BB	Comparative Study
Boolean Algebra and K-Map: Boolean Algebra – Axioms and Theorems – Simplification of Boolean Functions – Karnaugh Map – Mc Clausky Method					
10	Laws of Boolean Algebra	50	1	BB	Discussion

11	DeMaorgan's Theorems	50	1	BB	Discussion
12	Simplification of Boolean Functions	50	1	BB	Assignment
13	NAND as Universal Gate	50	1	BB	Group discussion
14	Karnaugh Map	50	1	BB	Group discussion
15	Don't Care conditions	50	1	BB	Discussion
16	Simplification using K-Map	50	1	BB	Discussion
17	Mc Clausky Method	50	1	BB	Group discussion
18	Simplification using Mc Clausky Method	50	1	BB	Announced Quiz
Combinational Circuits: Adders – Sub tractors – Decoders – Encoders – Multiplexers – Demultiplexers – Flip Flops.					
16	Binary addition & Half adder	50	1	BB	Group discussion
17	Full adder & Four bit binary adder	50	1	BB	Discussion
18	BCD adder & Half subtractor	50	1	BB	Assignment
19	Full subtractor	50	1	BB	Discussion
20	Multiplexer	50	1	BB	Assignment
21	Demultiplexer	50	1	BB	Discussion
22	Decoder & Encoder	50	1	BB	Discussion
23	SR Flip-flop & D Flip-flop	50	1	BB	Discussion
24	JK Flip-flop & T Flip flop	50	1	BB	Discussion
Sequential Circuits: Registers- Shift Registers – Counters – Ripple Counters – BCD Counters – Synchronous counters-Counter Design.					
25	Registers	50	1	BB	Discussion
26	Shift Registers	100	1	BB	Discussion
27	Asynchronous counters	50	1	BB	Discussion
28	Synchronous counters	50	1	BB	Discussion
29	Ring counter	50	1	BB	Discussion
30	Design of synchronous counters	100	1	BB	Discussion
31	Summary	50	1	BB	Unannounced Quiz
ALU: Design of Arithmetic Unit – Logic Unit – Design of ALU – Control Unit.					
35	Introduction	50	1	BB	Group discussion
36	Design of Arithmetic Unit	100	1	BB	Discussion
37	Logic Unit	100	1	BB	Discussion
38	Design of ALU	100	1	BB	Discussion
39	Control Unit.	100	1	BB	Test