LIST OF EXPERIMENTS

- 1. Verification of KVL & KCL
- 2. Verification of Thevenin's Theorem
- 3. Verification of Norton's Theorem
- 4. Verification of Superposition Theorem
- 5. Verification of Reciprocity Theorem
- 6. Verification of Compensation Theorem
- 7. Verification of Maximum Power Transfer Theorem
- 8. Rectifier Circuits
- 9. Clipping Circuits
- **10. Clamping Circuits**
- 11. RC Phase Shift Oscillator

VERIFICATION of KCL & KVL THEOREM

AIM:

To Verify KCL & KVL from the given circuit

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistor	1 ΚΩ	3
3	Ammeter	0-25 mA	3
4	Voltmeter	0-30 V	2
5	RPS	0-30 V	1

THEORY:

Kirchhoff's Voltage Law (KVL) states that the algebraic sum of all branch voltages around any closed path in a circuit is always zero at all instants of time. In the figure 1.1, if KVL is applied then the equation is

 $V_s = V_1 + V_2 + V_3$

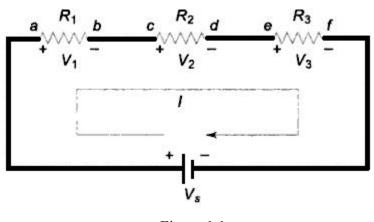


Figure 1.1

Kirchhoff's Current Law (KCL) states that the sum of the currents entering into any node/point/junction is equal to the sum of the currents leaving that node/point/junction. In the figure 1.2, if KCL is applied then the equation is

 $I_T = I_1 + I_2 + I_3$

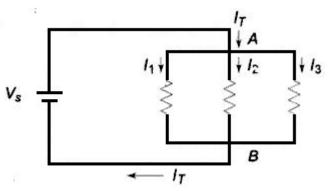
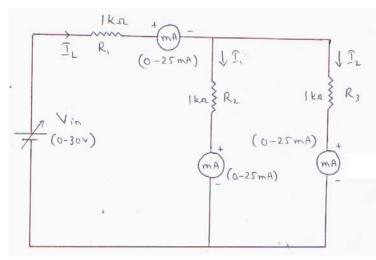


Figure 1.2

- a. Verification of KCL
- 1. Give the connection according to circuit shown in figure 1.3
- 2. Vary the supply voltage and take the corresponding readings of I_L , $I_1 \& I_2$ from the ammeter.
- 3. Verify the reading.
- b. Verification of KVL
- 1. Connection are made as per the circuit diagram shown in figure 1.4
- 2. Vary the supply voltage and take the corresponding readings $V_1 \& V_2$ from the voltmeter.
- 3. Verify the reading.





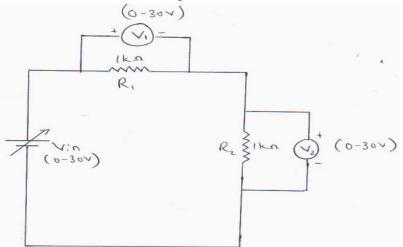


Figure 1.4

Tabulation:

Table 1(for KCL):

Vin	I ₁ (n	nA)	I ₂ (1	nA)	$I_{L} = I_{1} +$	I_2 (mA)
(v)	Theoretical	Practical	Theoretical	Practical	Theoretical	Practical

Table 2 (for KVL):

Vin	V_1	(v)	V ₂	(v)	$\mathbf{V}_{in} = \mathbf{V}_1$	$+V_{2}(v)$
(v)	Theoretical	Practical	Theoretical	Practical	Theoretical	Practical

Note: All theoretical values can be found by using either mesh analysis or nodal analysis and also using voltage division rule and current division rule where it is applicable.

VERIFICATION of THEVENIN'S THEOREM

AIM:

To find the Thevenin's equivalent circuit from the given circuit.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistor	1 KΩ	3
3	Resistor	2.2 ΚΩ	2
4	Resistor	4.7 ΚΩ	1
5	Ammeter	0-100 mA	1
6	Voltmeter	0-30 V	1
7	RPS	0-30 V	1

THEORY:

Thevenin's theorem states that any two terminal linear network having a number of voltage current sources and resistances can be replaced by a simple equivalent circuit consisting of a single voltage source in series with a resistance, where the value of the voltage source is equal to the open circuit voltage across the two terminals of the network, and resistance is equal to the equivalent resistance measured between the terminals with all the energy sources are replaced by their internal resistances.

- 1. Connection are made as per the circuit diagram shown in figure 2.1
- 2. Vary the supply voltage V_1 and take the corresponding reading I_3 from the ammeter.
- 3. Now connect the circuit diagram in figure 2.2 in bread board (Removing the load resistor R_{6}).
- 4. Vary the supply voltage V_1 in the same way as done in step 2 and note down the corresponding V_{AB} or V_{TH} from the voltmeter.
- 5. Find out the R_{TH} and draw the Thevenin equivalent ciruit.

6. Now connect the circuit diagram in figure 2.3 in bread board and note down the I_L value by varying V_{TH} (fix the values of V_{TH} got from step 4).

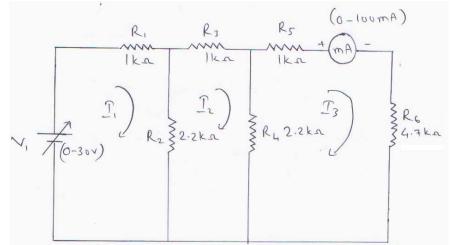


Figure 2.1

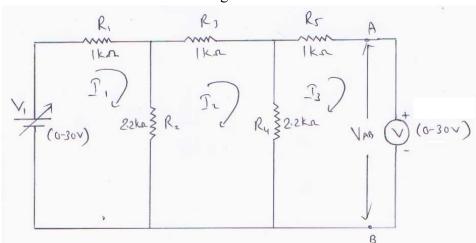
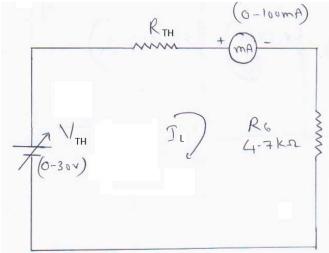


Figure 2.2





Tabulation:

Table 1(for I_3 & V_{TH} or V_{AB}):

V1 (v)	I ₃ (1	mA)	$V_{TH}(v)$		
	Theoretical	Practical	Theoretical	Practical	

Table 2 (for I_L):

$V_{TH}(v)$	$I_{L}(mA)$		
(practical)	Theoretical	Practical	

Note: All theoretical values can be found by using either mesh analysis or nodal analysis and also using voltage division rule and current division rule where it is applicable.

VERIFICATION of NORTON'S THEOREM

AIM:

To find the Norton's equivalent circuit from the given circuit.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistor	1 KΩ	3
3	Resistor	2.2 KΩ	2
4	Resistor	4.7 ΚΩ	1
5	Ammeter	0-100 mA	1
6	Voltmeter	0-30 V	1
7	RPS	0-30 V	1

THEORY:

Norton's theorem states that any two terminal linear network with current sources, voltage sources and resistances can be replaced by an equivalent circuit consisting of a current source in parallel with a resistance. The value of the current source is the short circuit current between the two terminals of the network and the resistance is equal to the equivalent resistance measured between the terminals with all the energy sources are replaced by their internal resistances.

- 1. Connection are made as per the circuit diagram shown in figure 3.1
- 2. Vary the supply voltage V_1 and take the corresponding reading I_3 from the ammeter.
- 3. Now connect the circuit diagram in figure 3.2 in bread board (Removing the load resistor R₆ and shorting the terminals).
- 4. Vary the supply voltage V_1 in the same way as done in step 2 and note down the corresponding I_N from the ammeter.
- 5. Find out the R_N and draw the Norton's Equivalent circuit

- 6. Now apply source transformation in the circuit diagram as shown in figure 3.3 and obtain the circuit as shown in figure 3.4.
- 7. Connect the circuit as shown in figure 3.4 in bread board and vary the supply voltage and note down the corresponding I_L from the ammeter.

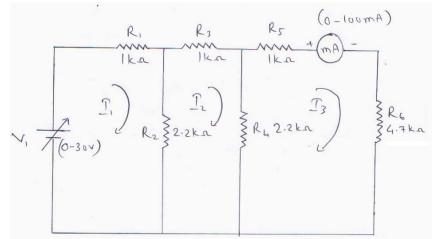


Figure 3.1

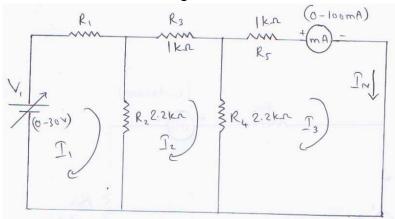
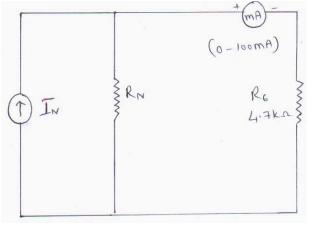


Figure 3.2





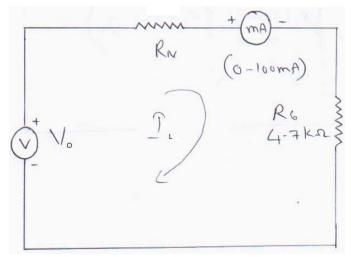


Figure 3.4

Tabulation:

Table 1(for $I_3 \& I_N$):

$\mathbf{V}_{1}(\mathbf{x})$	I ₃ (1	mA)	I _N (1	mA)
V1 (v)	Theoretical	Practical	Theoretical	Practical

Table 2 (for I_L):

$V_{o}(v)$	$I_{L}(mA)$				
	Theoretical	Practical			

Note: All theoretical values can be found by using either mesh analysis or nodal analysis and also using voltage division rule and current division rule where it is applicable.

VERIFICATION of SUPERPOSITION THEOREM

AIM:

To verify the superposition theorem in the given network.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistor	1 KΩ	2
3	Resistor	2.2 ΚΩ	2
4	Ammeter	0-25 mA	1
5	Voltmeter	0-30 V	1
6	RPS	0-30 V	1

THEORY:

The superposition theorem states that in any linear network containing two or more sources, the response in any element is equal to the algebraic sum of the responses caused by individual sources acting alone, while the other sources are nonoperative; that is, while considering the effect of individual sources, other ideal voltage sources and ideal current sources in the network are replaced by short circuit and open circuit across their terminals.

- 1. Connection are made as per the circuit diagram shown in figure 4.1
- 2. Vary the supply voltage V_{S1} & V_{S2} and take the corresponding reading I_2 from the ammeter.
- 3. Now V_{S2} is short circuited. Vary V_{S1} & take the corresponding reading I_2^{-1} from the ammeter as shown in figure 4.2
- 4. Now V_{S1} is short circuited. Vary V_{S2} & take the corresponding reading I_2^{11} from the ammeter as shown in figure 4.3
- 5. Finally Verify whether $I_2 = I_2^{1} + I_2^{11}$

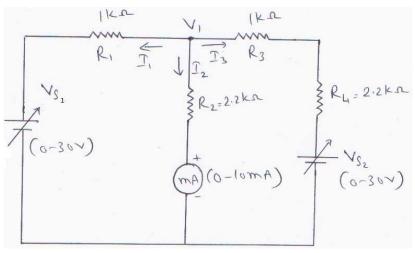


Figure 4.1

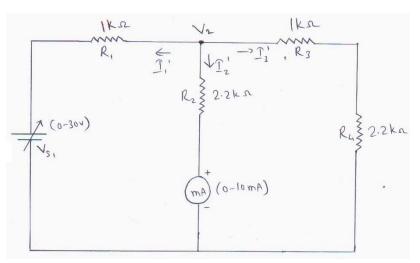


Figure 4.2

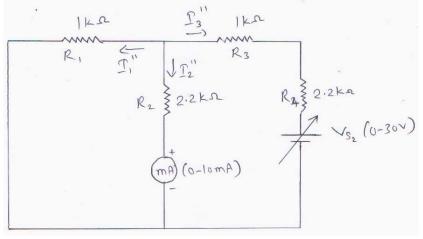


Figure 4.3

Tabulation:

Table 1(for I_2):

V_{S1}	V_{S2}	$I_2 (mA)$			
V _{S1} (v)	V _{S2} (v)	Theoretical	Practical		

Table 2 (for $I_2^{\ 1} \& I_2^{\ 11}$):

V_{S1} acting alone, V_{S2} replaced by internal Resistance (v)			V _{S2} acting alone, V _{S1} replaced by internal Resistance (v)		Total I ₂ (mA) I ₂ = I ₂ ¹ + I ₂ ¹¹		
$V_{S1}(v)$ $I_2^{-1}(mA)$		V _{S2} (v)	$I_2^{11}(mA)$		Theoretical	Practical	
	Theoretical	Practical		Theoretical	Practical		

Note: All theoretical values can be found by using either mesh analysis or nodal analysis and also using voltage division rule and current division rule where it is applicable.

VERIFICATION of RECIPROCITY THEOREM

AIM:

To verify Reciprocity theorem for a given network.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistor	1 KΩ	3
3	Resistor	2.2 KΩ	3
4	Ammeter	0-10 mA	1
5	Voltmeter	0-30 V	1
6	RPS	0-30 V	1

THEORY:

In any linear bilateral network, if a single voltage source V_a in branch 'a' produces a current I_b in branch 'b', then if the voltage source V_a is removed and inserted in branch 'b' will produce a current I_b in branch 'a'. The ratio of response to excitation is same for the two conditions mentioned above. This is called the reciprocity theorem.

Consider the network shown in figure 5.1. AA^1 denotes input terminals and BB^1 denotes output terminals. The application of voltage V across AA^1 produces current I at BB^1 . Now if the position of source and responses are interchanged, by connecting the voltage source across BB^1 , the resultant current I will be at terminals AA^1 . According to Reciprocity theorem, the ratio of response to excitation is the same in both cases.

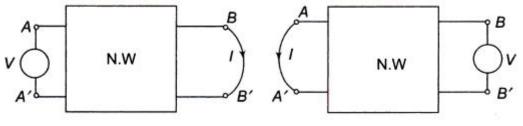


Figure 5.1

- 1. Connection are made as per the circuit diagram shown in figure 5.2
- 2. Vary the supply voltage V_1 and take the corresponding reading I_3 from the ammeter.
- 3. Find out the ratio $R = (V_1/I_3)$
- 4. Now interchange the position of ammeter and Variable voltage supply V_1 as shown in figure 5.3.
- 5. Vary the supply voltage V_1 and take the corresponding reading I_3^{11} from the ammeter.
- 6. Find out the ratio $R^1 = (V_1/I_3^1)$
- 7. Now check whether R and R^1 are same.

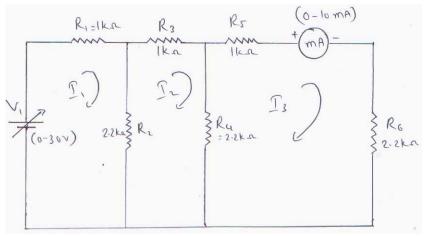


Figure 5.2

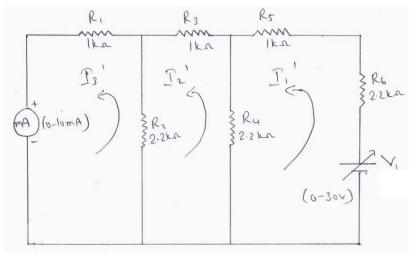


Figure 5.3

Tabulation:

Table 1(for I_3):

$\mathbf{V}_{1}(\mathbf{x})$	$I_3 (mA)$		$\mathbf{R} = (\mathbf{V}_1 / \mathbf{I}_3) \ (\mathbf{\Omega})$	
V1 (v)	Theoretical	Practical	Theoretical	Practical

Table 2 (for $I_3^{\ l}$):

VI (II)	I_3^1 (mA)		$\mathbf{R}^{1} = (\mathbf{V}_{1}/\mathbf{I}_{3}^{1}) (\mathbf{\Omega})$	
V1 (v)	Theoretical	Practical	Theoretical	Practical

Note: All theoretical values can be found by using either mesh analysis or nodal analysis and also using voltage division rule and current division rule where it is applicable.

VERIFICATION of COMPENSATION THEOREM

AIM:

To verify Compensation theorem for the given network.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistor	1 KΩ	3
3	DRB	-	1
4	Ammeter	0-25 mA	1
5	Voltmeter	0-30 V	1
6	RPS	0-30 V	1

THEORY:

The compensation theorem states that any element in the linear, bilateral network, may be replaced by a voltage source of magnitude equal to the current passing through the element multiplied by the value of the element, provided the currents and voltages in other parts of the circuit remain unchanged. Consider the circuit shown in figure 6.1. The element R can be replaced by voltage source V, which is equal to the current I passing through R multiplied by R as shown below.

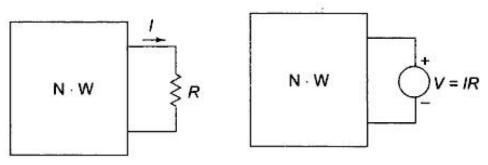


Figure 6.1

This theorem is useful in finding the changes in current or voltage when the value of resistance is changed in the circuit as shown in figure 6.2

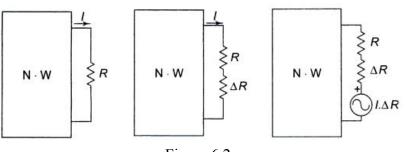


Figure 6.2

- 1. Connection are made as per the circuit diagram shown in figure 6.3
- 2. Set the supply voltage $V_1 = 15$ V and take the corresponding reading I_3 from the ammeter.
- 3. Now connect the additional resistor (DRB) as shown in figure 6.4
- 4. Now fixing $V_1 = 15$ V and finding out the current I_3^{-1} due to extra resistor DRB where Decade Resistance Box value is changed correspondingly.
- 5. Now replace the voltage V_1 by compensated voltage V_2 as shown in figure 6.5 and find out the current I_3^{11} due to compensated voltage V_2
- 6. Finally find the Ammeter Reading $I = I_3 I_3^{11}$

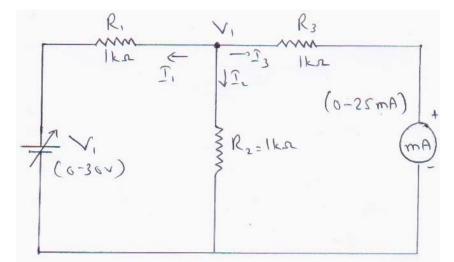
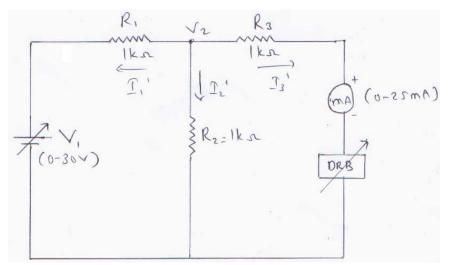


Figure 6.3





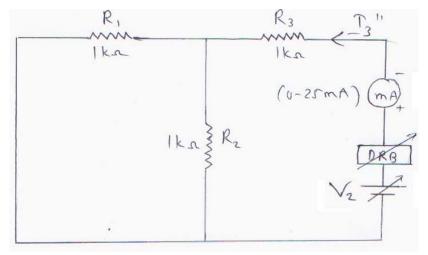


Figure 6.5

Tabulation:

Table 1(for I_3):

$\mathbf{V}_{1}(\mathbf{x})$	I ₃ (mA)		
V1 (v)	Theoretical	Practical	
15			

Table 2 (for $I_3^{\ l}$):

R _{add}	$I_{3}^{1}(mA)$		
(KΩ)	Theoretical	Practical	
1 2 3 4 5			

Table 3 (for I_3^{11}):

$V_2 =$	I_{3}^{11} (mA)	
I_3R_{add} (v)	Theoretical	Practical

Table 4 (for Ammeter Reading):

I ₃ (mA)	I_{3}^{11} (mA)	Ammeter Reading $I = I_3 - I_3^{11}$ (mA)

Note: All theoretical values can be found by using either mesh analysis or nodal analysis and also using voltage division rule and current division rule where it is applicable.

VERIFICATION of MAXIMUM POWER TRANSFER THEOREM

AIM:

To verify Maximum Power Transfer Theorem.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistors	470 Ω, 750 Ω	1 Each
3	Resistors	560 Ω, 330 Ω	1 Each
4	Ammeter	0-10 mA	1
5	Voltmeter	0-30 V	1
6	RPS	0-30 V	1
7	DRB	-	1

THEORY:

Maximum power transfer theorem states that the maximum power is delivered from a source to a load when the load resistance is equal to the source resistance. Depending upon the conditions of the circuit, there are three cases:

CASE 1: (Purely Resistive circuit & Load resistance is variable) - "Maximum power is delivered from a source to a load when the load resistance is equal to the source resistance". ($R_L = R_S$)

CASE 2: (Reactants present & load resistance and reactance can be independently varied) - "Maximum power is delivered from a source to a load when the load impedance is the complex conjugate of source impedance". ($X_L = -X_S \& R_L = R_S$)

CASE 3: (Reactants present but only the magnitude of the load resistance can be varied) - "Maximum power is delivered from a source to a load when the magnitude of the load impedance is equal to the magnitude of source impedance".

PROCEDURE:

1. First find the Thevenin equivalent circuit for circuit shown in figure 7.1.

- 2. After finding R_{TH} & V_{TH} , vary the load resistance R_L (DRB) from the minimum value to maximum value (shown in figure 7.2).
- 3. Plot the graph between R_L & Power $(I_L^2 R_L)$ where, theoretical $I_L = [V_{TH}/(R_{TH}+R_L)]$
- 4. Finally verify that when $R_L = R_{TH}$, maximum power is delivered or not.

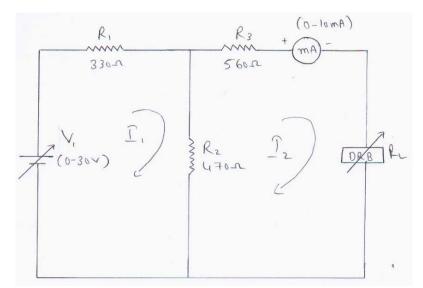
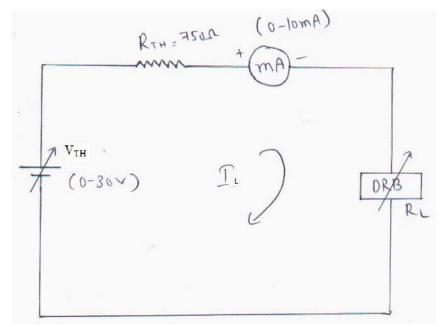
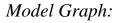
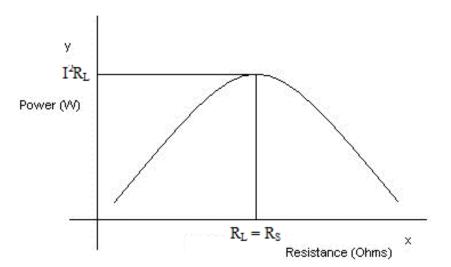


Figure 7.1









Tabulation:

Table 1:

$\mathrm{R}_{\mathrm{L}}\left(\Omega ight)$	I _L (mA)	$P = I_L^2 R_L$ (mW)

Note: All theoretical values can be found by using either mesh analysis or nodal analysis and also using voltage division rule and current division rule where it is applicable.

RECTIFIER CIRCUITS

AIM:

To study the characteristics of Half-wave rectifier & Full-wave rectifier

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistor	1 KΩ	1
3	Transformer	6-0-6	1
4	Diode	1N4007	1
5	CRO	-	1
6	Multimeter	-	1
7	Function Generator	-	1

THEORY:

Rectifier changes ac to dc and it is an essential part of a power supply. The unique property of a diode, permitting the current to flow in one direction, is utilized in rectifiers.

HALF WAVE RECTIFIER: Mains power supply is applied at the primary of the step down transformer. All the positive half cycles of the stepped down ac supply pass through the diode and all the negative half cycles get eliminated. Peak value of the output voltage is less than the peak value of the input voltage by 0.6 V because of the voltage drop across the diode.

For a half wave rectifier, $V_{rms} = V_m/2$ and $V_{dc} = V_m/\pi$ where $V_{rms} = rms$ value of the input, V_{dc} = Average value of input and V_m = peak value of the output. The ripple factor $r = V_{r,rms}/V_{dc}$ where $V_{r,rms}$ is the rms value of the ac component. $r = \{(V_{rms}/V_{dc})^2 - 1\}^{1/2} = 1.21$

FULL WAVE RECTIFIER: During the positive half cycle of the transformer secondary voltage, diode D_1 is forward biased and D_2 is reversed biased. So a current flows through the diode D_1 , load resistor R_L and upper half of the transformer winding. During the negative half cycle, diode D_2 becomes forward biased and D_1 becomes reverse biased. The current then flows through the diode D_2 , load resistor R_L and lower half of the transformer winding. Current flows

through the load resistor in the same direction during both the half cycles. Peak value of the output voltage is less than the peak value of the input voltage by 0.6 V because of the voltage drop across the diode.

For a full wave rectifier, $V_{rms} = V_m/1.414$, $V_{dc} = 2V_m/\pi$. Ripple factor $r = \{(V_{rms}/V_{dc})^2 - 1\}^{1/2} = 0.48$

- 1. The circuit of half wave rectifier is made as shown in figure 8.1 in bread board.
- 2. Switch on mains supply. Observe the transformer secondary voltage waveform and output voltage waveform across the load resistor, simultaneously on the CRO screen. Note down V_m & calculate V_{rms} & V_{dc}
- 3. Calculate the ripple factor using the expression and plot the waveform.
- 4. Repeat the above steps for full wave rectifier where the circuit of full wave rectifier is shown in figure 8.2.

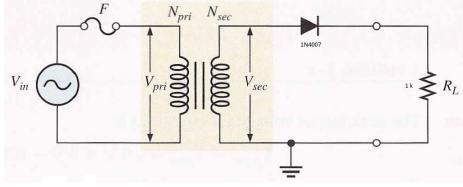
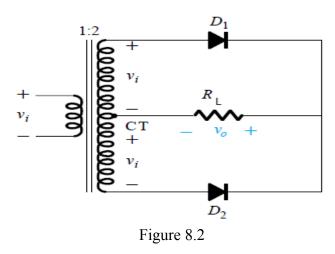
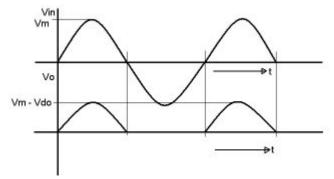


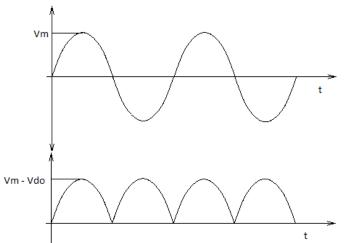
Figure 8.1



Model Graph: Half Wave Rectifier: V_{do} stands for voltage drop across the diode.



Full Wave Rectifier:



Tabulation:

Table 1:

Half Wave	$V_{m}(v)$	$V_{rms}(v)$	$V_{dc}(v)$	Ripple Factor r
Rectifier				
F 11 W	$V_{m}(v)$	$V_{rms}(v)$	$V_{dc}(v)$	Ripple Factor r
Full Wave Rectifier				

CLIPPING CIRCUITS

AIM:

To design, set up & study various shunt clipping circuits & series clipping circuits using diodes.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Resistor	3.3 KΩ	1
3	DC source	3 V	1
4	Diode	1N4007	1
5	CRO	-	1
6	Multimeter	-	1
7	Function Generator	-	1

THEORY:

Clipping circuits are non-linear wave shaping circuits. They are useful to clip off the positive or negative portions of an input waveform. It can be also used to slice off an input waveform between two voltage levels. The diode clippers can be classified as series and shunt clippers. The property of a diode as a switching device is utilized in clipping circuits. In the shunt clippers, output is taken parallel with the diode and in series clippers, output is taken in series with the diode. In other words, in the shunt clippers (parallel clippers), load comes in parallel with the diode and in series clippers, load comes in series with the diode.

Positive clipper clipping at 0 V: This circuit passes only negative going half waves of the input to the output. All the positive half cycles are bypassed through the diode to ground terminal because the diode gets forward biased when the input voltage becomes positive. Due to the voltage drop across the diode, the clipping occurs at +0.6 V.

Negative clipper clipping at 0 V: This circuit passes only positive going half waves of the input to the output. All the negative half cycles are bypassed through the diode to ground terminal because the diode gets forward biased when the input

voltage becomes negative. Due to the voltage drop across the diode, the clipping occurs at -0.6 V.

Positive clipper clipping at + 3V: Till the input becomes greater than + 3 V, diode is reverse biased and the input appears at the output. When input is greater than +3V, diode becomes forward biased and cell voltage appears at the output. Since the voltage drop across the diode develops in series with the cell, actual clipping level is at +3.6 V.

Positive clipper clipping at – 3V: Diode becomes reverse biased when the input voltage is less than – 3V and the input appears at the output. When the input is above – 3V, diode becomes forward biased and the cell voltage is available at the output since the voltage drop across the diode develops in series and opposite with the cell, actual clipping level is at – 2.4 V.

Negative clipper clipping at – 3V: When the input voltage becomes less than -3 V, diode becomes forward biased and the cell voltage becomes available at the output. When the input is greater than – 3 V, diode is reverse biased and the input appears at the output. Actual clipping level is at – 3.6 V, due to the voltage drop across the diode.

Negative clipper clipping at + 3V: Diode becomes reverse biased when the input voltage is greater than + 3V and the input appears at the output. When the input is below + 3V, diode becomes forward biased and the cell voltage is available at the output since the voltage drop across the diode develops in series and opposite with the cell, actual clipping level is at + 2.4 V.

Double clipper clipping at + 3V \& - 3 V: This circuit is the combination of positive and negative clippers. During the positive half cycle of the input, one branch is effective and the other remains open &vice versa during the negative half cycle. Actual clipping levels are + 3.6 V & - 3.6 V due to the diode drops.

Slicer: A slicer circuit is nothing but a two level clipper which has both clipping levels either in the positive or in negative part of the input signal. Consider the two level slicer with slicing levels at + 3V and +5V. This circuit allows the input signal pass to the output only between +3V & +5V. During the negative half cycle of the input, diode D₁ conducts & diode D₂ get reverse biased. The output voltage remains at +3V because the diode D₁ conducts when the input is less than +3V. During the positive half cycle of the input when input exceeds +3V, D₁ is reverse biased and input appears at the output. If the input exceeds +5 V, D₂ conducts and

the output remain at +5 V. When the diode drop is considered, actual clipping occurs at +2.4 V & +5.6 V.

Unbiased positive clipper: This circuit passes only negative going half waves of the input to the output. During the positive going half cycle of the input, diode turns off. Since 0.6V get dropped across the diode during conduction, amplitude of the output peak is reduced by 0.6 V.

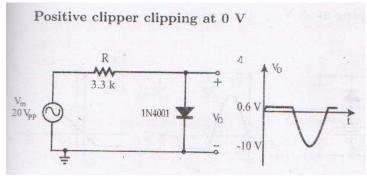
Unbiased negative clipper: This circuit passes only positive going half waves of the input to the output. During the negative going half cycle of the input, diode turns off. Amplitude of the output peak is reduced by 0.6 V.

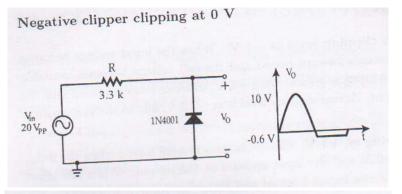
Biased clippers: Diodes in the positive and negative clippers are either forward biased or reverse biased in these circuits. Thus four combinations of diodes and dc sources create four different clipping circuits namely, forward biased positive clipper, reverse biased positive clipper, forward biased negative clipper and reverse biased negative clipper. When the dc source is connected such a way that it reverse biases the diode, the peak value of the output voltage is smaller than the input peak value by the amount of the dc voltage applied. Diode conducts only when the input voltage sufficiently high to forward biases the diode, the peak value of the output voltage the diode. When the dc source is connected such a way that it forward biases the diode, the peak value of the output voltage is greater than the input peak by the amount of the dc voltage applied.

PROCEDURE:

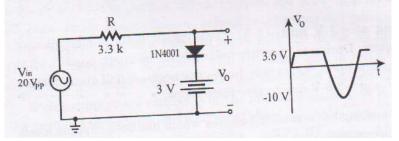
- 1. Set up the circuit one by one after testing the components. Apply 20V peak to peak sine at the input.
- 2. Observe the input & output waveforms simultaneously on the CRO screen.
- 3. Note the values & plot the waveform.

Circuit Diagrams & Model Waveforms:

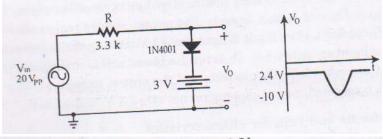




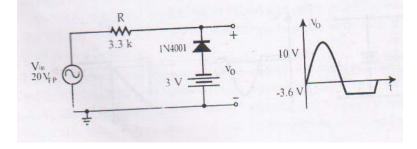
Positive clipper clipping at +3 V

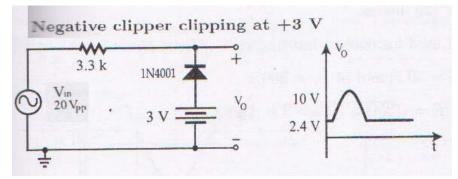


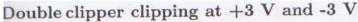
Positive clipper clipping at -3 V

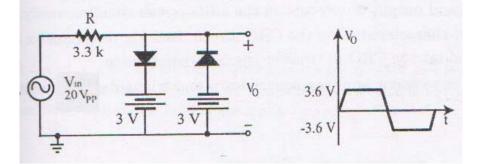


Negative clipper clipping at -3 V

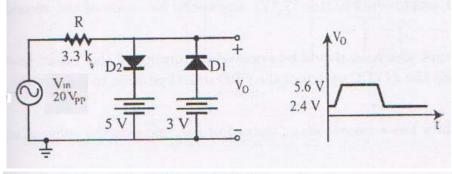




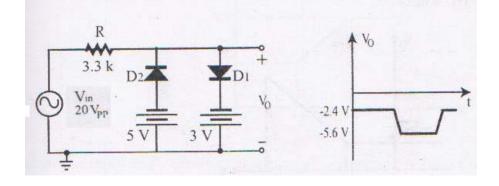


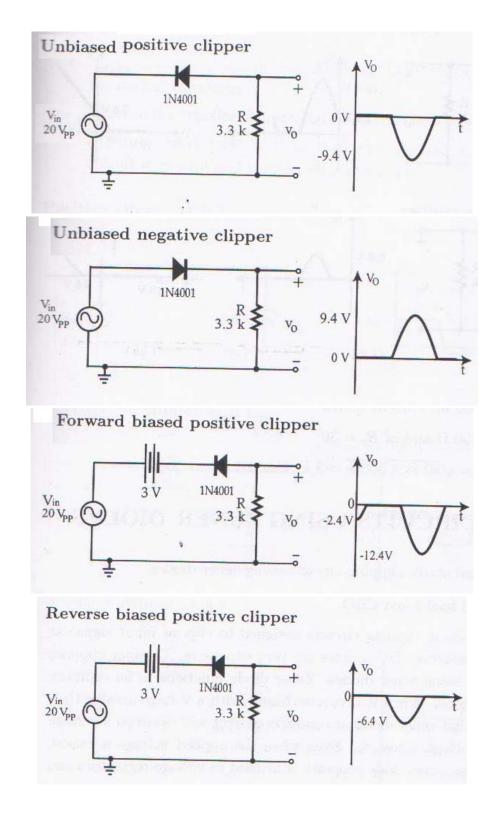


Slicer slicing at +5 V and +3 V



Slicer slicing at -5 V and -3 V





CLAMPING CIRCUITS

AIM:

To Study various clamping circuits using diodes.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Capacitor	1µF	1
3	DC source	3 V	1
4	Diode	1N4007	1
5	CRO	-	1
6	Multimeter	-	1
7	Function Generator	-	1

THEORY:

In some situations, it is necessary to add or subtract a dc voltage to a given waveform without changing its shape. Circuits used for this purpose are called clamping circuits. This can be achieved by connecting a dc source in series with the input. DC sources are very expensive and bulky equipments. A capacitor which is charged to a voltage & subsequently prevented from discharging can serve as a suitable replacement for a dc source. This principle is utilized in clamping circuits. The clamping level can be made at any voltage level by biasing the diode. Such a clamping circuit is called a biased clamper.

Positive clamper clamping at 0 V: Suppose the input voltage is represented by the expression V_m Sinwt. During one negative half cycle of the input sine wave, the diode conducts and the capacitor charges to V_m with positive polarity at the right side of the capacitor. During the positive half of the input sine wave, the capacitor cannot discharge since the diode does not conduct. Thus capacitor acts as a dc source of V_m volts in series with input signal source. The output voltage then can be expressed as $V_o = V_m + V_m$ Sinwt

Negative clamper clamping at 0 V: Suppose the input voltage is represented by the expression V_m Sinwt. During one positive half cycle of the input sine wave, the diode conducts and the capacitor charges to V_m with positive polarity at the right

side of the capacitor. During the positive half of the input sine wave, the capacitor cannot discharge since the diode does not conduct. Thus capacitor acts as a dc source of V_m volts in series with input signal source. The output voltage then can be expressed as $V_o = -V_m + V_m$ Sinwt

Positive clamper clamping at + 3V: During one negative half cycle of the input sine wave, capacitor charges through the dc source and diode till ($V_m + 3$) volts with positive polarity of the capacitor at its right side. The charging of the capacitor is limited to ($V_m + 3$) volts due to the presence of the dc source. The output is then expressed as $V_o = (V_m + 3) + V_m \operatorname{Sin}wt$

Positive clamper clamping at – **3V:** During one negative half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m - 3) volts with positive polarity of the capacitor at its right side. The charging of the capacitor is limited to (V_m - 3) volts due to the presence of the dc source. The output is then expressed as $V_o = (V_m - 3) + V_m$ Sinwt

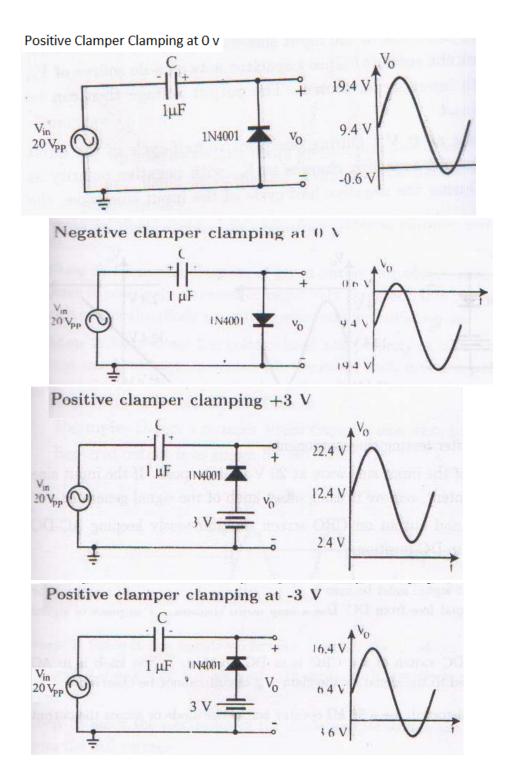
Negative clamper clamping at + *3V*: During one positive half cycle of the input sine wave, capacitor charges through the dc source and diode till ($V_m - 3$) volts with negative polarity of the capacitor at its right side. The charging of the capacitor is limited to ($V_m - 3$) volts due to the presence of the dc source. The output is then expressed as $V_o = -(V_m - 3) + V_m \operatorname{Sin}wt$

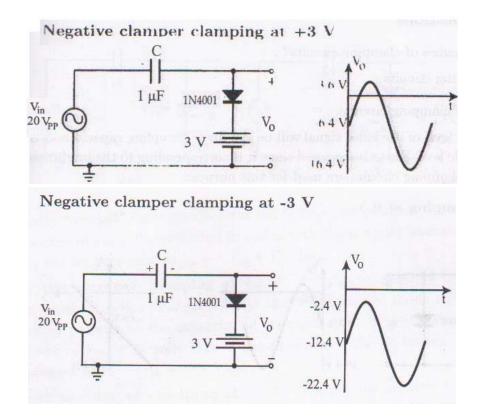
Negative clamper clamping at - 3V: During one positive half cycle of the input sine wave, capacitor charges through the dc source and diode till ($V_m + 3$) volts with negative polarity of the capacitor at its right side. The charging of the capacitor is limited to ($V_m + 3$) volts due to the presence of the dc source. The output is then expressed as $V_o = -(V_m + 3) + V_m$ Sinwt.

Note in the above discussion the voltage drop across the diode is neglected to simplify the discussion. Voltage across the diode (0.6 V) is not negligible compared to clamping voltage of 3 V. Therefore, it must be considered.

- 1. Set up the circuit one by one after testing the components. Apply 20V peak to peak sine at the input.
- 2. Observe the input & output waveforms simultaneously on the CRO screen keeping AC-DC switch of the CRO in DC position.
- 3. Note the values & plot the waveform.

Circuit Diagrams & Model Waveforms:





RC PHASE SHIFT OSCILLATOR

AIM:

To Study various clamping circuits using diodes.

APPARATUS REQUIRED:

S.NO.	Name of the Apparatus	Range	Quantity
1	Bread Board	-	1
2	Capacitor	0.1µF	4
3	Transistor	BC108	1
4	CRO	-	1
5	Multimeter	-	1
6	DC Source	-	1

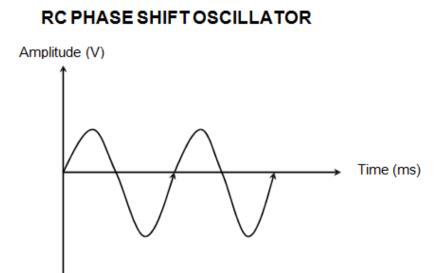
THEORY:

An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and positive feedback from the output to the input. RC phase shift oscillator is basically an amplifier circuit with positive feedback introduced. In this case the CE amplifier is followed by a frequency determining network. The R1, R2 combination provides dc potential divider bias and Ro, CE provides temperature stability and provides ac signal degeneration. The high pass or low pass RC - RC network may be used as positive feedback between input and output.

- 1. Set up the amplifier part of the oscillator and test the dc conditions. Ensure that the transistor is operating as an amplifier with the required gain.
- 2. Connect the feedback network and observe the sine wave on CRO screen and measure its amplitude and frequency.

3. Observe the waveforms at the base and collector of the transistor simultaneously on CRO screen and notice the phase difference between them

Model Waveforms:



Design:

FORMULA:

$$=\frac{1}{2 \pi RC \sqrt{6}}$$

DESIGN:

R = 200kΩ C = 100pF F=?
F =
$$\frac{1}{2 \pi RC \sqrt{6}}$$

= $\frac{1}{2 \pi \times 200 \times 10^3 \times 100 \times 10^{-12} \sqrt{6}}$
= 3.248 kHz

Circuit Diagram:

