Academic Course Description

SRM University
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

EM2002 **Microprocessors and Microcomputers**

First Semester, 2015-16 (Odd semester)

Course (catalog) description:
This course deals with the architecture of RISC and CISC processors, specifically ARM and Pentium processors. It also provides adequate study of assembly and C language programming of ARM processor. As an adjunct Lab, Nuvoton embedded development board, which uses Nuvoton ARM processor is studied. There are some case studies to explain the concepts.

Compulsory/Elective course: Core course

Credit hours: 4 credits

Course coordinator(s)

V.Natarajan, Prof., Department of ECE

Instructor(s)

Name of the instructor	Class handling	Office location	Office phone	Email	Consultations
Mr.V.Natarajan	A	TP11S2	2060	natarajan.v@ktr.srmuniv.ac.in	12.30PM to 1.30PM

Relationship to other courses

Pre-requisites : *Basic knowledge of 8 bit microprocessor.*

Assumed knowledge : *Basic mathematics.*

Following courses : -

Computer usage: C programming, Keil IDE, Nuvoton development board based software lab.

Class schedule : Four 50 minutes lecture sessions per week, for 11-12 weeks

Section	Schedule
A	DAY-1 – 1st Hr and 7 and 8 Lab DAY-2 – 2nd Hr DAY-3 – 5th Hr DAY-4 – 6th Hr DAY-5 – 3 and 4 Lab

Professional component

General	-	5%
Basic Sciences	-	5%
Engineering sciences & Technical arts	-	5%
Professional subject	-	85%

Broad area : Processor and instruction set architecture, C language application, assembly programming of ARM processor.

Test Schedule

S. No.	Test	Portions	Duration
1	Test-1	Session 1 to 4	2 Periods
2	Test-2	Session 1 to 12	3 Hrs

Course objectives

1. To make the student gain proficiency in developing software in C language, for ARM processor.

Course Learning Outcome

This course provides the foundation in the system concepts of microprocessor architecture RISC and CISC. Covers basic hardware and instruction set architectures, and C language. Students are expected to write programmes in C language and interfacing it with assembly language of ARM processors. Specific issues involved and methods used in using C for embedded software is dealt with. Through lecture and out-of-class assignments, students are provided learning experiences that enable them to:

1. Conceptualize system from given requirements.
2. Read and understanding microprocessor architectures.
3. Design and write programs using C, for developing embedded systems and other related applied areas.
4. Proficiency in developing applications using Nuvoton embedded boards.

Syllabus Contents

UNIT I - MICROPROCESSOR ARCHITECTURE (9 hours)

Instruction set - Data formats - Instruction formats - Addressing modes - Memory Hierarchy - register file - Cache - Virtual memory and paging - Segmentation - Pipelining - The instruction pipeline - pipeline hazards - Instruction level parallelism - reduced instruction set - Computer principles - RISC versus CISC - RISC properties - RISC evaluation - On-chip register files versus cache evaluation.

UNIT II - HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM (9 hours)

The software model - functional description - CPU pin descriptions - RISC concepts - bus operations - Super scalar architecture - pipelining - Branch prediction - The instruction and caches - Floating point unit - protected mode operation - Segmentation - paging - Protection - multitasking - Exception and interrupts - Input/Output - Virtual 8086 model - Interrupt processing - Instruction types - Addressing modes - Processor flags - Instruction set - Basic programming the Pentium Processor. Lab exercise.

UNIT III - HIGH PERFORMANCE RISC ARCHITECTURE (9 hours)

ARM: The ARM architecture - ARM organization and implementation - The ARM instruction set - The thumb instruction set - Basic ARM Assembly language program - ARM CPU cores.
The AMULET asynchronous ARM Processors. Embedded Operating Systems - Principle Components – Application case study – **VLSI Ruby II** Advanced communication processor.

UNIT IV - INTRODUCTION TO EMBEDDED C AND APPLICATIONS (9 hours)

C-looping structures – Register allocation – Function calls – Pointer aliasing – structure arrangement – bit fields – unaligned data and endianness – inline functions and inline assembly – portability issues. Embedded Systems programming in C – Binding & Running Embedded C program in Keil IDE – Dissecting the program -Building the hardware. Basic techniques for reading & writing from I/O port pins – switch bounce - LED Interfacing using Embedded C. Lab exercise.

UNIT V: EMBEDDED OPERATING SYSTEMS (sEOS): (9 hours)

Basics of sEOS – Timer Design consideration using sEOS- Multistate system design. Implementation of Traffic light sequencing using on chip UART for RS-232 communication-memory requirements. Case study – Intruder alarm system. Hyper Terminal based control-packet based control for LED interfacing- Security challenges and authentication process for Embedded Systems.

LAB: ARM DEVELOPMENT ENVIRONMENT (45 Hours)

Nuvoton Cortex M0 (Nu-LB-NUC140) Micro controller processor & its supporting tools. Lab exercises.

RFERENCES:

1. Daniel Tabak, "*Advanced Microprocessors-SIE*", Tata McGraw Hill. Inc., 2011.
2. James L. Antonakos, "*The Pentium Microprocessor*", Pearson Education, 2002.
3. Steave Furber, "*ARM system - on - chip architecture*", Addison Wesley, 2000.
4. Andrew N. Sloss, Dominic Symes, Chris Wright and John Rayfield, "*ARM System Developer's Guide, Designing and Optimizing System Software*", Elsevier, 2004.
5. David Seal, "*ARM Architecture Reference Manual*", Pearson Education, 2007.
6. Michael J. Pont, "*Embedded C*", Addison Wesley, 2002.

Weekly Teaching Plan

Week #	Topics	Readings	Assignments
1	Introduction to microprocessor and Nuvoton embedded board.	Nu_LB002 User Manual	
	Hardware design issues.	(class notes)	
2	Instruction word, addressing modes	Chapter 1 & 2 [Andrew Sloss] & (class notes)	
	RISC (ARM) processor architecture	Chapter 2 [Andrew Sloss]	
3	Memory hierarchy and cache memory	Chapter 12 [Andrew Sloss]	
	Pipelining and its requirements	Chapter 2 [Andrew Sloss]	Assignment - I
4	ARM processor architecture	Chapter 2 & 3 [Andrew Sloss]	
	ARM instruction set architecture, addressing modes.	Chapter – 3 & 4 [Andrew Sloss]	
5	ARM assembly language programming.	Chapter – 4 : [Andrew Sloss]	
	Recap of C language	Essential “C” & (class notes)	
6	Efficient C programming, for ARM processor – Part 1	Chapter – 5 : [Andrew Sloss]	
	Efficient C programming, for ARM processor – Part 2	Chapter – 5 : [Andrew Sloss]	Assignment - II
7	Nuvoton board software architecture.	NuMicro NUC140 data sheet	
	VLSI ruby, communication processor	Chapter – 9 : [Steve Furber]	
8	Keil IDE structure and use of tools	Nu_LB002 User Manual	
	Mid semester review of Lab assignments.	(class notes) & NuMicro NUC140 data sheet	
-	Self Study	Chapter 1 thro' 6 [Michael J.Pont]	Assignment - III
9	s EOS – an example	Chapter 8 :[Steve Furber]	
	Multistate software; traffic light sequencing using timer.	Chapter 8 :[Michael J.Pont]	
10	Intruder alarm systems	Chapter 10:[Michael J.Pont]	Assignment - IV
	Introduction to Pentium processor.	Chapter 4 : [James Antonakos]	
11	Super scalar architecture - pipelining	Chapter 4 : [Daniel Tabak]	
	Segmentation, paging, protection of memory in Pentium processor.	Chapter 4 : [Daniel Tabak]	
12	Virtual 8086 mode, Instruction set architecture.	Chapter 2,3 : [James Antonakos]	
	C language to assembly conversion for Intel architecture in PC.	Class notes	
13	Examples of assembly programs in Pentium. (Using gcc).	Class notes	Assignment – V

Evaluation methods

Assignments	-	5%
Test – I	-	20%
Test - II	-	20%
Surprise Test	-	5%
Final exam	-	50%

Prepared by: Mr.V. Natarajan, Professor, Department of ECE.

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Course-in-charge/Course-coordinator Professor-in-charge