Academic Course Description

SRM University
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

VL2118 Digital HDL Design and Verification

First Semester, 2014-15(Odd semester)

Course (catalog) description: HDL Programming is essential in the area of VLSI design . This syllabus has been framed based on the above requirement.

Compulsory/Elective course: Elective for M. Tech (VLSI Design) I year students

Credit hours: 3 credits

Course coordinator(s) N.Saraswathi , Asst. Professor(SG), Department of ECE

Instructor(s)

Name of the instructor	Class handling	Office location	Office phone	Email	Consultation
N.Saraswathi	M.Tech (VLSI Design)	TP10S1	-----	**saraswathy.n@ktr.srmuniv.ac.in**	Day 4, 2 – 4 pm

Relationship to other courses

Pre-requisites : Digital Systems

Assumed knowledge : Basic knowledge about Digital System and in C language

Following courses : ---

References

1. Ben Cohen ," VHDL : Coding styles and Methodologies " ,Kluwer Academic Publisher (1999),Reprint 2004.
2. J. Bhaskar ," A System C Primer " Galaxy Publications,2004.
3. Z.Navabi ,"VHDL :Modular Design and synthesis of cores and systems", McGraw Hill Publications, Reprint 2005.

Class schedule: Four 50 minutes Lecture sessions per week, for 11 weeks

Section	Schedule
VLSI Design	Day 2 Hrs 6 & 7 Day 3 Hr 3 Day 4 Hr 1

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area: Communication | Signal Processing | Electronics | **VLSI** | Embedded

Test Schedule - Theory

S. No.	Test	Portions	Duration
1	Cycle Test	Weeks 1 to 5	1 hr 40 min
2	Model Exam	Weeks 6 to 14	3 hrs

Course objectives

- To make the students write a code for a digital system in VHDL.
- To help the students gain a knowledge in System C.

Weekly teaching plan

Week #	Topics	Text / Chapter
1	Operators, Basic concepts	Ref [1], Chapter 2
	Entity and Architecture design,	
	System task and functions, Value set .	
	Data types	
2	Operands, Operators	Ref [1], Chapter 2,3
	Entity and Ports, Gate level modeling	
	Dataflow modeling	

Week #	Topics	Text / Chapter
	Behavioral modeling	
3	Test bench,	Ref [1] , Chapter 7,8,9
	Package	
	Functions, Sub Program	
	User defined attributes	
4	Specifications and Configurations	Ref [1], Chapter 8,9
	Delay modeling,	
	Pin to Pin delay, distributed delay modeling	
	Timing delay analysis	
5	FSM Design and Synthesis	Ref [1], Chapter 12 Ref [2], Chapter 1,3
	UART	
	Introduction to System C, Design methodology	
	Data types,-Bit ,logic,Integer	
6	Precision signed type&resolved types ,	Ref [2], Chapter 3,4
	User defined data type,Data operators	
	logical arithmetic ,relational operators	
	Vectors and ranges,	
7	sequential statements-if,loop,switch statements	Ref [2], Chapter 4,5
	Methods,	
	structures	
	SC_Module,file structure,	
8	Reading and writing port signals	Ref [2], Chapter 6
	Miscellaneous logic,	
	modeling basic combinational logic circuits	
	Multiplexer, Decoder,encoder	
9	Memory model, modeling an FSM ,	Ref [2], Chapter 7
	Moore FSM	
	Mealy FSM	
	Universal shift register	

Week #	Topics	Text / Chapter
10	**SC_THREAD process**	Ref [2], Chapter 9
	dynamic sensitivity	
	Constructors,arguments,	
	Ports,interfaces and channels	
11	Shared data types,	Ref [2], Chapter 9
	Module simulation algorithm	
	Run time environment,	
	Filter design (2 hrs)	

Evaluation methods

Cycle Test	-	20
Model Test	-	20
Surprise Test	-	5
Assignment	-	5
Final exam	-	50

Prepared by: N.Saraswathi ,Asst. Professor, Department of ECE

Dated: 20.08.2014 **Revision No.:** 0 **Date of revision:** NA